Research output

Defect-location identification for cell-aware test
3D test: no longer a bottleneck!

Handbook of 3D integration: Volume 4: Design, test, and thermal management

3D design-for-test architecture

Cost modelling for 2.5D and 3D stacked ICs

IEEE Std P1838: 3D test access standard under development

Optimization of test-access architectures and test scheduling for 3D ICs

Pre-bond testing through direct probing of large-array fine-pitch micro-bumps

Test and debug strategy for TSMC CoWoS® stacking process-based heterogeneous 3D-IC: a silicon study

Electrical modeling of STT-MRAM defects

On-chip toggle generators to provide realistic conditions during test of digital 2D-SoCs and 3D-SICs

Solutions to multiple probing challenges for test access to multi-die stacked integrated circuits

High density and high-bandwidth chip-to-chip connections with 20μm pitch flip-flop chip on fan-out wafer level package

Automatic generation of in-circuit tests for board assembly defects
**Test-station for flexible semi-automatic wafer-level silicon photonics testing**

**A DfT architecture and tool flow for 3D-SICs with test data compression, embedded cores, and multiple towers**

**At-speed testing of inter-die connections of 3D-SICs in the presence of shore logic**

**Cost components for 3D system integration**

**Two-step interconnect testing of semiconductor dies**

**Two-step interconnect testing of semiconductor dies**

**Transition delay detector for interconnection test**

**Transition delay detector for interconnect test**

**Transition delay detector for interconnect test**

**Transition delay detector for interconnect test**

**Controlled toggle rate of non-test signals during modular scan testing of an integrated circuit**

**Controlled toggle rate of non-test signals during modular scan testing of an integrated circuit**

**Creating options for 3D-SIC testing**
**Test access architecture for TSV-based 3D stacked ICS**

**Test access architecture for TSV-based 3D stacked ICS**

**Test access architecture for interposer-based 3D die stacks**

**Fault mode circuits**

**Fault mode circuits**

**On-chip testing using time-to-digital conversion**

**On-chip testing using time-to-digital conversion**

**A DfT architecture for 3D-SICs based on a standardizable die wrapper**

**On-chip testing using time-to-digital conversion**

**EDA solutions to new-defect detection in advanced process technologies**

**Test access architecture for TSV-based 3D stacked ICS**

**Test access architecture for TSV-based 3D stacked ICS**

**Method and device for testing TSVs in a 3D chip stack**

**Method and device for testing TSVs in a 3D chip stack**
3D DfT architecture for pre-bond and post-bond testing

Challenges in testing TSV-based 3D stacked ICs: test flows, test contents, and test access

Test cost analysis for 3D die-to-wafer stacking

Testing of an integrated circuit that contains secret information

Testing of an integrated circuit that contains secret information

Testing of an integrated circuit that contains secret information

A structured and scalable test access architecture for TSV-based 3D stacked ICs

Adapting to adaptive testing

Testing TSV-based three-dimensional stacked ICs

Bandwidth analysis of functional interconnects used as test access mechanism

On scan chain diagnosis for intermittent faults

Testing 3D chips containing through-silicon vias

Impact of 3D design choices on manufacturing cost
Guest editors’ introduction: the status of IEEE Std 1500-Part 2

Test data volume comparison: monolithic vs. modular SoC testing

Testing of an integrated circuit that contains secret information

Testing of SoCs with hierarchical cores: common fallacies, test access optimization, and test scheduling

Guest Editors’ introduction: the status of IEEE Std 1500

IEEE Std 1500 enables modular SoC testing

Testing of an integrated circuit that contains secret information

Analysis of the test data volume reduction benefit of modular SOC testing

Bandwidth analysis for reusing functional interconnect as test access mechanism

Bugs, moths, grasshoppers, and whales

Guest editors’ introduction: addressing the challenges of debug and diagnosis

Will test compression run out of gas?

Silicon debug and diagnosis: editorial

Test architecture and method

Selected best papers from ETS’06
Design and DfT of a high-speed area-efficient embedded asynchronous FIFO  

Embedded multi-detect ATPG and its effect on the detection of unmodeled defects  

ITC 2006 panels  

Test quality analysis and improvement for an embedded asynchronous FIFO  

Wrapper design for the reuse of a bus, network-on-chip, or other functional interconnect as test access mechanism  

Automatic test pattern generation  

Automatic test pattern generation  

Core test control  

On-chip test infrastructure design for optimal multi-site testing  

Hierarchy-aware and area-efficient test infrastructure design for core-based system chips  

Wrapper design for the reuse of networks-on-chip as test access mechanism  

Zero defect: mission impossible?  

Microelectronics and test in "The New Europe" - challenges and opportunities in research and industry  
Optimisation of on-chip design-for-test infrastructure for maximal multi-site test throughput

Security versus test quality: can we only have one at a time?

Optimal interconnect ATPG under a ground-bounce constraint

Redundancy modelling and array yield analysis for repairable embedded memories

Challenges in embedded memory design and test

IEEE Std 1500 compliant infrastructure for modular SOC testing

On-chip test infrastructure design for optimal multi-site testing of system chips

Test scheduling for modular SOCs in an abort-on-fail environment

Method of testing a memory

Test infrastructure design for the Nexperia™ home platform PNX8550 system chip

Method and apparatus for testing a memory array using compressed responses

IEEE P1500-compliant test wrapper design for hierarchical cores

Infrastructure for modular SOC testing

Security vs. test quality: can we really only have one at a time?
Test resource management and scheduling for modular manufacturing test of SOCS

Trends in testing integrated circuits

User-constrained test architecture design for modular SOC testing

Test access mechanism optimization, test scheduling, and tester data volume reduction for system-on-chip

SOC test architecture design for efficient utilization of test bandwidth

A test time reduction algorithm for test architecture design for core-based system chips

Efficient test access mechanism optimization for system-on-chip

Control-aware test architecture design for modular SOC testing

Creating value through test

Layout-driven SOC test architecture design for test time and wire length minimization

Minimizing pattern count for interconnect test under a ground bounce constraint

Optimal interconnect ATPG under a ground-bounce constraint

Yield analysis for repairable embedded memories

Recent advances in test planning for modular testing of core-based SOCs
Test wrapper and test access mechanism co-optimization for system-on-chip

A method for testing a memory array and a memory-based device so testable with a fault response signalizing mode for when finding predetermined correspondence between fault patterns signalizing one such fault pattern only in the form of a compressed response

A novel test time reduction algorithm for test architecture design for core-based system chips

A set of benchmarks for modular testing of SOCs

Cluster-based test architecture design for system-on-chip

Effective and efficient test architecture design for SOCs

Efficient wrapper/TAM co-optimization for large SOCs

How useful are the ITC 02 SoC test benchmarks?

On IEEE P1500's standard for embedded core test

On using rectangle packing for SOC Wrapper/TAM co-optimization

Test resource optimization for multi-site testing of SOCs under ATE memory depth constraints

The role of test protocols in automated test generation for embedded-core-based system ICs

Wrapper/TAM co-optimization, constraint-driven test scheduling, and tester data volume reduction for SOCs
Method for making a digital circuit testable via scan test

A method and a device for testing a memory array in which fault response is compressed.

Application of deterministic logic BIST on industrial circuits

A method for testing a memory array and a memory-based device so testable with a fault response signalizing mode for when finding predetermined correspondence between fault patterns signalizing one such fault pattern only in the form of a compressed response

Core test control

Test wrapper and test access mechanism co-optimization for system-on-chip

Core test control

Application of deterministic logic BIST on industrial circuits

On using IEEE P1500SECT for test plug-n-play

System chip test: how will it impact your design?

Wrapper design for embedded core test

Towards a standard for embedded core test: an example

Challenges in testing core-based system ICs

Testing embedded-core-based system chips
Zorian, Y., Marinissen, E. J. & Dey, S., Jun 1999, In : Computer. 32, 6, p. 52-60
The role of test protocols in testing embedded-core-based system ICs

A structured and scalable mechanism for test access to embedded reusable cores

Debugging systems on chips

Scan chain design for test time reduction in core-based ICs

Test protocol scheduling for embedded-core based system ICs

Testing embedded-core based system chips

Testability and test plan generation in hierarchical macro testing

AutoLISP voor beginners : een beknopte handleiding

Minimization of test control blocks

Prizes
Best 3D Track Paper at International Wafer-Level Packaging Conference 2018
Armita Podpod (Recipient), Dimitrios Velenis (Recipient), Alain Phommahaxay (Recipient), Pieter Bex (Recipient), Ferenc Fodor (Recipient), Erik Jan Marinissen (Recipient), Kenneth June Rebibis (Recipient), Andy Miller (Recipient), Gerald Beyer (Recipient) & Eric Beyne (Recipient), 25 Oct 2018

Best Paper Award Chrysler-Delco-Ford Automotive Electronics Reliability Workshop 1995
Erik Jan Marinissen (Recipient), Oct 1995

Best Paper Award IEEE International Board Test Workshop (BTW’02)
Erik Jan Marinissen (Recipient), Ben Bennetts (Recipient) & H.G.H. (Bart) Vermeulen (Recipient), Oct 2002

Best Paper Award IEEE Latin-American Test Symposium 2019
Zhan Gao (Recipient), Santosh Malagi (Recipient), Erik Jan Marinissen (Recipient), Joe Swenton (Recipient), Jos A. Huiskens (Recipient) & Kees G.W. Goossens (Recipient), 13 Mar 2019
Best Paper Award International Wafer-Level Packaging Conference 2018
Arnita Podpod (Recipient), Dimitrios Velenis (Recipient), Alain Phommahaxay (Recipient), Pieter Bex (Recipient), Ferenc Fodor (Recipient), Erik Jan Marinissen (Recipient), Kenneth June Rebibis (Recipient), Andy Miller (Recipient), Gerald Beyer (Recipient) & Eric Beyne (Recipient), 25 Oct 2018

HiPEAC Technology Transfer Award 2015
Mottaqiallah Taouil (Recipient), Said Hamdioui (Recipient) & Erik Jan Marinissen (Recipient), 2015

IEEE Computer Society Certificate of Appreciation
Erik Jan Marinissen (Recipient), Jul 2005

IEEE Computer Society Certificate of Appreciation
Erik Jan Marinissen (Recipient), Sep 2003

IEEE Computer Society Certificate of Appreciation
Erik Jan Marinissen (Recipient), Oct 2001

IEEE Computer Society Golden Core Member
Erik Jan Marinissen (Recipient), 2005

IEEE Computer Society Meritorious Service Award
Erik Jan Marinissen (Recipient), May 2005

IEEE Fellow
Erik Jan Marinissen (Recipient), 15 Dec 2010

IEEE Senior Member
Erik Jan Marinissen (Recipient), 2000

IEEE Standards Association Certificate of Appreciation
Erik Jan Marinissen (Recipient), Aug 2005

IEEE Standards Association Emerging Technology Award 2017
Erik Jan Marinissen (Recipient), 3 Dec 2017

Most Inspirational Presentation Award Semiconductor Wafer Test Workshop (SWTW’13)
Gunther Boehm (Recipient), Samuel Kalt (Recipient), Joerg Kiesewetter (Recipient), Armin Klumpp (Recipient), Wolfgang Schaeffer (Recipient) & Erik Jan Marinissen (Recipient), Jun 2013

Most Significant Paper Award IEEE International Test Conference (ITC’08)
Erik Jan Marinissen (Recipient), Robert Arendsen (Recipient), G.A.A. Bos (Recipient), Hans Dingemanse (Recipient), G.E.A. Lousberg (Recipient) & Clemens R. Wouters (Recipient), Oct 2008

Most Significant Paper Award IEEE International Test Conference (ITC’10)
Erik Jan Marinissen (Recipient), Sandeep Kumar Goel (Recipient) & G.E.A. Lousberg (Recipient), 5 Nov 2010

National Instruments Engineering Impact Award 2017
Ferenc Fodor (Recipient), Bart De Wachter (Recipient), Erik Jan Marinissen (Recipient), Joerg Kiesewetter (Recipient) & Ken Smith (Recipient), 26 May 2017

Jeroen De Coster (Recipient), Peter De Heyn (Recipient), Marianna Pantouvaki (Recipient), Brad Snyder (Recipient), Hongtao Chen (Recipient), Erik Jan Marinissen (Recipient), Philippe Absil (Recipient), Joris Van Campenhout (Recipient) & Bryan Bolt (Recipient), 16 Jul 2017
TTTC Meritorious Service Award
Erik Jan Marinissen (Recipient), 27 May 2015

TTTC Meritorious Service Award
Erik Jan Marinissen (Recipient), 23 Oct 2014

Press / Media
3D Test: No Longer a Bottleneck!
Erik Jan Marinissen
15/05/19
1 item of media coverage

A Fully Automatic Test System for Characterizing Wide-I/O Micro-Bump Probe Cards
Erik Jan Marinissen
14/06/17
1 item of media coverage

Best Paper Award at LATS2019 for Zhan Gao
Zhan Gao & Erik Jan Marinissen
3/04/19
1 item of media coverage

Cell-Aware Test: Research Cooperation Between Cadence, imec, and TU Eindhoven...Now Shipping in Modus DFT Software Solution
Erik Jan Marinissen & Zhan Gao
14/06/19
1 media contribution

Collecting Awards at SEMICON West
Erik Jan Marinissen
1/09/17
1 item of media coverage

Developing Silicon Photonics Technologies With A Wafer-Level Test Station
Erik Jan Marinissen
5/02/18
1 item of media coverage

imec and Cadence Collaboration on Test – Translating Academic Research into Production Software
Erik Jan Marinissen
10/06/19
1 media contribution

Imec and Cascade Microtech Develop First Automatic Probe System for Advanced 3D Chips
Erik Jan Marinissen
24/05/17
1 media contribution

imec, TU Eindhoven, and Cadence - Advances in Defect Location Identification
Zhan Gao & Erik Jan Marinissen
30/05/19
1 media contribution
imec, TU Eindhoven, and Cadence – Advances in Defect Location Identification
Zhan Gao, Santosh Malagi, Erik Jan Marinissen, Joe Swenton, Jos A. Huisken & Kees G.W. Goossens
7/05/19
1 media contribution

New Solution for Testing Chips Prior to 3D Stacking
Erik Jan Marinissen
21/08/17
1 media contribution

Test magic descends on Disneyland with ITC
Erik Jan Marinissen
4/10/15
1 item of media coverage

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