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400 Gbps 2-Dimensional Optical Receiver Assembled on Wet Etched Silicon Interposer

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Abstract— In this paper, based on a wet etched silicon interposer, we propose a 2.5D assembly of two dimensional optical transceivers for 400 Gbps parallel optical interconnections. In this opto-electronic packaging, two dimensional optical matrix is formed as 250 μm in both the x - and y - directions by exploiting commercial opto-electronic arrays, and a compact optical interface is used to couple the light channels with fiber ribbons. Each quadrant of the optical matrix is connected with its BiCMOS IC part via impedance matched co-planner wave guides. The shortest traces between optics and BiCMOS ICs can be 300 μm , benefiting from flip-chip technology. The process flow of silicon interposer fabrication is illustrated. With flip-chip bonding, 25 Gbps 2D 16-channel receiver is assembled on the silicon interposer, and the sub-module, including the optical interface, is scaled down to 4 mm by 6 mm. In addition, the performance of this assembled module is fully characterized. Uniform and clear eye patterns are captured for all of the channels. Receiver sensitivities are also tested for all channels at 25.78 Gbps, 2^{31} -1 PRBS, with the variation less than 1.5 dB at error free operation.

Keywords - silicon interposer, 2.5D stacking, optical interconnects, 2-dimensional optical transceiver.

I. INTRODUCTION

Driven by Moore's law, the performance of integrated-circuit (IC) chips doubles every 18 months, which leads to a limitation of off-chip interconnections, as the bandwidth of electrical connections cannot scale at the same pace as their dimensions shrinking [1]. Optical interconnects offer a higher bandwidth-distance product, comparing with electronic links, and have taken over most of the long distance communications [2]. Meanwhile, in the data center (DC), as the bandwidth demand of servers continues to increase, optical interconnects trend to be applied to short links and integrated closer to the application specific integrated circuits (ASICs) of the servers [3].

Transceivers, converting electrical signals into the optical domain and back, are essential building blocks in DC networks. Currently, transceivers for short reach optical interconnections are mostly based on vertical cavity surface emitting laser (VCSEL) and normal surface photo diode (PD) [4]. Using these optics, a cost-effective solution - quad small form-factor pluggable (QSFP) modules are currently

employed for 100 Gbps links, and emerging QSFP double density (QSFP-DD) will govern 200 Gbps and 400 Gbps Ethernet [5]. However, with the growth of data communication, manufacturers of such modules are under constant pressure to deliver low cost, small form factor and high bandwidth solutions, in order to integrate the transceivers closer to ASICs. Opto-electronic packaging is one of the main challenges, since both electrical interface and optical interface need to be considered to meet the requirements [6].

Two dimensional (2D) optical interconnects may be a viable packaging solution for such transceivers, since it is possible to offer high bandwidth density with small form factor. In addition, the surface area of ICs may be utilized, where optical ports can be placed [7]. However, there will be more requirements for the optical and electrical connections, comparing with 1D array optics. Previously, proposed schemes were based on post-processed active CMOS devices and specially designed optics [8, 9], which inevitably lead to a high cost of the modules. An alternative, which use commercially available components for assembly, will minimize the cost.

Silicon interposer is a good candidate for the multichip assembly, since its fabrication is compatible with the semiconductor technology. It has attracted much attention recently for microelectronic and opto-electronic packaging [10]. Besides, wet etching of silicon is a low cost method for optical through silicon vias, which enables optical access and electrical connections from different sides of silicon interposer. 2.5D and 3D embedding schemes have been proposed to obtain compact packaged modules [11, 12]. However, the resolution of lithography is low in the deeply etched cavity in standard contact lithography. To achieve 2D optical inputs/outputs, a fine resolution routing is needed. We propose a 2.5D package approach, using a pre-processed passive silicon interposer, where commercially available dies, working at 10 Gbps, are assembled only at the very last step [13].

In this paper, by using a similar package scheme, for the first time, 4×4 channels optical module is designed, assembled and tested, using commercially available 25 Gbps chip sets. The testing results show the packaged receiver module offers 400 Gbps data rate with in an area of 4 mm $\times$ 6 mm, offering a bandwidth density of 16.7 Gbps/mm². This paper is organized as follows. Firstly, the concept of assembly is detailed. Secondly, the fabrication process is illustrated,

following four lithography steps. Thirdly, four pairs of 4-channel dies together with optical interface (OI) are bonded on the silicon interposer through flip-chip bonding technology. Finally, the performance of the packaged receiver is fully characterized.

II. CONCEPT OF ASSEMBLY

As shown in Fig. 1, the schematic drawing, 4 pairs of the commercial opto-electronics dies [14] and BiCMOS IC chips [15] are assembled on a patterned silicon interposer. The pitch of the 2D optical matrix is formed as $250\ \mu\text{m}$ in both the x - and y - directions using four commercial 4-channel opto-electronic ICs flip-chip bonded side by side in a $1\ \text{mm}^2$ area. The four BiCMOS ICs are connected with these four quadrants of the optical matrix through coplanar waveguides (CPWs), which are designed to match the impedance with TIA and to reduce the crosstalk. Short distance ($300 - 700\ \mu\text{m}$) between opto-electronics and BiCMOS IC chip is realized through a compact flip-chip design. The outputs of the BiCMOS IC chip are redistributed to the 1D pads on the two opposite edges of silicon interposer with $250\ \mu\text{m}$ pitch through differential traces. Besides, the power rails and I²C bus lines are also routed to the other two edges of silicon interposer, which will be beneficial for further package.

Figure 1. Scheme of 2.5D assembly of electronics, optics, optical interface and the heat sink.

For a simple and low cost optical access solution, a single compact OI, designed and optimized by using a PRIZM[®] MT ferrule, is attached on the opposite side of the silicon interposer: collimated lenses system between ferrules is employed to couple the light with standard fiber ribbons. This solution supports emitters/detectors with a $250\ \mu\text{m}$ pitch in both the x - and y - directions coupling with standard fiber. It can be scaled up to a maximum of 4×16 lanes [16]. In this scheme, the light from the 4×4 channels penetrate the silicon interposer through wet etched vias and couple into the 16 channels of the OI. The suggested heat sink can be also placed around the OI, since the silicon interposer itself is a good heat conductor. The fully assembled module is within an area of $4\ \text{mm} \times 6\ \text{mm}$, offering a bandwidth density of $16.7\ \text{Gbps}/\text{mm}^2$.

III. SILICON INTERPOSER FABRICATION

The fabrication includes four steps of lithography, starting on a cleaved 1-inch silicon sample with $210\ \mu\text{m}$ thickness. The wafer thickness is selected to optimize the distance between optical dies and OI, and thinned down to $180\ \mu\text{m}$ in the

potassium hydroxide (KOH) solution. A layer of silicon nitride (SiN_x) and a layer of electro-plating base are deposited and sputtered before electro-plating. Metal traces and bumps are then plated respectively. After that, the openings for wet etching of optical through silicon vias (OTSVs) are defined on both sides of the silicon interposer by selectively removing SiN_x . The photography of processed wafer is taken under microscope, in Fig. 2, shows the results of three lithography steps, and the plated electrical interfaces and matrix of optical ports are all well-defined. Finally, after 120 minutes double-side wet etching, the OTSVs are vertically formed, and the process is complete.

Figure 2. Micrograph of patterned photoresist for wet etching of OTSVs. Details of the PD channel connections is also shown. One quadrant is connected with one TIA/LA, with the noted channels. The plated CPWs can be clearly seen, and ground (G) and signal (S) are indicated.

Figure 3. SEM photo of complete silicon interposer, including etched OTSVs for 16 optical channels and short CPWs from BiCMOS ICs to opto-electronics dies.

A SEM photo shows the wet etched OTSVs, in Fig. 3. The sidewall of OTSVs are vertically formed through well

controlled etching time. In addition, the cleaving lines are also designed and etched on the bottom side, together with the openings of optical ports. According to the principle of anisotropic wet etching of silicon, the depth of the grooves will be $70\text{ }\mu\text{m}$, when the width is $100\text{ }\mu\text{m}$. With the help of the etched grooves, fabricated interposers on the silicon wafer can be easily separated.

IV. ASSEMBLY OF RECEIVER

After cleaving, the fabricated silicon interposer can be used for photonic and electronic dies flip-chip bonding. Alignment and heat reflow ($270\text{ }^{\circ}\text{C}$) are performed on a die bonder, shown in Fig. 4, a side view photo of flip chip holder and PD dies. The gold pads on the PDs and the plated bumps on the silicon interposer are thermal compression bonded. In order to keep the $250\text{ }\mu\text{m}$ pitch of optical ports, two PDs are placed next to each other, since the width of PD die is $250\text{ }\mu\text{m}$. This requires a high precision of flip-chip bonding.

Figure 4. Side view of flip-chip bonding process; the PDs are picked and placed by a special holder, and bonded side by side to keep $250\text{ }\mu\text{m}$ pitch of optical ports.

Figure 5. microphotography of four assembled PD arrays bonded on silicon interposer.

The photography of the top side of silicon interposer are shown in Fig. 5. In order to check the electrical connections, we measure the current–voltage characteristic of all channels, and they show uniform results. The leakage current is also tested below 1 nA at reverse voltage of 2.0 V . In addition, as shown in Fig. 6, micro photography is taken from bottom side of silicon interposer. Through OTSVs, we can clearly see the apertures of PDs. However, there is slightly misalignment between PD array 2 (row 2) and PD array 3 (row 3).

Figure 6. micrograph of assembled PDs, taken from bottom side of silicon interposer.

After that, 4 TIA/LAs, which are supplied with solder bumps, are reflowed ($235\text{ }^{\circ}\text{C}$) on the die bonder with standard soldering reflow process. Finally, the designed OI is placed with the same die bonder. Passive alignment is performed by aligning the apertures of PDs and the lenses on the OI. Transparent epoxy, EPO-TEK[®] 301, is used to fix the OI at the bottom of the silicon interposer, with 2 hour curing at $65\text{ }^{\circ}\text{C}$.

Figure 7. Side photograph of the assembled module on a testing clamp. PRIZM[®] MT ferrule, connected with fiber ribbons, accesses to the module through guide pins and holes.

The fully assembled module is ready for high speed characterization. As shown in Fig. 7, the commercial PRIZM[®] MT ferrule with fiber ribbons is easily access to the module, though the guide pins and holes. Bonded opto-electronics and BiCMOS ICs can be also seen in this photo. The module connected with PRIZM[®] MT ferrule is fixed on a clamp for testing.

V. PERFORMANCE CHARACTERIZATION

Performance characterization is performed for the assembled 16-channel receiver module on a probe station. The fiber ribbons from PRIZM[®] MT ferrule further breaks out to LC fibers for optical input signals. A commercial QSFP28 (100G-SR4-S, Cisco) is used as a high speed light sources.

As shown in Fig. 8, via DC probes, the power rails and I²C bus lines are connected to a 3.3 V power supply and a microcontroller, respectively. Then, serial data can be transferred for full chip configuration. In order to test high speed performance, multiple differential RF probes (signal-signal) are connected on the fan-out pads of the silicon interposer for electrical output signals.

Figure 8. photography of the fully assembled receiver module and its testing setup.

A. Signal Integrity Characterization

All channels are tested at 25.78 Gbps, with a 2³¹-1 pseudo random bit stream (PRBS). The converted electrical signal outputs from assembled receiver module, are fed into an oscilloscope through differential probes. The open and uniform eye patterns are captured for all 16 channels, shown in Fig. 9, grouped with four TIA/LAs.

Receiver sensitivity characterization is also performed for all channels by an error detector. Bit error rate (BER) curves is shown in Fig. 10, all channels demonstrated error free operation (level 10⁻¹²), with the sensitivities between -7.1 dBm and -5.6 dBm. The variation of received power at level 10⁻¹² of all channels is 1.5 dB. This is mainly due to the variation of light coupling efficiency of the OI, which is causes by slightly misalignment between lenses of the OI and apertures of PDs.

In addition, we also test the performance at 28.05 Gbps, 2³¹-1 PRBS, with the clock data recovery (CDR) function enabled. The electrical outputs of one channel of the packaged module is tested. In Fig. 11, an open eye diagram is captured, although the QSFP28 module is only designed for 25 Gbps and produce a lot jitter in the optical input signal. This result indicates the packaged module could offer 448 Gbps data capacity.

Figure 9. the eye patterns for each channel working at 25.78 Gbps, 2³¹-1 PRBS.

Figure 10. Measured bit error rate curves for all 4 channels (CH) of 4 TIA/LAs (T).

Figure 11. The eye patterns of electrical output of package receiver working at 28.05 Gbps, $2^{31}-1$ PRBS.

B. Crosstalk Penalty

Crosstalk is characterized by power penalties on receiver sensitivity of the receiver module. We generate two optical signals from the QSFP28 module, with the same 25.78 Gbps $2^{31}-1$ PRBS, and couple them to two adjacent channels, channel 2 and channel 3 in TIA/LA4. We test the BER performance of channel 2 using the same error detector, and results are shown in Fig. 12. There is 0.4 dB power penalty on the performance of channel 2 at BER level 10^{-12} , if channel 3 is fed with optical signal. The crosstalk impact can be further suppressed by mounting decoupling capacitors next to the chips on the silicon interposer.

Figure 12. The BER curves of channel 2 of TIA/LA 4; channel 2 alone, channel 2 and channel 3 are fed with optical signals. The tested crosstalk penalty is 0.4 dB.

VI. CONCLUSION

We assembled 4 pairs of commercially available 4-channel TIA/LAs and PDs in a 2D arrangement based on the low cost wet etched silicon interposer, within an area of $4 \text{ mm} \times 6 \text{ mm}$. The compact optical connector, which can support up to 4×16 lanes, is employed to enable the optical access through OTSVs. The process flow of silicon interposer is detailed demonstrated. Thermal compression bonding and solder reflow are used for the opto-electronics and BiCMOS ICs flip-chip bonding. In addition, the 1D fan-out design enables an easy further package of this module.

The performance of packaged module is fully characterized. All channels work at error free operation at 25.8 Gbps, with the variation of receiver sensitivity 1.5 dB at BER level 10^{-12} , and slight crosstalk impact (0.4 dB). Further, one of the channels is tested at 28.05 Gbps, and shows an open eye diagram, which indicates the module could offer 448 Gbps data capacity.

In the future, both 400 Gbps transmitter and 200 Gbps transceiver can be easily assembled through this novel opto-electrical packaging technology, which can be used to fulfill the demands of next generation of optical interconnects in data centers. In addition, this platform can also support > 1 Tbps data rate, whenever more channels (4×10 channels, or even 4×16) are employed.

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