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A 10-b 20-MS/s SAR ADC With DAC-Compensated Discrete-Time Reference Driver

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Abstract—Successive approximation register (SAR) analog-to-digital converters (ADCs) with a charge-redistribution (CR) digital-to-analog converter (DAC) usually require a power-hungry reference driver or large decoupling capacitance, occupying significant chip area. This paper presents a CR SAR ADC with an integrated low-power and area-efficient discrete-time reference driver. An on-chip capacitor is pre-charged to the reference voltage during the tracking phase and drives the DAC of the SAR ADC passively during the conversion phase. The charge sharing between the driving capacitor and the DAC will cause reference voltage drop and code-dependent non-binary DAC switching steps. This is compensated by switching an auxiliary DAC array together with the regular binary DAC array according to each specific code. The compensation relaxes the required decoupling capacitor and introduces little overhead in power or chip area. The above-mentioned driving scheme is applied to a 10-b 20-MS/s successive approximation register (SAR) ADC fabricated in 65-nm CMOS, where the first three DAC switching steps are compensated. Moreover, redundancy is utilized to reduce the impact of reference voltage drop further. With a near-Nyquist input tone, the signal to noise and distortion ratio (SNDR) and spurious free dynamic range (SFDR) of the SAR ADC with the uncompensated reference driver are 54.4 and 58.9 dB, respectively. After enabling the compensation, the SNDR and SFDR are increased to 56.8 and 72.4 dB, achieving 2.4 and 13.5 dB improvement, respectively. The SAR ADC consumes a total power of 133.1 μ W while the discrete-time reference driver with and without compensation add 17.2 and 14.0 μ W, respectively. The SAR ADC with integrated reference driver occupies a chip area of 0.081 mm² where 8.6% is occupied by the reference driver.

Index Terms—Area efficient, charge-redistribution (CR), discrete time, low power, reference driver, SAR analog-to-digital converter.

I. INTRODUCTION

SAR analog-to-digital converters (ADCs) are well known for their excellent energy efficiency and friendliness to technology scaling thanks to the simple and highly digitized architecture. For instance, the prevailing capacitive digital-to-analog converters (DACs) in SAR ADCs are only comprised of capacitors and switches, consuming only dynamic energy.

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Fig. 1. SAR ADC reference voltage driver. (a) Active driver. (b) Passive driver.

However, the reference voltage driver for the DAC can be costly in power consumption or chip area. This is commonly neglected as most publications only consider the ADC core.

In general, two capacitive DAC types are possible: charge-sharing (CS) DACs and charge-redistribution (CR) DACs. A CS DAC is first proposed in [1] to ease the harsh requirements for the reference driver. The binary search is realized in charge domain passively by connecting the pre-charged binary DAC array successively to the sampling capacitors, where the reference driver is only needed during the tracking phase of a SAR ADC. However, a CS DAC is complex and sensitive to parasitic capacitances. The CS topology will attenuate the DAC output voltage, increasing the noise requirement for the comparator. With the absence of the above-mentioned disadvantages of CS DACs, CR DACs are more widely used despite the requirement for a costly reference driver due to the frequent switching activity of the DAC.

The conventional driving scheme for the CR DAC in a SAR ADC is shown in Fig. 1(a), where one uses either a power-hungry driver or a large decoupling capacitor (C_{DEC}) while a low-power driver is recovering the reference voltage slowly. As shown in Fig. 2(a), for the former scheme, the reference driver must recover the reference voltage ($V_{REF,DRI}$) within a short time, T_{REC} (much smaller than sampling period T_S), resulting in a power-hungry driver. In [2] and [3], the power consumption of the driver is $9\times$ and $25\times$ the SAR ADC power, respectively. The latter scheme reduces the power consumption by using a large decoupling capacitor. Since V_{DROP} of the reference voltage is usually signal dependent, it must be minimized to provide a near-constant reference voltage, requiring a large decoupling capacitor (C_{DEC}) as shown in Fig. 2(b). The ratio between C_{DEC} and C_T (the total capacitance at each side of the DAC) can be easily

Fig. 2. Waveforms of different DAC driving schemes for SAR ADCs. (a) $V_{REF, DRI}$. (b) $V_{REF, DEC}$. (c) [6]. (d) [7]–[9].

beyond $200\times$ [4] and sometimes an off-chip capacitor is adopted [5]. In order to get rid of both a power-hungry buffer and a large C_{DEC} , some solutions have been presented using a small C_{DEC} driving the DAC passively and eliminating the signal dependence of the reference voltage drop as shown in Fig. 1(b). In [6], one capacitor (C_1) is pre-charged to V_{REF} and besides, an extra capacitor array (C_2) is pre-charged to a voltage higher than V_{REF} . During the conversion, according to the specific code and charge consumption, a part of C_2 is connected to C_1 to drive the DAC together to maintain a constant reference voltage [Fig. 2(c)]. Equivalently, the charge consumed by the DAC is provided by part of C_2 . This scheme requires an extra reference voltage higher than V_{REF} (usually $V_{REF} = V_{DD}$), making it difficult to produce and no chip implementation of this scheme is given. In [7]–[9], the reference voltage drop is not eliminated but made signal independent. In [7], similar C_1 and C_2 are used while C_1 is pre-charged to V_{REF} and C_2 is discharged to ground. During conversion, a part of C_2 is connected to C_1 for each switching step to draw the same amount of charge from C_1 irrespective of the signal. In [8] and [9], the DAC, driven by a pre-charged reservoir capacitor [8] or multiple reservoir capacitors (one for each bit) [9], is designed in a way that the charge consumption is signal independent. In [7]–[9], calibration and digital post processing are required to correctly reconstruct the output, increasing the implementation complexity and power consumption.

In this paper, which is an improved version of [10], a low-power and area-efficient solution for the reference driver is proposed by combining a discrete-time reference driver with an analog DAC compensation technique. In the prototype, a decoupling capacitor, C_{DEC} , equal to $20 \cdot C_T$ is pre-charged to the reference voltage during the tracking phase and drives the CR DAC passively during conversion. The CS between C_{DEC} and C_T causes a signal-dependent reference voltage drop and non-binary switching steps, which is corrected by switching an

TABLE I
FIRST THREE DAC SWITCHING STEPS WITH IDEAL REFERENCE DRIVER

V_{REF} [V]	C_i	ΔV_{DAC} [V]
1	$8C$	0.5
1	$4C$	0.25
1	$2C$	0.125

auxiliary DAC in addition to the binary DAC array according to each specific code. Different from [7]–[9], this auxiliary DAC does not compensate the reference voltage, but it compensates the DAC output signal directly. Rather than compensating all bits (which would be complex), only the first three MSB steps are corrected, which only requires an auxiliary DAC capacitance of $1.4\% \cdot C_T$. The presented reference driver requires no high-bandwidth operational amplifier (OPAMP) or large decoupling capacitance and the compensation is realized in the analog domain without calibration or digital processing, hence being low power and area efficient simultaneously.

This paper is organized as follows. Section II describes the principle of the discrete-time reference driver. In Section III, a 10-b SAR ADC using this driver is introduced. Measurement results are shown in Section IV and Section V concludes this paper.

II. DAC-COMPENSATED DISCRETE-TIME REFERENCE DRIVER

A. Operation of a CR DAC

The CR DAC in a SAR ADC samples the input signal and performs a binary search. For a differential split-monotonic DAC [11] where each DAC bit is split into two half pairs, the differential DAC output voltage shift of the i th switching step can be expressed as

$$\Delta V_{DAC}(i) = 2 \cdot \frac{C_i}{C_T} \cdot V_{REF} \quad (1)$$

where C_i is the switched binary-scaled capacitance at each side of the DAC, C_T is the total capacitance at each side of the DAC, and V_{REF} is the reference voltage. In order to achieve binary steps of $\Delta V_{DAC}(i)$, V_{REF} should be constant, which may cost a lot of effort as discussed in Section I. One example of an ideal binary search in a split-monotonic DAC is shown in Table I.

B. CR DAC Driven by C_{DEC}

Considering a single SAR conversion where the DAC is passively driven by a pre-charged decoupling capacitor, C_{DEC} [as shown in Fig. 1(b)], in order to perform an accurate binary search, C_{DEC} has to be large enough to minimize V_{DROP} [Fig. 2(b)]. If C_{DEC} is not large enough, V_{REF} on C_{DEC} will change according to the specific code, causing signal-dependent non-linearity. The DAC output voltage shift can be expressed as

$$\Delta V'_{DAC}(i) = 2 \cdot \frac{C_i}{C_T} \cdot V_{REF}(D_i) \neq \frac{1}{2} \Delta V'_{DAC}(i-1) \quad (2)$$

TABLE II
FIRST THREE UNCOMPENSATED DAC SWITCHING
STEPS WITH PASSIVE DRIVER

V_{REF} [V]	C_i	ΔV_{DAC} [V]
$1 \rightarrow 0.95$	$8C$	0.48
$0.95 \rightarrow 0.88$	$4C$	0.22
$0.88 \rightarrow 0.85$	$2C$	0.10

TABLE III
FIRST THREE COMPENSATED DAC SWITCHING
STEPS WITH PASSIVE DRIVER

V_{REF} [V]	C_i	ΔV_{DAC} [V]
$1 \rightarrow 0.95$	$8C$	0.48
$0.95 \rightarrow 0.87$	$4C + C_{a2}$	0.24
$0.87 \rightarrow 0.83$	$2C + C_{a3}$	0.12

where D_i is the current code, varying from 0 to $2^i - 1$, and $V_{\text{REF}}(D_i)$ is the reference voltage after switching to code D_i . One example of the above-mentioned case is illustrated in Table II. The first column denotes the reference voltage change before and after switching C_i , which is code dependent. Only one case is shown in Table II. Due to the CS, the reference voltage is dropping and causes code-dependent non-binary search steps, leading to ADC non-linearity.

C. DAC Switching Correction

Looking back at (2), it can be noted that the non-binary search is caused by the non-constant $V_{\text{REF}}(D_i)$, which is inevitable with a small C_{DEC} . If an adjusted “ C_i ” can be chosen according to $V_{\text{REF}}(D_i)$, the non-binary search can be corrected. As shown in Table III, for the second and third switching steps, a specific auxiliary capacitor (C_{a2} and C_{a3}) can be switched in addition to the capacitors from the binary DAC array. Although the reference voltage still suffers from the code-dependent drop, V_{DAC} can be made binary scaled again. Since the charge consumption of each switching is code dependent, the resulting reference voltage drop and the required auxiliary capacitors (C_{a2} and C_{a3}) also vary from code to code. Table III only illustrates the case for one code. Compared with Table II, the reference voltage drop (first column) is slightly different due to the extra auxiliary capacitors being switched. Note that V_{REF} on C_{DEC} is always decreasing, thus the correction can never recover the original full-scale range, but it can achieve binary-scaled output steps. This results in a slightly smaller ADC full-scale range, while it recovers the ADC linearity. Also, note that the first voltage step effectively determines the scale, and thus, only step two and further need to be compensated (by means of C_{a2} and C_{a3}).

D. Auxiliary DAC Capacitance Calculation

While the auxiliary DAC could be implemented in various ways, it is assumed here that it is also a differential DAC array for the sake of simplicity and good matching to the main DAC.

In order to achieve correct compensation, the capacitance of the auxiliary DAC has to be determined carefully. The calculation of the compensation capacitance is derived subsequently. For the i th switching step, the output voltage shift at each side of the DAC can be expressed as follows:

$$\Delta V_{\text{DAC}+,i} = \frac{C_{S,i}}{C_T} \cdot (V_{\text{REF},i} - 0) + \frac{C_{R+,i}}{C_T} \cdot (V_{\text{REF},i} - V_{\text{REF},i-1})$$

$$= \alpha_{S,i} \cdot V_{\text{REF},i-1} + (\alpha_{R+,i} + \alpha_{S,i}) \cdot \Delta V_{\text{REF},i} \quad (3)$$

$$\Delta V_{\text{DAC}-,i} = \frac{C_{S,i}}{C_T} \cdot (0 - V_{\text{REF},i-1}) + \frac{C_{R-,i}}{C_T} \cdot (V_{\text{REF},i} - V_{\text{REF},i-1})$$

$$= -\alpha_{S,i} \cdot V_{\text{REF},i-1} + \alpha_{R-,i} \cdot \Delta V_{\text{REF},i} \quad (4)$$

where two variables are defined

$$\Delta V_{\text{REF},i} = V_{\text{REF},i} - V_{\text{REF},i-1} \quad (5)$$

$$\alpha_x = C_x / C_T. \quad (6)$$

In (3)–(6), $\Delta V_{\text{DAC}+,i}$ and $\Delta V_{\text{DAC}-,i}$ are the positive and negative voltage shifts of the two DAC outputs, respectively. $C_{S,i}$ is the total switched capacitance and differential switching is maintained as well for the compensation, $V_{\text{REF},i}$ is the reference voltage on C_{DEC} after the i th switching step ($V_{\text{REF},0}$ denotes the original reference voltage), $\Delta V_{\text{REF},i}$ is the reference voltage drop due to the CS by the i th switching, $C_{R+,i}$ and $C_{R-,i}$ are the total capacitance connected to the reference voltage both before and after the i th switching step at each side and α_x denotes the ratio between C_x and C_T . Since the DAC adopts the split-monotonic scheme, the total capacitance connected to V_{REF} in the DAC remains constant as C_T , which can be expressed as

$$C_{S,i} + C_{R+,i} + C_{R-,i} = C_T$$

$$\alpha_{S,i} + \alpha_{R+,i} + \alpha_{R-,i} = 1. \quad (7)$$

In (3) and (4), one parameter, $\Delta V_{\text{REF},i}$ is unknown yet, which can be solved according to the law of charge conservation. The charge absorbed by each side of the DAC can be expressed as

$$Q_{+,i} = C_{S,i} \cdot (V_{\text{REF},i} - \Delta V_{\text{DAC}+,i}) + C_{R+,i} \cdot (\Delta V_{\text{REF},i} - \Delta V_{\text{DAC}+,i}) = C_{S,i} \cdot V_{\text{REF},i-1} + (C_{S,i} + C_{R+,i}) \cdot (\Delta V_{\text{REF},i} - \Delta V_{\text{DAC}+,i}) \quad (8)$$

$$Q_{-,i} = C_{R-,i} \cdot (\Delta V_{\text{REF},i} - \Delta V_{\text{DAC}-,i}). \quad (9)$$

The total transferred charge of the DAC and C_{DEC} equals 0 (assuming C_{DEC} equals γ times C_T)

$$Q_{+,i} + Q_{-,i} + \gamma C_T \cdot \Delta V_{\text{REF},i} = 0. \quad (10)$$

Subsequently, $\Delta V_{\text{REF},i}$ can be expressed as follows by solving (10):

$$\Delta V_{\text{REF},i} = -\frac{2\alpha_{S,i}\alpha_{R-,i}}{\gamma + 2\alpha_{R-,i} - 2\alpha_{R-,i}^2} \cdot V_{\text{REF},i-1}. \quad (11)$$

Equation (11) indicates three conditions where the reference voltage drop equals 0. As expected, when an infinitely large C_{DEC} is used (γ is infinite), the consumed charge can be provided by C_{DEC} without voltage drop. If $\alpha_{S,i}$ or $\alpha_{R-,i}$ is 0, the resulted reference voltage drop is also 0. The former corresponds to no switched capacitance and the latter indicates a special condition where no charge is consumed from the

reference voltage when all the capacitance connected to GND is switched to V_{REF} ($\alpha_{S,i} + \alpha_{R+,i} = 1$) at one side of the DAC. However, the above-mentioned three conditions are not feasible in a practical design and the reference voltage drop is inevitable.

The resulted differential DAC voltage shift can be expressed as

$$\begin{aligned}\Delta V_{DAC,i} &= \Delta V_{DAC+,i} - \Delta V_{DAC-,i} \\ &= 2\alpha_{S,i} V_{REF,i-1} \frac{\gamma + \alpha_{R-,i}}{\gamma + 2\alpha_{R-,i} - 2\alpha_{R-,i}^2}.\end{aligned}\quad (12)$$

In (12), $2\alpha_{S,i} V_{REF,i-1}$ is the desired DAC voltage shift and the coefficient with the divided polynomials indicates the impact of the reference voltage drop due to the CS. Similar as in (11), an infinite γ results in a coefficient equal to 1 and the desirable DAC voltage shift. In general, $\alpha_{S,i}$ is binary scaled and $V_{REF,i-1}$ and $\alpha_{R-,i}$ are code dependent, causing code-dependent DAC voltage shifts. One freedom that can be tuned in (12) is $\alpha_{S,i}$ ($\alpha_{R-,i}$ is determined by $\alpha_{S,i}$ according to (7) since $\alpha_{R+,i}$ is known before each switching). Although the reference drop cannot be avoided, $\Delta V_{DAC,i}$ can still be binary scaled by choosing an appropriate $\alpha_{S,i}$. Moreover, for a symmetric DAC, $\alpha_{S,1}, \alpha_{R+,1}$, and $\alpha_{R-,1}$ are the same despite the MSB code, leading to a code-independent $\Delta V_{DAC,1}$ that can be used as the reference for $\Delta V_{DAC,i}$ tuning during the following switching steps.

For the first DAC switching where no compensation is applied ($\alpha_{S,1} = 0.25, \alpha_{R-,1} = 0.25$, and assuming $V_{REF,0} = 1$), when a C_{DEC} equal to $20 C_T$ is adopted, $\Delta V_{REF,1}$ equal to $-1/163$ and $\Delta V_{DAC,1}$ equal to $81/163$ according to (11) and (12). For simplicity, the calculation of the second switching step below is under the assumption that the first comparison result is 0 (the case of 1 is totally symmetric). If the second comparison result is also 0, by forcing $\Delta V_{DAC,2} = 0.5 \Delta V_{DAC,1}$ according to (12), $\alpha_{S,2}$ can be solved (note that in this case $\alpha_{R+,2}$ is 0.75 so that $\alpha_{R-,2}$ equals $0.25 - \alpha_{S,2}$). Two roots are achieved from the above-mentioned calculation: $\alpha_{S,2} = 0.1256$ and $\alpha_{S,2} = 27.0411$ and the second root is not valid hence left out. The first root is a valid solution: in addition to the nominal switched binary DAC ($0.125 C_T$), a compensation capacitance $C_{A,i} (= \alpha_{A,i} C_T)$ equal to $0.0006 C_T$ leads to a binary differential DAC output voltage shift.

Similarly, if the second comparison result is 1, the above-mentioned calculation can be repeated and it should be noted that $\alpha_{R+,2}$ is 0.25. Two roots are solved: $\alpha_{S,2} = 0.1240$ and $\alpha_{S,2} = 27.3740$ (left out). In this case, the calculated $\alpha_{S,2}$ is smaller than the nominal binary DAC (0.125). In order to achieve decent matching, it is favorable to keep the binary DAC and switch a standalone auxiliary DAC. As a result, the solution 0.1240, in this case, cannot be used either. Previous derivation assumes that the auxiliary DAC is switched in the same way as the binary DAC at each side, while a solution smaller than the nominal switched binary DAC indicates that the auxiliary capacitance $C_{A,i}$ should be switched oppositely with $C_{S,i}$ in order to keep $C_{S,i}$ as $(C_T/2^{i+1})$. Modifying (3)–(10) and repeating the derivation, $\Delta V_{REF,i}$ and

$\Delta V_{DAC,i}$ can be expressed

$$\Delta V_{REF,i} = -\frac{2(\alpha_{S,i} - \alpha_{A,i})(\alpha_{R-,i} + \alpha_{A,i}) + 2\alpha_{A,i}}{\gamma + 2(\alpha_{R-,i} + \alpha_{A,i}) - 2(\alpha_{R-,i} + \alpha_{A,i})^2} \times V_{REF,i-1} \quad (13)$$

$$\Delta V_{DAC,i} = 2(\alpha_{S,i} - \alpha_{A,i}) V_{REF,i-1} \times \frac{\gamma + \alpha_{R-,i} + \alpha_{A,i} + \beta}{\gamma + 2(\alpha_{R-,i} + \alpha_{A,i}) - 2(\alpha_{R-,i} + \alpha_{A,i})^2} \quad (14)$$

where β is expressed

$$\beta = \frac{2(\alpha_{R-,i} + \alpha_{A,i}) - 1}{\alpha_{S,i} - \alpha_{A,i}} \cdot \alpha_{A,i}. \quad (15)$$

Equations (13) and (14) are similar with (11) and (12) and by replacing $\alpha_{A,i}$ with 0, (13) and (14) will be simplified to (11) and (12). Note that in this case, $\alpha_{S,i}$ is fixed and (7) should be rewritten

$$\alpha_{S,i} = 1/2^{(i+1)} \quad (16)$$

$$\alpha_{S,i} + \alpha_{A,i} + \alpha_{R+,i} + \alpha_{R-,i} = 1. \quad (17)$$

Using (14), the case of a second comparison result equal to 1 can be re-calculated and the solved valid solution is $\alpha_{A,2} = 0.00097$, which should be switched oppositely with the binary DAC ($C_{S,2}$). For the following switching steps, the above-mentioned calculation can be repeated: first using (12) to solve $\alpha_{S,i}$. If $\alpha_{S,i}$ is larger than $1/2^{(i+1)}$, the compensation for this case is to switch an auxiliary capacitor equal to $[\alpha_{S,i} - 1/2^{(i+1)}]C_T$ in the same way as the binary capacitor $[1/2^{(i+1)}]C_T$. If $\alpha_{S,i}$ is smaller than $1/2^{(i+1)}$, (14) should be used for the calculation and the compensation is to switch an auxiliary capacitor equal to $\alpha_{A,i}$ oppositely with the binary capacitor.

During the previous calculation, only the differential DAC output voltage shift is considered while the common mode of the DAC output voltage should be constant to avoid causing signal-dependent comparator offset. Taking the sum of (3) and (4), the DAC common mode shift is

$$\Delta V_{DACCM,i} = (\Delta V_{DAC+,i} + \Delta V_{DAC-,i})/2 = \Delta V_{REF,i}/2. \quad (18)$$

From the previous calculation, a C_{DEC} equal to $20 C_T$, $\Delta V_{REF,1}$ is $1/163$ and results in $\Delta V_{DACCM,1}$ of merely 0.6% of the initial reference voltage. As a result, the impact on the comparator offset caused by the compensation scheme is negligible.

While the above-mentioned calculations show the ideal case, in practice the parasitic capacitances must be taken into consideration as well since they also change the energy consumption of the DAC. Two types of parasitic capacitance are most critical (Fig. 3): the parasitic capacitance at the DAC output nodes (C_{PT}) and those at the other plates of the binary DAC array (C_{PB}). C_{PT} should be included in C_T and C_{PB} increases the charge consumption of the DAC when switched from ground to V_{REF} . Consequently, the final values of the capacitors in the auxiliary DAC should be determined after layout extraction. Also, note that the capacitance of the auxiliary DAC contributes to $C_{R+,i}$, $C_{R-,i}$, and C_T . Since its exact value is not known before the calculation, the calculation

Fig. 3. Two types of critical parasitic capacitances.

TABLE IV
AUXILIARY CAPACITANCE FOR THE COMPENSATION
OF THREE SWITCHING STEPS

	Code	1 st step	2 nd step	3 rd step
Binary DAC		240fF	120fF	60fF
Auxiliary DAC	0/1	0		
	00/11		1.8fF	
	01/10		-1.1fF	
	000/111			1.35fF
	001/110			-1.4fF
	010/101			1.2fF
	011/100			0.25fF

gives the first estimate, and iteration is advised taking into account the auxiliary DAC capacitance as well as the layout extracted parasitic.

Table IV shows the numerical values of the auxiliary capacitors based on above-mentioned calculations for the compensation of the first three switching steps in a split-monotonic DAC with a decoupling capacitance of $20 \cdot C_T$ and a C_T of 1 pF, where parasitic capacitance is also taken into account after layout extraction. The capacitors for the binary DAC and the auxiliary DAC are shown. The first switching step requires no compensation as explained earlier. Note that a negative sign in Table IV means that the switching of this auxiliary capacitance is opposite with the related binary capacitor. Table IV shows that the total capacitance of the auxiliary DAC is only 1.4% of the binary DAC for the compensation of the first three switching steps, which introduces little power and chip area overhead. In order to compensate n switching steps, a total of $(2^n - 2)$ different possibilities are needed.

In this paper, different from [7]–[9] (Fig. 2), the V_{REF} drop is still signal dependent after compensation while the DAC switching steps are binary now by tuning the switched capacitance. In this way, no calibration or digital post-correction is needed to generate the final output code.

E. Reference Voltage Recovery During Tracking Phase

The above-mentioned discussion is under the assumption that the voltage on the decoupling capacitance is recovered to V_{REF} at the start of each conversion, and that C_{DEC} is not recharged by the driver during conversion. This can be realized by a discrete-time driver which is only active during the tracking phase. As shown in Fig. 4(a), during the conversion phase, $V_{REF,DEC}$ drops gradually due to the CS. During the tracking phase, C_{DEC} is pre-charged via the PMOS

Fig. 4. (a) $V_{REF,DEC}$ during conversion. (b) Pre-charger with cross detector.

pass gate while a comparator is detecting when $V_{REF,DEC}$ has reached V_{REF} [Fig. 4(b)]. At that moment, the pass gate is switched off and C_{DEC} is disconnected from the power supply. For a symmetric DAC like a split-monotonic DAC, the tracking phase consumes no energy from the reference so that the voltage of C_{DEC} will remain at V_{REF} until the next conversion starts. The discrete-time driver saves power significantly compared to an always-on buffer.

Taking the noise, offset, and delay of the comparator into account, the final pre-charged voltage on C_{DEC} can be expressed as

$$V_{DEC,pre} = V_{REF} + V_{OS} + V_{noise} + I_{ch} \cdot \tau / C_{DEC} \quad (19)$$

where V_{OS} is the offset of the comparator, V_{noise} is the input-referred noise in voltage, I_{ch} is the pre-charging current, and τ is the delay of the comparator. V_{OS} , I_{ch} , and τ , as long as they are constant, only introduce a gain error for the SAR ADC. As for V_{noise} , it will contribute to ADC output noise and should preferably be set well below 1 LSB.

F. Behavioral Simulations

The presented method was verified with MATLAB simulations where a 10-b SAR ADC with a split-monotonic DAC is driven by different C_{DEC} 's and a different number of compensated steps. It is assumed that the reference voltage on C_{DEC} is recovered at the start of each conversion. It can be found from Fig. 5 that it requires a C_{DEC} equal to $2^9 \cdot C_T$ to achieve an ideal signal to noise and distortion ratio (SNDR) of 62 dB and an spurious free dynamic range (SFDR) above 80 dB if the reference voltage drop is not compensated just as discussed in Section I. For smaller C_{DEC} , the SNDR and SFDR will drop, but this can be mitigated by compensating more and more switching steps, at the cost of more complexity in the auxiliary DAC. In practice, a tradeoff must be made between the performance improvement and the complexity of the hardware. The first switching steps consume the most charge and cause the largest V_{REF} drop, hence being the most urgent to be compensated. Moreover, the amount of compensation hardware increases exponentially with the amount of compensated switching steps as discussed in Section II. As shown in Fig. 6, compensating more than four switching steps can barely gain any improvement while the hardware complexity keeps growing. As shown in Fig. 5, to achieve the same SNDR, 3-b compensation can save about $3 \times$ in C_{DEC} when compared to the uncompensated case.

Fig. 5. Behavioral simulation of SNDR/SFDR of a 10-b SAR ADC driven by the discrete-time reference driver with a different number of compensated switching steps at a different ratio of C_{DEC}/C_T .

Fig. 6. SNDR and hardware complexity versus number of compensated steps.

Fig. 7. Behavioral simulations of integral non-linearity and differential non-linearity with a different number of compensation steps.

The impact of the compensation scheme on SAR ADC linearity is further investigated via integral non-linearity (INL)/differential non-linearity (DNL) plots as shown in Fig. 7, where the INL/DNL without and with 3-b/4-b/5-b compensation is depicted. Without compensation, an INL error pattern is observed which gives rise to third-order harmonic

Fig. 8. Behavioral simulations of SNDR/SFDR versus input amplitude.

distortion. The pattern is caused by signal-dependent reference voltage drop which modulates with the signal and thus creates distortion. With compensation, the INL curve is segmented into 2^{NoC} (NoC is the number of compensation bits) groups and shifted toward 0. The INL and DNL are globally reduced (especially around 1/4 and 3/4 full-scale input range, where originally the largest errors occurred), but locally (at the segment transitions) new errors can occur. However, when compensating more bits, the INL and DNL are gradually improving (Fig. 7). The above-mentioned discussion is also seen in the dependence of SNDR/SFDR on input amplitude (Fig. 8). With a small input, the SNDR/SFDR with compensation is worse than those without compensation due to the worse INL at the middle of the input range. When the input amplitude is large, the SNDR/SFDR with compensation improves the performance.

The calculation in Section II-D indicates that with a C_{DEC} equal to $20 C_T$, the first switching step generates a constant $\Delta V_{DAC,1}$ ($=81/163$), which corresponds to a 0.6% full-scale range reduction. While as shown in Fig. 8, the maximum SNDR/SFDR is achieved with an input amplitude of 0.45 for the 3-b compensation, which is caused by the large INL error at the small and large input (Fig. 7). With more compensation bits, the range is approaching full scale (Fig. 8).

Due to the CS, the reference voltage keeps dropping. For a C_{DEC} equal to $20 C_T$ driving a 10-b SAR ADC, the simulated reference voltage drop ranges from 1.2% to 2.0% during each conversion.

As shown previously in Table IV, the required auxiliary capacitors are very small and their capacitances are non-integer multiples of the unit capacitor so that the impact of matching is worth mentioning. Fig. 9 shows the SNDR/SFDR of the SAR ADC driven by an ideal driver as well as the

Fig. 9. Impact of mismatch on SFDR/SNDR (mean value and sigma) for different driving schemes.

Fig. 10. SNDR/SFDR versus the actual $C_{DEC,real}$ (normalized to $20 C_T$).

presented discrete-time driver with 3-b compensation and without compensation. Different capacitor standard deviations (normalized to the unit capacitance) are used to model mismatch and the average and the standard deviation of SNDR/SFDR among a total of 200 runs are monitored. When a small mismatch is only applied to the binary DAC, the performance is limited by the V_{REF} drop and the compensation can still achieve considerable improvement. When the mismatch is large, the improvement is reduced since now the performance is limited by the mismatch. If the mismatch is only applied to the compensation DAC, the performance gain is relatively constant until an extremely large mismatch is applied (30%). Even though the relative mismatch of the compensation DAC is large, the absolute mismatch of the compensation DAC is still very small, so that it has little impact on the performance of the SAR ADC. Thus, the compensation scheme is relatively robust against a mismatch.

Another problem is a mismatch between C_{DEC} and C_T , as the compensation capacitance is calculated based on a certain ratio between those two. Fig. 10 shows the impact of C_{DEC} and C_T mismatch where the compensation capacitance is calculated for a C_{DEC} equal to $20 C_T$ and C_{DEC} has a variation from -90% to 100% . As can be seen, the compensation is not very sensitive to the actual value of C_{DEC} and gives an

Fig. 11. 10-b SAR ADC with three compensated DAC switching steps.

almost constant improvement when C_{DEC} varies from -20% to 50% . When C_{DEC} is larger than $1.5 \times$ the nominal value, the compensation starts to worsen the performance since now the compensation DAC is too far away from the desired value. When C_{DEC} is less than $0.8 \times$ the nominal value, apart from the deviation of the compensation, the smaller C_{DEC} accelerates the performance degradation.

III. CIRCUIT IMPLEMENTATION

A. 10-b SAR ADC With Three Compensated DAC Switching Steps

The 10-b SAR ADC driven by the presented discrete-time reference driver with three compensated DAC switching steps is shown in Fig. 11. The main DAC is segmented into 3-b unary split-monotonic MSBs and 6-b binary monotonic LSBs. In order to avoid missing codes caused by unsettled DAC as in [10], eight LSB redundancy is inserted in the main DAC similar to [12] (so that the weights of the DAC array are 512, ..., 32, 16, 8, 8, 4, 2, 1) and digital reconstruction logic is included to obtain regular 10-b binary output codes. Since eight LSB is very small (8% of full scale), the redundancy will cause a negligible reference voltage drop or signal range loss. The unit capacitance is about 2 fF, leading to a C_T of 1 pF. The main DAC is implemented with lateral metal-metal capacitors as in [13]. The auxiliary DAC is connected in parallel with the main DAC and controlled by the MSB-code $D_{OUT}(10 : 8)$, with a total capacitance of 14.2 fF (1.4% of C_T). A C_{DEC} equal to about $20 \cdot C_T$ is adopted to drive the DAC passively. The pre-charger operates at 1.0-V power supply (V_{DD}) and charges C_{DEC} to V_{REF} of 0.8 V. The rest of the SAR ADC (sample and hold (S&H), comparator, and logic) also operates at 0.8-V V_{DD} .

B. Auxiliary DAC and C_{DEC}

As discussed in Section II, as a tradeoff between performance and circuit complexity, the first three switching steps are compensated in this paper. The auxiliary DAC is illustrated in Fig. 12. There are four capacitor pairs for the second switching step, corresponding to the four possible codes after the first 2-bit decisions. Similarly, there are eight capacitor pairs for the third switching step as there are eight possible codes by then. Due to symmetry, each code and its complement require

Fig. 12. Auxiliary DAC.

Fig. 13. Schematic of the pre-charger.

the same compensation capacitance but switch oppositely. For instance, C_{10} and C_{01} are the compensation capacitors for code “10” and “01”; they have the same value but switch oppositely. The values of these capacitors are calculated after layout extraction since the parasitic capacitance will change the charge consumption and the compensation capacitance. The capacitor values can be found in Table IV. The total compensation capacitance at each side of the DAC is about 14.2 fF, only 1.4% of the total capacitance of the DAC array. In order to get a good matching with the main DAC, the auxiliary DAC is implemented using the same type of capacitors as the main DAC and they are placed close to each other in the layout.

In order to reduce the chip area of C_{DEC} , it is implemented with MOS capacitors. This implies it will not match accurately with the DAC due to different types of capacitance. However, the compensation is not sensitive to the ratio between C_{DEC} and C_T as discussed earlier (Fig. 10).

C. Pre-Charger

The schematic of the pre-charger is shown in Fig. 13. Different from the conceptual diagram in Fig. 4, in order to improve the power supply rejection ratio (PSRR), C_{DEC} is charged by a current source instead of a pass transistor. The current source is realized with a beta multiplier with cascade current mirrors, which also generates the bias for the OPAMP in the crossing detector. The crossing detector is comprised of an OPAMP and several logic gates. The output of the detector controls M_7 to enable and disable the charging of C_{DEC} . Since the pre-charging only happens during the tracking

TABLE V
COMPARISON OF POST-LAYOUT AND BEHAVIORAL SIMULATIONS

	Behavioral simulations		Post-layout simulations	
	With parasitic capacitance			
	Input amplitude = 0.35·full-scale			
	10000-point FFT		128-point FFT	
	SNDR	SFDR	SNDR	SFDR
No compensation	54.5dB	58.7dB	54.2dB	58.0dB
3b compensation	57.6dB	67.1dB	57.5dB	63.8dB
Ideal driver	60.5dB	81.6dB	60.4dB	69.3dB

Fig. 14. Die photograph in 65-nm CMOS.

phase, the sampling clock is used to force M_7 to switch off during conversion. The noise of the comparator is mainly determined by the first stage (M_{0-4}), whose input-referred noise is simulated to be 0.2 mV (0.13 LSB). At different VDD and temperature, V_{OS} , I_{ch} , and τ in (19) will deviate and lead to different $V_{REF,pre}$. At 1-V VDD and room temperature, $V_{REF,pre}$ is 806 mV, which causes a gain error as long as this is constant for all samples. When VDD is changing from 1 to 1.5 V, $V_{REF,pre}$ changes from 806 to 813.2 mV and the VDD dependence of $V_{REF,pre}$ is 14.4 mV/V. From -40°C to 85°C , $V_{REF,pre}$ changes from 804.8 to 807.8 mV and the temperature dependence is 0.024 mV/ $^\circ\text{C}$. At different process corners, $V_{REF,pre}$ ranges from 805.6 to 809.0 mV.

D. Simulation Results

The SAR ADC with extracted information is simulated at circuit level to verify the presented compensation scheme. No thermal noise or mismatch is included in the simulation. Due to the long simulation time, only a 128-point fast Fourier transform is performed and the comparison with the behavioral model (including parasitic capacitance) is listed in Table V with the same input amplitude (0.35 · full scale). The absolute performance of the post-layout simulation deviates from the behavioral model, as the circuit simulation also includes other non-idealities, such as S&H distortion, hence showing slightly different results as the behavioral model (Fig. 8). In general, the post-layout simulations show the same trend as the behavioral model.

IV. MEASUREMENT RESULTS

The prototype is fabricated in 65-nm CMOS technology and occupies a chip area of 0.081 mm² (Fig. 14). The SAR ADC core occupies a chip area of 0.074 mm² and the pre-charger, C_{DEC} , compensation DAC, and the control logic add

Fig. 15. Measured spectrum without and with compensation.

Fig. 16. (a) INL without compensation. (b) DNL without compensation. (c) INL with compensation. (d) DNL with compensation.

only 9.5% more chip area to the SAR ADC, where C_{DEC} is dominant. At 20 MS/s and with a near-Nyquist input tone, the compensation reduces the third-order harmonic by 13.5 dB and the SNDR is improved by 2.4 dB, achieving 56.8-dB SNDR and 72.4-dB SFDR (Fig. 15, both cases with redundancy). The THD is improved from 56.9 to 64.1 dB which can be explained by Figs. 7 and 15. The compensation scheme worsens the INL at the middle of the full-scale input range but greatly improves the INL at 1/4 and 3/4 of the full-scale input range. As a result, the third-order distortion is greatly reduced (SFDR) with increased high-order distortion (Fig. 15). However, the introduced high-order distortion increment is smaller than the third-order reduction and the THD is still improved. Despite the large THD improvement, the SNDR improvement is only 2.4 dB, limited by the SNR (Fig. 15). The linearity improvement can be further observed in INL/DNL plots (Fig. 16). The initial third-order distortion shape in the INL plot is caused by the V_{REF} drop and improved by the compensation. Since only three switching steps are compensated, transitions in the INL curve become visible for the lower uncompensated bits, which correspond to the previous discussion (Fig. 7). Compared with [10], the INL_{max} is greatly improved thanks to the redundancy. The SNDR and SFDR at different input frequencies are also measured with different driving schemes: external power supply, on-chip discrete-time driver without and with compensation as shown in Fig. 17.

Fig. 17. Measured SNDR and SFDR at different input frequencies with DAC driven by the external power supply, C_{DEC} without and with three compensation steps. Fig. 18. SAR ADC power breakdown at the near-Nyquist input with DAC driven by the external power supply, C_{DEC} without and with three compensation steps. Fig. 19. Measured SNDR and SFDR for different interference amplitudes at 4.9 MHz on the power supply when using an external supply directly, or when using the on-chip driver and C_{DEC} without and with compensation.

The compensation improves the performance throughout the entire bandwidth. Since only the first three switching steps are compensated and the other steps still suffer from V_{REF} drop, the SNDR/SFDR of the SAR ADC with compensation at a near-Nyquist input remains 1.3 dB/4.7 dB lower than the case with external power supply. The power consumption and breakdown are shown in Fig. 18. The stand-alone SAR ADC consumes 0.133 mW and the discrete-time reference driver adds 0.014 mW/0.017 mW without/with compensation, respectively, where the added power is dominated by the driver and the dropout loss. The power introduced by the auxiliary DAC and extra compensation logic is only about 2% of the SAR ADC power consumption.

The PSRR of the discrete-time driver is also demonstrated by removing all the external decoupling capacitance and forcing a sinewave interference at the power supply to measure the dynamic performance. Fig. 19 shows the SNDR and SFDR

TABLE VI
PERFORMANCE SUMMARY AND COMPARISON

	This work		[10]	[7]	[8]	[14]	[15]	[16]
Technology (nm)	CMOS 65		CMOS 65	FinFET 16	CMOS 65	CMOS 28	CMOS 28	CMOS 28
VDD (V)	1.0/0.8		1.0/0.8	0.8	1.2	1.2/1.1	1.8/1.0	0.9
Sample rate (MS/s)	20		20	303	80	104	100	100
Resolution (bit)	10		10	12	14	12	15	12
C_T (pF)	1		1	1	4.1	3.6	1.25	0.9
V_{REF} driver	C_{DEC}	C_{DEC}	C_{DEC}	C_{DEC}	C_{DEC}	Buffer	Buffer	Buffer
Compensation	No	Yes	Yes	-	-	-	-	-
Calibration and digital processing required?	No	No	No	Yes	Yes	-	-	-
ADC area (mm ²)	0.074		0.069	0.27	0.55	0.003	0.077	0.0046
V_{REF} driver area (mm ²)	0.006	0.007	0.007	0.043*	N/A	0.004	0.023	0.0028
C_{DEC} included in area?	Yes	Yes	Yes	Yes	Yes	Not mentioned	Not mentioned	No
C_{DEC} (pF)	20	20	20	50	160	-	-	-
Area _{driver} /Area _{ADC} (%)	8.1	9.5	10.8	16	N/A	133.3	29.9	60.9
ADC power (mW)	0.133		0.136	3.6	31.1	0.88	4.8	0.35
V_{REF} driver power (mW)	0.014	0.017	0.015	0.18*	4.0	0.72	3.2	1.56
P_{driver}/P_{ADC} (%)	10.5	12.8	10.1	5	12.9	81.8	66.7	445.7
SFDR (dB)	58.9	72.4	67.8	73.6	88.6	-	-	75.4
SNDR (dB)	54.4	56.8	55.4	63.9	71.3	63	67.1	64.4
FoM (fJ/conv.-step)	17.2	13.3	15.7	9.2	146.3	13.2	43.2	12.5
FoM _{Schreier} (dB)**	162.7	165.0	163.6	169.9	161.9	168.1	165.1	168.6

* The power and chip area do not include the driver used during tracking phase.

** FoM_{Schreier} (dB) = SNDR + 10 * log₁₀(f_{snyq}/2/P).

of the SAR ADC at a near-Nyquist input tone with different amplitudes of interference (at 4.9 MHz) on the power supply for the three driving scenarios as discussed earlier. When driven by an external VDD, the SAR ADC reveals no power regulation ability and the performances degrade rapidly with an increasing interference amplitude. With a realistic interference amplitude of 20-mVpp, the discrete-time reference maintains an SNDR/SFDR drop of less than 1.8 dB/1.9 dB.

Table VI summarizes this paper and compares it with other SAR ADCs with reference driver. The work in Table VI can be categorized into two types: this paper, [7], [8], and [10] utilize C_{DEC} as the driver, while [14]–[16] use an active buffer. Compared with an active buffer, driving with C_{DEC} reveals advantages both in power consumption (P_{driver}/P_{ADC} ranges from 5% to 12.9%) and chip area (Area_{driver}/Area_{ADC} ranges from 8.1% to 16%). Compared with [10], redundancy introduces a little bit more chip area while improving the SFDR/SNDR of the SAR ADC by 4.6 dB/1.4 dB. Compared to [7] and [8] which require calibration and digital post-processing, the presented discrete-time reference realizes the compensation in the analog domain, eliminating the cost for calibration and reducing the complexity. After enabling the compensation, the presented reference driver improves the SNDR/SFDR with little power overhead, enhancing the Walden FoM from 17.2 to 13.3 fJ/conv.-step and the Schreier FoM from 162.7 to 165.0 dB.

V. CONCLUSION

SAR ADCs with a CR capacitive DAC are energy efficient, while the reference driver for the DAC can consume significant power or occupy a large chip area. In this paper, a low-power and area-efficient discrete-time reference is presented. The discrete-time passive driving replaces the continuous-

time buffer to save power. Moreover, the reference drop is compensated to reduce C_{DEC} , hence saving substantial chip area. The compensation for the first three DAC switching steps in this paper reduces C_{DEC} by a factor of 3. The presented compensation is realized in the analog domain, requiring no calibration or digital processing. A similar compensation technique with tweaked capacitor weights can also be adopted in [8] and [9] to get rid of the calibration and digital processing. The presented passive driving scheme combines the advantages of a CR DAC (simple and insensitive to parasitic capacitance) and a CS DAC (only using the reference during tracking). The 10-b 20-MS/s prototype ADC proves that the reference driver can be made with low power (12.8% of the ADC core) and small area (0.007 mm²).

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