Physical-based Analytical Model of Flexible a-IGZO TFTs Accounting for Both Charge Injection and Transport

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Abstract

Here we show a new physical-based analytical model of a-IGZO TFTs. TFTs scaling from L=200 μm to L=15 μm and fabricated on plastic foil are accurately reproduced with a unique set of parameters. The model is used to design a zero-VGS inverter. It is a valuable tool for circuit design and technology characterization.

Introduction

Amorphous Indium-Gallium-Zinc-Oxide thin-film transistors (a-IGZO TFTs) are promising candidates for the next generation of flexible and large area electronics [1-3]. A-IGZO TFTs show high electron mobility (μ~10 cm\textsuperscript{2}/Vs), simple, low-cost and room-temperature fabrication processes, optical transparency, good uniformity, satisfactory device lifetime, and large-area integration even on flexible substrates [1]. The technology development and the design of displays and circuits urgently demand accurate physical-based analytical models. State-of-art physical-based [4-7] and compact [8] models merely describe the channel transport and are only suitable for long channel a-IGZO TFTs. In high mobility and/or short channel a-IGZO TFTs the charge injection severely affects the transistor performance [9,10] and it must be taken into account.

Here we show a new physical-based analytical model of the drain current in a-IGZO TFTs. The model takes into account both the charge transport in the channel and the charge injection at the source contact. It accurately reproduces, with a unique set of parameters, the measurements of high-performance a-IGZO TFTs with channel lengths scaling from L=200 μm to L=15 μm fabricated in our flexible technology. The physical-based analytical model combined with the good stability and uniformity of the fabrication process allow us to disentangle and quantify the channel and contact contributions. The model provides a comprehensive physical picture of the a-IGZO TFTs, and it is a valuable tool for the technology characterization. The model has been eventually implemented in a circuit simulator and it has been used to simulate analog and digital a-IGZO circuits.

a-IGZO TFTs fabrication

Fig. 1 shows cross-section and the top-view optical image of the fabricated a-IGZO TFTs with staggered architecture.
The transistors and circuits fabricated in this large-area flexible technology are shown in Fig. 2, left. The plastic foil is glued to a rigid substrate and detached after the fabrication with no impact on the a-IGZO TFTs characteristics (Fig. 2, right). The fabricated TFTs show stable characteristics also if rolled up to 10⁴ times.

**a-IGZO TFTs uniformity and stability**

The breakdown electric-field of the gate insulator is larger than 6 MV/cm and the leakage current is lower than 10⁻⁸ A/cm² at V_g = 20 V. The measured gate capacitance per unit area is 22 nF/cm². Bias stress stability is very important for stable operation of flexible displays and circuits. A constant gate bias stress of +1 MV/cm (-1 MV/cm) is applied for 10⁴ s. Fig. 3 shows that the maximum ON voltage shift (ΔV_on) is lower than +0.3 V (-0.03 V), and the on-voltage variation across the wafer is below 5% (216 a-IGZO TFTs were measured).

**a-IGZO TFTs analytical model**

In a-IGZO the spherical symmetry of the bonds between the s orbital of metal cations reflects in a reduced density of localized (trap) states. Therefore, in a-IGZO TFTs the carrier concentration, and hence the drain current, depends on the interplay of trapped and free charges. In addition, the low density of trapped charges enables to easily push the Fermi energy level above the conduction band edge and at large V_g the degenerate conduction is reached. The a-IGZO conductivity is described by the multiple trapping and release transport theory combined with the band-percolation [4-7].

The drift-diffusion drain current integral [11,12] accounting for the charge transport in the a-IGZO reads

\[
I_{DS} = \frac{W}{L} \cdot \frac{V_D}{V_S} \int_0^{\Delta V_{ch}} \frac{q \mu_b n_b \phi (\phi', V_{ch})}{\sqrt{\frac{2}{\pi k_B T} + \frac{e_s}{k_B T}}} d\phi dV_{ch}
\]  

where W is the channel width, L is the channel length, V_s and V_d are the source and the drain voltages, respectively, V_ph is the channel potential (viz. pseudo Fermi potential), φ is the electrostatic potential, \( \phi' \) is the surface potential at the insulator-semiconductor interface, \( n_b \) is the free charge carrier concentration, \( \mu_b = \mu_0 \exp \left( \frac{\phi - \phi_0}{k_B T} \right) \) is the band mobility \( \mu_0 \) modulated by the percolation term [7], \( F_p \) and \( F_{pb} \) are the electric fields calculated accounting for the trapped and the free charges, respectively. The electric field depends on the charge concentration and it is expressed as

\[
F_{So} = \frac{2}{\sqrt{2}} \exp \left( \frac{\phi - \phi_0}{k_B T} \right)
\]

\[
F_{t} = \frac{2}{\sqrt{2}} \exp \left( \frac{\phi - \phi_0}{k_B T} \right)
\]

\[
I_{DS} = \frac{L}{W} \cdot \frac{I_{DS}^0 \times I_{DS}^{10} \times I_{DS}^{+10}}{I_{DS}^{0+10} + I_{DS}^{0+10}}
\]  

where \( I_{DS}^{0+10} \) is the drain current given by Eq. (1) with \( F_{xb} = 0 \) and \( I_{DS}^{0+10} \) is the drain current given by Eq. (1) with \( F_{xt} = 0 \). Solving Eq. (5) and accounting for the leakage current flowing from the source to the drain contact when the transistor is in the off-state, the drain current results

\[
I_{DS} = \frac{W}{L} \cdot \frac{I_{D}^{0+10}}{L_{OFF}} + \frac{V_{DS}}{R_{OFF}}
\]
In Fig. 4 and Fig. 5 the channel model [Eq. (6)] is validated on the transfer and output characteristics of long channel (L=200 μm) a-IGZO TFTs, respectively. In both cases the model shows negligible error in a wide range of biasing conditions. Fig. 6 (symbols) shows the L/W normalized output characteristics varying the a-IGZO TFTs channel length. The normalized current is lower for short channel devices and this can be explained by the limited charge injection at the source contact [9,10]. The stability and uniformity of our a-IGZO TFTs together with the analytical channel model allowed us to accurately calculate the contact characteristics. The $I_{ch}$ of the shortest channel (L=15 μm) a-IGZO TFT is obtained by splitting the channel into a small contact region [14], where there is a voltage drop $V_C$, and the main channel, where the voltage drop is $V_{DS} - V_C$ (Fig. 6, inset). Fig. 7 (symbols) shows the $I_{ch}$ for several gate voltages. We model the contact as a reverse biased Schottky-gated diode as proposed for staggered organic TFTs [15,16]. The contact model reads:

$$I_c = W I_0 \exp \left( \frac{qV_C}{n V_0} \times \left[ \exp \left( \frac{qV_C}{n V_0 \eta kT} \right) - 1 \right] \right)$$

$$I_0 = I_{00} \times \left\{ \log \left[ 1 + \exp \left( \frac{V_{G}-V_{fb}}{V_{00}} \right) \right] \right\}^\gamma$$

where $V_0$ accounts for the Schottky barrier lowering effect, is the quality factor, and $I_{00}$ is the reverse current prefactor. $V_{00} = 1V$ and it is introduced to keep the dimensionality of the pre-factor $I_{00}$, and $\gamma$ is a fitting parameter.

In Fig. 6 (full lines) the model (viz. channel and contact model), enables to describe the drain current of a-IGZO TFTs with L ranging from 15 μm to 200 μm. It is worth to note that the model describes a-IGZO TFTs with different channel lengths with the single set of parameters reported in Tab. 1. The model [Eqs. (6), (12)] has been implemented in a circuit simulator and used to design a unipolar zero-VGS inverter, that is the basic building block of any analogue and digital circuits.
The comparison between the designed and measured inverter transfer characteristic is shown in Fig. 8. A good agreement between the simulation and the measurements is obtained thanks to the model accuracy and the process stability.

**Conclusion**

A physical-based analytical model of the drain current and charge concentrations in a-IGZO TFTs is proposed. The model is validated with the measurements of a-IGZO TFTs fabricated on flexible plastic substrate. We show that the a-IGZO TFTs scaling from \( L=200 \, \mu \text{m} \) to \( L=15 \, \mu \text{m} \) can be accurately reproduced with a single set of parameters. Both the charge transport in the channel and the charge injection at the source contact must be taken into account when \( L \leq 20 \, \mu \text{m} \). The model is implemented in a circuit simulator and a zero-\( V_{GS} \) unipolar inverter is designed. The agreement between the simulations and measurements show that the model can be used for the design of flexible displays and circuits.

**References:**


