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Modeling of Distributed Energy Resources for Simulating Fault-Initiated Islanding of Microgrids

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Abstract—To increase the reliability of distribution networks, novel network operation concepts including fault-initiated islanding of microgrids may be integrated in the future. During fault-initiated islanding a sequence of fault, islanding and control-mode switching transients take place. In the literature, simplified distributed energy resource models are often used for simulations, however stability assessment for this complicated switching transient requires dedicated models. Different distributed energy resource models are developed in this paper and compared to a reference model to analyze the impact of switching harmonics, DC-link dynamics and PLL dynamics on fault-initiated islanding simulations. Additionally, the impact of several distributed energy resource and load parameters on the modeling accuracy is determined. The results indicate that the switching harmonics and DC-link dynamics can be neglected in some cases, while the PLL dynamics should be modeled when PLLs have different bandwidth or structure.

Index Terms—Distributed energy resources, dynamic models, microgrids, islanding.

I. INTRODUCTION

The integration of distributed energy resources (DERs) and automated switchgear in distribution networks enables network operation strategies which form microgrids. Microgrids are capable of switching between grid-connected and islanded operation which makes novel network operation concepts possible. Concepts described by [1]–[3] can island part of the network to maximize the supplied load after a fault has occurred. During this fault-initiated islanding (FII) a sequence of fault, islanding and control-mode switching transients take place. During the control-mode switching transient the DERs inverters switch from grid-feeding to grid-supporting control mode.

To analyze the stability during and after these transients, time-domain simulations can be performed using large-signal models of DERs. Different DERs models have been described in the existing literature. Differences can be found in the modeling of switching harmonics and DC-link dynamics. Neglecting switching harmonics can significantly decrease simulation time since switching components cause the models

to become non-linear and time-varying [4]. The two main alternative modeling methodologies proposed in the literature are: average value modeling (AVM) and dynamic phasor modeling (DPM). An AVM only considers the fundamental frequency, while a DPM can also consider the switching harmonics [5].

Neglecting DC-link dynamics decreases the number of states in the model, which also decreases the computation time. A stiff DC-link voltage is used by [6], a constant power is assumed from the primary DER source by [7] and the primary source is modeled in more detail by [8].

It is often assumed that a stiff external grid is available which enables the phase-locked loop (PLL) to accurately determine the reference angle for the grid-feeding controllers of the DERs. However, between the islanding and control-mode switching transients the DERs are operating in grid-feeding mode in an islanded network. As described by [9] for weak external grids, the PLL bandwidth impacts the phase angle determined by the PLL.

Literature on FII is limited, and there is no paper which analyzes the impact of modeling the inverter switching harmonics, DC-link dynamics and PLL dynamics on the accuracy of FII simulations of microgrids. Models without switching harmonics, DC-link dynamics and PLL dynamics may neglect important phenomena. However, highly detailed models may unnecessarily increase the computation time and require more detailed modeling parameters.

In this paper FII simulations of a microgrid with two DERs are performed using different DERs models. To determine the accuracy of the models, the simulation results are compared to a reference model.

The contributions of this paper are:

- 1) To analyze the impact of modeling switching harmonics, DC-link dynamics and PLL dynamics on the accuracy of FII simulations.
- 2) To determine when switching harmonics, DC-link dynamics and PLL dynamics can be neglected during FII simulations.

In the next section the network, models and model evaluation are described, in section III the simulation results and

TABLE I
SYSTEM PARAMETERS

Parameter	Value
BESS voltage (E_m)	48V
BESS resistance (R_0)	0.1152 Ω
DC-link switching frequency	10kHz
DC-link inductance (L_b)	21 μ H
DC-link capacitance (C_{dc})	1mF
Inverter switching frequency (f_{sw})	16kHz
Filter input inductance (L_1)	4.3mH
Filter output inductance (L_2)	930 μ H
Filter damping resistance (R_d)	2 Ω
Filter capacitance (C_1)	8.8 μ F
Cable resistance	0.206 Ω /km
Cable inductance	0.17mH/km
Cable capacitance	281nF/km
Cable 1;2;3 length	0.5;0.2;0.5km
Load resistance	15.075 Ω
Load inductance	15.8mH
External grid voltage	325sin(ωt)V
External grid resistance	0.0163 Ω
External grid inductance	0.519 μ H
Inverter current controller gain ($P_1; I_1$)	0.1439;411.0
Inverter voltage controller gain ($P_2; I_2$)	0.0893;537.4
Inverter 1 droop coefficients ($k_{P1}; k_{Q1}$)	$\frac{-0.325}{5000}; \frac{0.02\pi}{5000}$
Inverter 2 droop coefficients ($k_{P2}; k_{Q2}$)	$\frac{-3.25}{5000}; \frac{0.2\pi}{5000}$
Inverter 1;2 active power references ($P_1^*; P_2^*$)	3;2kW
Inverter 1;2 reactive power reference ($Q_1^*; Q_2^*$)	0;0Var
PLL PI gain 10Hz bandwidth ($P_3; I_3$)	43.27;21.64
PLL PI gain 20Hz bandwidth ($P_3; I_3$)	86.55;43.27
PLL PI gain 50Hz bandwidth ($P_3; I_3$)	216.35;108.2
DC-link voltage controller gain ($P_4; I_4$)	0.1;10

modeling errors are presented and discussed. Finally, in section IV conclusions are presented based on the simulation results.

II. METHODOLOGY

This paper considers the microgrid shown in Fig. 1 consisting of two DERs which are connected to a three-phase load and an external grid via three cables. The DERs consist of a battery energy storage system (BESS), a DC-link, a three-phase inverter and a LCL output filter (parameters in table I). The inverters are controlled in the dq reference frame in both grid-feeding and grid-supporting operation. A reference model is developed which considers the switching harmonics, PLL dynamics and DC-link dynamics. Reduced models are developed and the simulation results are compared to the reference model to determine accuracy of each model.

A. Reference model

Detailed overviews of the DER hardware, controllers and PLL are shown in Fig. 2, 3, 4 and 5.

1) *BESS, DC-link and inverter*: The DC-link consists of a Rint BESS model in series with a buck-boost converter. The buck-boost converter is controlled with unipolar PWM control signal $S_{dc} \in [0, 1]$ to maintain a constant DC-link voltage (V_{Cdc}). The battery output current and DC-link voltage are described by equation 1.

$$\dot{I}_{BESS} = \frac{1}{L_b} [E_m - I_{BESS}R_0 - V_u] \quad (1a)$$

$$\dot{V}_{Cdc} = \frac{1}{C_{dc}} [I_u - I_{dc}] \quad (1b)$$

Fig. 1. Network overview including DER 1 and DER 2.

Fig. 2. Overview of the battery energy storage system, DC-link and inverter.

$$V_u = S_{dc}V_{Cdc} \quad (1c)$$

$$I_u = S_{dc}I_{BESS} \quad (1d)$$

The three-phase inverter consists of six switches and an LCL output filter with damping resistance. The inverter is controlled with bipolar PWM control signals $S_a, S_b, S_c \in [-1, 1]$ to control I_{L1} , V_o and the output power. The currents and voltages can be described for each phase $i \in [a, b, c]$ by equation 2.

$$\dot{I}_{L1,i} = \frac{1}{L_{1,i}} \left[\frac{V_{Cdc}}{2} S_i - (I_{L1,i} - I_{L2,i}) R_{d,i} - V_{C1,i} - V_n \right] \quad (2a)$$

$$\dot{I}_{L2,i} = \frac{1}{L_{2,i}} [V_{C1,i} + (I_{L1,i} - I_{L2,i}) R_{d,i} - V_{o,i}] \quad (2b)$$

$$\dot{V}_{C1,i} = \frac{1}{C_{1,i}} [I_{L1,i} - I_{L2,i}] \quad (2c)$$

$$\dot{V}_n = \frac{V_{Cdc}}{6} [S_a + S_b + S_c] \quad (2d)$$

$$I_{dc} = I_{L1,a} S_a + I_{L1,b} S_b + I_{L1,c} S_c \quad (2e)$$

2) *Inverter and DC-link controllers*: The inverter controller is shown in Fig 3. The switching of the inverter is controlled by PWM signals S_a, S_b, S_c which are generated from three reference signals (m_a, m_b, m_c). The reference signals are generated by PI controllers in the dq0 reference frame as described by [10]. The network consists of low voltage cables which leads to a relatively high R/X ratio. A P-V/Q-f droop

Fig. 3. Overview of the inverter controller. The switches allow switching between grid-feeding and grid-supporting mode.

Fig. 4. Overview of the DC-link controller.

control scheme is used which has superior power sharing performance compared to conventional droop control in this case [11]. The PI controller gains and droop coefficients are given in table I. The reference signals in the dq reference frame are described by equation 3.

$$m_d = P_1(I_d^* - I_{L1,d}) + P_1 I_1 \int (I_d^* - I_{L1,d}) dt \quad (3a)$$

$$m_q = P_1(I_q^* - I_{L1,q}) + P_1 I_1 \int (I_q^* - I_{L1,q}) dt \quad (3b)$$

To protect the inverter, the voltage and current references V_d^* , V_q^* , I_d^* and I_q^* are limited in the inverter controller. In this paper the voltage references are limited to 390V and the current references are limited to 12.3A.

The DC-link controller consist of a PI controller which regulates the duty cycle of the buck-boost converter according to the DC-link voltage V_{Cdc} and reference V_{dc}^* as shown in Fig. 4. The PI controller gain is given in table I.

3) *Phase-locked loop*: This paper considers a synchronous reference frame PLL as shown in Fig. 5. Different PLL dynamics are analyzed by varying the PLL bandwidth. The closed loop transfer function of the PLL is given by equation 4.

$$H_{PLL}(s) = \frac{P_3 s + P_3 I_3}{s^2 + P_3 s + P_3 I_3} \quad (4)$$

The propotional and integral gains for a bandwidth of 10Hz and 20Hz with a damping factor of $\frac{1}{\sqrt{2}}$ are given in table I.

B. Model reductions

1) *Switching harmonics AVM*: In AVMs the discontinuous PWM switching signals S_i are replaced by the continuous reference signals m_i . To develop the AVM, equations 2a, 2d and 2e are replaced by equations 5a, 5b and 5c.

$$\dot{I}_{L1,i} = \frac{1}{L_{1,i}} \left[\frac{V_{Cdc}}{2} m_i - (I_{L1,i} - I_{L2,i}) R_{d,i} - V_{C1,i} - V_n \right] \quad (5a)$$

$$\dot{V}_n = \frac{V_{Cdc}}{6} [m_a + m_b + m_c] \quad (5b)$$

Fig. 5. Overview of the phase-locked loop.

$$I_{dc} = \frac{1}{2} [I_{L1,a} m_a + I_{L1,b} m_b + I_{L1,c} m_c] \quad (5c)$$

2) *Switching harmonics DPM*: In DPMs each signal is represented by a fourier series. A DPM therefore consists of multiple similar models, each for a different frequency of interest. This allows a time-invariant model to be created which includes (part of) the switching harmonics. A time-invariant model can be simulated with a larger time-step, however the inclusion of more harmonics increases the number of states which increases the computation time. To develop the DPM, all states are divided into real and imaginary parts to represent phasors using the property in equation 6, where $\langle x \rangle_k$ indicates the average value of variable x for harmonic k of the fundamental frequency $\bar{\omega}$ [5].

$$\frac{d}{dt} \langle x \rangle_k(t) = \left\langle \frac{d}{dt} x \right\rangle_k(t) - j k \bar{\omega} \langle x \rangle_k(t) \quad (6)$$

The number of states of a DPM is equal to $2ho + d$ where h is the number of included harmonics, o is the number of AC states and d is the number of DC states in the switched model. The DPM developed in this paper includes: the fundamental frequency, second-order sidebands of the switching frequency and first-order sidebands of $2x$ the switching frequency, which are the most significant harmonics [12].

As with the AVM, the DPM is controlled by reference signals m_i in the fundamental frequency. The control signals for higher harmonics are described by equation 7 [12]. Where $\bar{\omega}$ and $\hat{\omega}$ are the fundamental and switching frequency. The frequency described by the model is $\omega k = n\hat{\omega} + s\bar{\omega}$. J_s is the Bessel function of the first kind of order s .

$$m_{i,n,s}^R = \frac{2}{n\pi} \sin\left(\frac{\pi(n+s)}{2}\right) J_s(y_n) \cos(n\hat{\phi} + s\bar{\phi}) \quad (7a)$$

$$m_{i,n,s}^I = \frac{-2}{n\pi} \sin\left(\frac{\pi(n+s)}{2}\right) J_s(y_n) \sin(n\hat{\phi} + s\bar{\phi}) \quad (7b)$$

$$y_n = \frac{n\pi}{2} |m_i| \quad (7c)$$

$$\bar{\phi} = \angle m_i \quad (7d)$$

3) *DC-side dynamics*: When the DC-side dynamics are not modeled, a stiff DC-link voltage is assumed. In this case, equation 1 is neglected and variable V_{Cdc} is equal to the nominal DC-link voltage of 800V.

4) *Phase-locked loop bandwidth*: In the reference model the bandwidth of PLL 1 and PLL 2 are 10Hz and 20Hz respectively. In the reduced PLL model the bandwidth of both PLLs is considered to be 10Hz.

C. Model evaluation

To determine the accuracy of the reduced models, the simulation results are compared to the reference model. The instantaneous, average and peak time-domain errors are determined by equation 8, where x_1 is a state of the reference model and x_2 is a state of a reduced model. The average and peak errors are determined for three different periods: fault (e_1), islanding with controllers grid-feeding mode (e_2) and islanding with controllers in grid-supporting mode (e_3). Each period starts at $T_{s,l}$ and ends at $T_{e,l}$ for $l \in [1, 2, 3]$.

$$e(t) = |x_1(t) - x_2(t)| \quad (8a)$$

$$e_{al} = \frac{1}{T_{e,l} - T_{s,l}} \int_{t=T_{s,l}}^{T_{e,l}} e(t) dt \quad (8b)$$

$$e_{pl} = \max e(t) \quad \forall T_{s,l} \leq t \leq T_{e,l} \quad (8c)$$

III. RESULTS

The simulations are performed using Simulink. The fault, islanding and control-mode switching transients take place at times $T_{s,1} = 55\text{ms}$, $T_{s,2} = T_{e,1} = 155\text{ms}$ and $T_{s,3} = T_{e,2} = 255\text{ms}$ respectively. The total simulation time is $T_{e,3} = 500\text{ms}$. The fault is located at the terminals of the external grid. The AVM and DPM are simulated with different damping resistances to analyze the impact of the severity of switching harmonics. The model without DC-link dynamics is compared to a reference model with C_{dc} of 0.1mF, 1mF and 10mF to analyze the impact of the DC capacitance size. The model is also simulated with a BESS voltage of 48V and 43V to analyze the impact of the primary source output power. The model with equal PLL bandwidths is compared to the reference model where PLL 1 has a bandwidth of 10Hz, and PLL 2 has bandwidths of 20Hz and 50Hz to analyze the impact of different PLL bandwidths. The model is evaluated with a load power factor (PF) of 0.95 and 0.80 (inductive) to analyze the impact of the load. The errors of each model are given in table II.

A. Switching harmonics

The waveforms of the AVM closely resemble those of the reference model as shown in Fig. 6. A difference was found in the value of the DC-link voltage during grid-supporting operation, which leads to a temporary output current difference with a peak of 1.72A. When the damping resistance is reduced to $R_d = 0\Omega$ the modeling error of the AVM during grid-feeding islanding increases as shown in table II.

The DPM shows relatively large modeling errors during the fault and grid-feeding islanding periods as shown in table II. Fig. 7 shows that this is caused by the inability of the DPM to deviate from the fundamental frequency. During the fault period, the magnitude of the output current is similar to the reference model while the phase angle is different. During the grid-feeding islanding period the magnitude and frequency of the output current differ significantly. Removing the damping resistance from the LCL filter does not significantly impact the modeling errors of the DPM.

Fig. 6. DER 1 output current and DC-link voltage of reference model and AVM during transients. $R_d = 2\Omega$.

Fig. 7. DER 1 output current and DC-link voltage of reference model and DPM during transients. $R_d = 2\Omega$.

B. DC-Link dynamics

When the DC-link dynamics are neglected, the behavior during grid-feeding operation is accurately represented since the DC-link voltage remains around nominal voltage as shown in Fig. 8. However, during grid-feeding operation the output power of DER 1 becomes larger than the output power of the BESS which decreases the DC-link voltage. When the DC-link voltage drops to around 2x the nominal (peak) grid voltage, the output current of the reference model decreases. This phenomena is not visible when the DC-link voltage is neglected.

Reducing the capacitance C_{dc} to 0.1mF or the voltage E_m to 43V causes voltage V_{dc} to decrease faster, leading to larger modeling errors during grid-supporting operation. Increasing capacitance C_{dc} to 10mF increases the amount of energy stored in the DC-link, causing the DC-link voltage to decrease slower during grid-supporting operation. In this case, voltage V_{dc} remains above 2x the nominal (peak) grid voltage and the modeling error is small.

C. Phase-locked loop dynamics

When the bandwidth of PLL 1 and PLL 2 are 10Hz and 20Hz respectively, the phase angle determined by the PLLs during faults and grid-feeding islanding is different. This

TABLE II
AVERAGE AND PEAK MODELING ERRORS OF OUTPUT CURRENT AND DC-LINK VOLTAGE OVER THE DIFFERENT PERIODS.

Model reduction	Properties	I_{L1} (A)						V_{Cdc} (V)					
		e_{a1}	e_{a2}	e_{a3}	e_{p1}	e_{p2}	e_{p3}	e_{a1}	e_{a2}	e_{a3}	e_{p1}	e_{p2}	e_{p3}
AVM	$R_d=2\Omega$	0.09	0.11	0.34	0.24	0.99	1.72	0.03	0.09	9.33	0.15	0.60	24.4
	$R_d=0\Omega$	0.04	0.49	0.34	0.69	2.41	1.73	0.03	0.12	9.24	0.72	0.90	25.1
DPM	$R_d=2\Omega$	9.42	5.91	0.24	16.4	9.87	5.47	0.04	0.30	5.76	0.69	0.69	17.28
	$R_d=0\Omega$	9.42	5.93	0.26	16.4	10.7	6.76	0.04	0.30	5.19	1.05	1.11	16.7
No DC-link dynamics	$C_{dc}=0.1\text{mF}, E_m=48\text{V}$	0.03	0.36	0.97	0.39	1.27	1.67	-	-	-	-	-	-
	$C_{dc}=1\text{mF}, E_m=48\text{V}$	0.03	0.15	0.47	0.31	1.22	1.62	-	-	-	-	-	-
	$C_{dc}=10\text{mF}, E_m=48\text{V}$	0.04	0.17	0.03	0.23	1.64	0.10	-	-	-	-	-	-
	$C_{dc}=1\text{mF}, E_m=43\text{V}$	0.04	0.16	1.39	0.26	0.95	3.49	-	-	-	-	-	-
Equal PLL bandwidth	PF=0.95, BW=20Hz	7.37	4.10	0.11	16.4	9.70	10.7	0.01	0.01	1.74	0.18	0.15	2.82
	PF=0.8, BW=20Hz	7.56	2.14	0.15	16.4	8.81	16.2	0.06	0.01	0.03	0.06	0.12	0.90
	PF=0.95, BW=50Hz	0.76	4.34	0.151	2.22	15.4	10.6	0.01	3.63	1.50	0.24	23.94	3.27

Fig. 8. DER 1 output current of reference model and model without DC-link dynamics during transients. $C_{dc}=1\text{mF}, E_m=48\text{V}$.

Fig. 10. DER 1 and DER 2 output current of reference model with PLL bandwidths 10Hz and 20Hz, and model with PLL bandwidths 10Hz and 10Hz during transients. PF=0.95.

Fig. 9. DER 1 output current of reference model and model without DC-link dynamics during transients. $C_{dc}=10\text{mF}, E_m=48\text{V}$.

Fig. 11. DER 1 and DER 2 output current of reference model with PLL bandwidths 10Hz and 50Hz, and model with PLL bandwidths 10Hz and 10Hz during transients. PF=0.95.

causes the output current waveform of both DERs 1 and DERs 2 to be shifted in phase, which is not present when the PLL dynamics of all DERs are equal as shown in Fig. 10.

When the PLL bandwidths are 10Hz and 50Hz, the frequency of the output current of DER 2 increases significantly during the fault period while the magnitude of the current decreases as shown in Fig. 11. During the grid-feeding islanding period a large circulating current is present while the DERs are synchronized.

D. Discussion

The switching harmonics have a minor impact on the dynamics during FII transients. The AVM can therefore be used with acceptable accuracy, especially when the switching harmonics are reasonably damped.

The DPM used in this paper is not valid during the fault and islanding periods due to the constant fundamental frequency $\bar{\omega}$ in equation 6. A DPM of a network containing synchronous

generators which can handle a variable fundamental frequency has been proposed by [13] which could solve this problem in future research.

In grid-feeding operation the input and output power is controlled to be equal, however during grid-supporting operation the DERs output power (P_{out}) can become larger than the power generated by the BESS (P_{BESS}). This causes a drop in DC-link voltage which impacts the output current as described in equation 2 and therefore the maximum output power of DERs. This effect is not visible when DC-side dynamics are not modeled, which may cause instabilities to be ignored. The DC-link dynamics may be neglected without large errors if equation 9 is valid for all t where $V_{dc,min}$ is around 2x the peak network voltage. This constraint is especially important when intermittent primary sources are present instead of BESS.

$$\int_{t=0}^{T_{e,3}} P_{out}(t) \leq \int_{t=0}^{T_{e,3}} P_{BESS}(t) + \frac{1}{2} C_{dc} (V_{dc,nom} - V_{dc,min})^2 \quad (9)$$

During steady-state operation, there is a stiff voltage available at the terminals of the inverter which allows for accurate tracking of the phase angle by the PLL. During faults and islanding in grid-feeding mode, the PLL phase angle drifts depending on the PLL dynamics and power factor of the load. When there are DERs with a different PLL dynamics in the network, the DERs have a different voltage phase angle which leads to circulating current. This changes the output current of the inverters, which is not visible when the PLLs are modeled with equal dynamics. DERs may have different dynamics through different PLL bandwidth (typically between 2Hz and 400Hz [7], [14]) or different PLL types [15].

Although this paper analyzed multiple models under different conditions, the results have the following limitations which will be treated by the researchers in future research.

The dynamics of the islanding detection systems are not considered in this paper. Islanding detection time depends on the used methodology [16] and could significantly impact the simulations results when DERs switch from grid-feeding to grid-supporting operation on different moments.

Switching-function based models which are comparable to the reference model used in this paper have been widely used as reference by literature e.g. [5], [12]. However these models have not yet been validated for FII simulations.

A series RL load model is used in this paper. The impact of voltage- and frequency-dependent behavior should be analyzed in future research with more detailed load models.

Only balanced situations and three-phase DERs have been analyzed in this paper.

IV. CONCLUSION

The impact of switching harmonics, DC-link dynamics and PLL dynamics model reductions on the average and peak errors during FII simulations has been determined under different conditions. The results indicate that AVMs are most suitable for FII simulations when the harmonics are reasonably damped. The DC-link dynamics can be neglected when the

DER output power is smaller than the sum of the power generated by the primary source and the energy which can be delivered by the DC-link capacitance. The PLL dynamics should be modeled for each DER individually as opposed to using an equal PLL model for all DERs in the network. The following aspects still require future research: experimental model validation, the impact of islanding detection systems, unbalanced networks and more detailed load models.

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