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Fast Voltage Stabilization Control of Split DC Bus Midpoint in 3P4W Shunt APFs

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Keywords

«Interleaved converters», «Active filter», «Three-phase system», «Power quality»

Abstract

A midpoint voltage balancer (MVB) based on dual-switching-leg is proposed in this paper. The MVB provides fast voltage stabilization of the midpoint in three-phase four-wire (3P4W) shunt active power filters (APFs). Interleaved control is adopted in the MVB to prevent high-frequency current circulation in split capacitors, and to facilitate an accurate neutral current tracking. All switches of the MVB operate in zero-voltage switching (ZVS) mode when the neutral current is smaller than the nominal phase current of the APF. MATLAB simulation is carried out to verify the effectiveness of the MVB. A 20 kVA prototype has been built, and experimental results show that the voltage ripple of the midpoint is maintained within 1.5% of the total dc bus voltage even under severe neutral current transient.

Introduction

Voltage quality issues in power distribution networks have received comprehensive attention in literature [1-5], among which voltage imbalance has become an increasing threat to normal operation of electric equipment in the power distribution network. Voltage imbalance causes transformer overloading and overheating [6], power loss in neutral wires, efficiency degradation of induction motors, and reduced lifetime of motor drives [7]. Voltage imbalance is mainly introduced by unmatched impedance on transformer banks, generation faults, and more prominently, the unequal distribution of single-phase power loads and single-phase power generators [8], such as electric vehicles and roof-top photovoltaic inverters.

Shunt APFs have been widely employed to deal with the voltage imbalance issue by actively ejecting or sinking currents to power distribution network [5, 6]. Since 3P4W configuration is commonly adopted in residential power distribution applications, the same configuration of the shunt APF is required to compensate zero-sequence current component in the neutral wire. Therefore, a dc bus midpoint of the shunt APF must be provided to create a path for neutral current flow. In this paper, the dc bus midpoint is also called the neutral point.

Existing solutions for neutral point creation in 3P4W shunt APFs can be classified into three categories: conventional split dc bus [5, 9, 10], fourth-switching-leg [11, 12], and actively controlled split bus

(ACSB) [13-16]. As it shown in Fig. 1, Fig. 2, and Fig. 3, the neutral point is either provided by the midpoint of split capacitors or the midpoint of a switching leg. High neutral current is expected under unsymmetrical load condition, since one of the functions of the 3P4W shunt APF is voltage imbalance correction.

Fig. 1: Neutral point configuration of 3P4W shunt APF: conventional split dc bus.

Fig. 2: Neutral point configuration of 3P4W shunt APF: fourth-switching-leg.

Fig. 3: Neutral point configuration of 3P4W shunt APF: actively controlled split bus (ACSB).

In case of solution one (see Fig. 1), two bulky capacitors C_{N1} and C_{N2} , normally electrolytic, are employed to form a neutral point, where the neutral wire is connected. The neutral current keeps charging one of the split capacitors while discharging the other for a certain period. On the one hand, this solution is easy to implement, on the other hand, it associates problem of voltage imbalance across two split capacitors. Several practical factors, including unequal capacitance, asymmetrical charging of the capacitors, and asymmetrical circuit configuration could cause voltage mismatching problem between two split capacitors [13]. In addition, a major voltage mismatching would happen, triggering over-voltage protection or resulting in system failure if the neutral current contains a dc component. Since the midpoint voltage in conventional split dc bus is not actively controlled, high voltage variation of the midpoint is highly probable under unbalanced loads. As a result, the high midpoint voltage variation affects current tracking precision of shunt APFs, thus degrading their voltage imbalance compensation performance.

The fourth-switching-leg approach was proposed in [12], adopting an extra switching leg on top of the conventional three-phase inverter, as shown in Fig. 2. In the fourth-switching-leg approach, bulky electrolytic capacitors have been eliminated, which contributes to components cost reduction and power density improvement. However, the control of the fourth-switching-leg and the three-phase inverter is not decoupled, which increases the development effort. In most low-voltage distribution networks, the neutral wire is connected to the protective earth. For 3P4W shunt APFs adopting the fourth-switching-leg, the voltage potential of the midpoint is not well defined, posing high-frequency voltage ripple over parasitic capacitors (between dc bus and ground). This voltage ripple causes common-mode currents, being a source of EMC problems [17].

An alternative approach (ACSB) is the combination of the conventional split dc bus and the fourth-switching-leg [16], as shown in Fig. 3. The control of the fourth switching leg in ACSB is decoupled from the three-phase inverter. Therefore, 3P4W shunt APFs adopting this approach are equivalent to three independent half bridge converters. Comparison of conventional split dc bus and ACSB is given in [18], where the ACSB approach can handle 137% more asymmetric current within the defined safe operating limits. However, experimental verification of the ACSB has not been shown. Note that, the maximum neutral current is twice of the nominal phase current under the worst scenario of asymmetric loads. Therefore, a single-switching-leg design in the ACSB is not sufficient. Furthermore, the high frequency (HF) charging/discharging current flowing into the neutral point could cause overheating to the split capacitors, thus degrading the lifespan of these capacitors.

This paper proposes a dual-switching-leg based MVB for 3P4W shunt APFs, as shown in Fig. 4. It provides fast voltage stabilization of the dc bus midpoint. The current rating of the neutral wire is more than doubled compared to that in the ACSB. Interleaved control is employed to minimize the HF current ripple introduced to the neutral point. The neutral inductors in the MVB are designed in a way to enable ZVS across all IGBT switches, when the neutral current is smaller than the nominal phase current. Finally, MATLAB simulation and converter prototyping have been carried out to verify the proposed MVB.

Proposed midpoint voltage balancer

System description

The circuit diagram of the proposed MVB is shown in Fig. 4, where a dual-switching-leg consisting of IGBT switches S_7, S_8, S_9 , and S_{10} , have been added. Together with two neutral inductors L_{N1} and L_{N2} , the MVB actively balances the voltage between two split capacitors, C_{N1} and C_{N2} , by moving extra energy stored in one of the capacitors to the other. Due to the dual-switching-leg configuration in the proposed MVB, current rating of the neutral wire is increased to more than twice of that in the ACSB.

Fig. 4: Circuit diagram of the proposed MVB with a three-phase inverter connected to a 3P4W power distribution network.

The focus of this paper is the neutral point configuration and its control considerations in 3P4W shunt APFs. Therefore, the input dc voltage source is assumed to be constant, and V_{DC} equals V_{bus} . The

electrical specifications of the 3P4W shunt APF are listed in Table 1. The shunt APF has a power rating of 20 kVA, with the maximum neutral current of 58 A_{rms}. This 3P4W shunt APF is used for voltage quality enhancement by providing voltage imbalance correction and harmonic mitigation in low-voltage power distribution network (230 V phase-to-neutral) [8].

Table 1: Electrical specifications of the 3P4W shunt APF

Parameter	Value	Parameter	Value
Nom. power (P_N)	20 kVA	Nom. phase current (I_{pN})	29 A _{rms}
Nom. dc bus voltage (V_{bus})	760 V	Max. phase current (I_{p_max})	33 A _{rms}
Nom. split capacitor voltage (V_{CNI} , V_{CNI})	380 V	Max. neutral current (I_{N_max})	58 A _{rms}
Max. midpoint voltage ripple (ΔV_{mid_max})	80 V	Switching frequency (f_s)	20 kHz
Grid voltage (phase to neutral) (V_g)	230 V _{rms}	Sampling frequency (f_{sample})	40 kHz

Interleaving of dual-switching-leg

The purpose of the dual-switching-leg in the proposed MVB is to actively regulate the midpoint voltage to half of the total dc bus voltage. During steady state operation the duty cycle D of the switches in the MVB is 50%. Therefore, interleaved control can be applied to the dual-switching-leg so that the total inductor current is, theoretically, ripple free [19], thus preventing HF current circulation in the split capacitors. To facilitate interleaved control, PWM signals of S_7 and S_8 need to be 180-degree phase shifted with PWM signals of S_9 and S_{10} .

The inductance of neutral inductors is designed smaller to conduct higher current ripple so that the IGBTs in the MVB operate in ZVS mode even under high neutral current. Due to interleaved control high current ripple does not propagate to the split capacitors.

Dimensioning of passive components

The proposed MVB contains two neutral inductors and two split capacitors. The neutral inductors are designed in a way to ensure ZVS of all IGBTs in the MVB, while the split capacitors are designed based on the maximum allowable midpoint voltage ripple.

If half of the peak-to-peak current ripple of the inductor is larger than the neutral current, the switches of the proposed MVB operate under ZVS condition, which eliminates the turn-on losses of IGBTs and reverse recovery losses of the anti-parallel diodes. However, a higher neutral inductor ripple also results in higher turn-off switching losses and higher conduction losses of the IGBTs in the MVB. According to the requirements of the power converter, the maximum neutral current is 58 A_{rms}. If the neutral inductor is designed to maintain full ZVS operation of the IGBTs in the MVB under all conditions, the inductor ripple current is too high to stay power efficient. Instead, the nominal phase current I_{pN} is considered as the neutral current of interest. Therefore, the neutral inductance can be derived as

$$L_{N1} = L_{N2} = \frac{DV_{bus}}{2kf_s I_{pN_peak}} \quad (1)$$

where duty cycle D equals 50% during steady state operation, k is the interleaving coefficient ($k=2$ for ACSB and $k=1$ for the proposed MVB), and I_{pN_peak} is the peak value of nominal phase current. Solution of (1) with some margin leads to an inductance of neutral inductors in ACSB,

$$L_N = 110 \mu\text{H}. \quad (2)$$

Similarly, solution of (1) leads to an inductance of the neutral inductor in the proposed MVB,

$$L_{N1} = L_{N2} = 220 \mu\text{H}. \quad (3)$$

Provided with the peak neutral current I_{N_peak} and maximum allowable midpoint voltage ripple ΔV_{mid_max} in Table 1, the capacitance C_{N1} and C_{N2} in conventional split dc bus approach can be derived through

$$C_{N1} = C_{N2} = \frac{I_{N_peak}}{2\Delta V_{mid_max}} \int_0^{\frac{1}{2f_g}} \sin(2\pi f_g t) dt = \frac{I_{N_peak}}{2\pi f_g \Delta V_{mid_max}} \quad (4)$$

where f_g is the grid frequency ($f_g=50$ Hz). Solution of (4) with some margin leads to

$$C_{N1} = C_{N2} = 3.3 \text{ mF}. \quad (5)$$

As for ACSB approach and the proposed MVB, a small capacitance of 100 μF is enough to maintain a stable dc bus midpoint voltage. Compared to that of the conventional split dc bus, the capacitance in ACSB approach and the proposed MVB is about 30 times smaller.

Control considerations

Fig. 5 shows the control scheme of the proposed MVB, where $H_{iLN1}(z)$, $H_{iLN2}(z)$, $H_{iN}(z)$, $H_{vCN1}(z)$, and $H_{vCN2}(z)$ are sensor gains of the inductor current samplings, neutral current sampling and split capacitor voltage samplings, respectively. Further, i_{LN1_sen} , i_{LN2_sen} , i_{N_sen} , v_{CN1_sen} , and v_{CN2_sen} denote the sampled neutral inductor currents, neutral current (zero-sequence current), and split capacitor voltages. According to Fig. 4, the capacitor charging/discharging current i_C is equal to the total inductor current i_L minus the neutral current i_N , as in

$$i_C = i_L - i_N. \quad (6)$$

The control scheme of the proposed MVB contains two loops: an inner current loop and an outer voltage loop. The inner loop controls the total inductor current ($i_L = i_{L1} + i_{L2}$), which guarantees the fast tracking of the neutral current i_N . Hence, only a close-to-zero value of i_C is injected into the neutral point even under severe neutral current transient. Therefore, the midpoint voltage of split capacitors is fast stabilized. The outer loop sets the current reference i_{C_ref} for charging and discharging the split capacitors. Block $G_v(z)$ is the outer loop controller, while block $G_{i1}(z)$ and block $G_{i2}(z)$ are the inner loop controllers, which are all implemented by PI compensators.

Fig. 5: Control scheme of the proposed split dc bus mid-point voltage balancer.

Simulation verification

MATLAB simulation has been carried out to verify the proposed MVB. The performance of the ACSB has also been investigated and the results are compared with the proposed MVB in terms of midpoint voltage stability, voltage imbalance correction capability, and HF current ripple content. All simulations are carried out under the maximum asymmetric condition either based on the circuit handling capability or based on the load condition. The simulation parameters of the proposed MVB and the ACSB are listed in Table 2. The switching frequency of the converter is 20 kHz and the sampling rate is chosen at 40 kHz.

Table 2: Simulation parameters of the proposed MVB and the ACSB

Parameter	Value	Parameter	Value
Nominal power of the APF (P_N)	20 kVA	Neutral inductor in ACSB (L_N)	110 μ H
DC bus voltage (V_{bus})	760 V	Neutral inductors in MVB (L_{N2}, L_{N2})	220 μ H
Switching frequency (f_s)	20 kHz	Split capacitors (C_{N1}, C_{N2})	100 μ F

When one phase of the shunt APF sinks nominal current from the grid while the other two phases inject nominal current to the power grid, or vice versa, the shunt APF operates under the worst condition of load asymmetry. The neutral current is twice of the phase current, which is 58 A_{rms}, and the current unbalance factor (IUF) [20], in this case, is 200%.

However, the maximum phase current I_{p_max} of the shunt APF, according to Table 1, is 33 A_{rms}, which means the current limit of the switching leg in the ACSB is also 33 A_{rms}. Therefore, the ACSB can only provide limited voltage imbalance correction during the worst load asymmetry. Since dual-switching-leg is employed in the proposed MVB, the voltage imbalance correction capability is not compromised even under the worst load asymmetry. Table 3 summarizes maximum ratings of the ACSB and the proposed MVB.

Table 3: Maximum ratings of ACSB and the proposed MVB

Description	ACSB	Proposed MVB
Max. phase current (I_{p_max})	33 A _{rms}	33 A _{rms}
Max. neutral inductor current (I_{L_max})	33 A _{rms}	66 A _{rms}
Max. neutral current (I_{N_max})	22 A _{rms}	58 A _{rms}
Voltage imbalance correction capability*	38%	100%

* The voltage imbalance correction capability mentioned above is specified under the worst load asymmetry condition, where a 58 A_{rms} zero-sequence current is presented.

A. ACSB under asymmetric load

Fig. 6 shows the simulation results of the ACSB under asymmetric load condition, where the neutral wire conducts 22 A_{rms}. These results include neutral inductor current i_{LN} , neutral current i_N , charging/discharging current of split capacitors i_C , and voltage of split capacitors v_{CN1} and v_{CN2} . A load transient is added at 0.5 s to verify the dynamic performance of the ACSB.

As shown in Fig. 6(d), the voltage of the split capacitors v_{CN1} and v_{CN2} is stabilized with a voltage ripple less than 20 V, which meets the requirement in Table 1. However, due to the phase current rating limitation (33 A_{rms}) and the existence of high current ripple in the neutral inductor current i_{LN} , the maximum neutral current i_N the ACSB can handle is 22 A_{rms}. This is only 38% of the neutral current under the worst asymmetric condition. Moreover, the neutral inductor current i_{LN} is not able to track the neutral current i_N accurately in HF (20 kHz), as shown in Fig. 6(b). As a result, the HF current ripple (close to 100 A_{pp}) in neutral current passes to the charging/discharging current of split capacitors i_C , as shown in Fig. 6(c). This HF current circulates inside the split capacitors branch, causing additional midpoint voltage variation as well as overheating of the split capacitors.

B. Proposed MVB under asymmetric load

The maximum neutral current the proposed MVB can handle is increased by 164% (22 A_{rms} to 58 A_{rms}) compared to that of the ACSB, because of the employment of a dual-switching-leg. Therefore, the proposed MVB can fully correct the voltage imbalance even under the worst load asymmetry.

Fig. 7 shows the simulation results of the proposed MVB under the worst asymmetric load, where the neutral wire conducts 58 A_{rms}. These results include neutral inductor current i_{LN1} and i_{LN2} , comparison of total inductor current i_L and neutral current i_N , charging/discharging current of split capacitors i_C , and

voltage of split capacitors v_{CN1} and v_{CN2} . A load transient is added at 0.5 s to verify the dynamic performance of the ACSB.

Due to interleaved control, the current ripples in two neutral inductors counteract each other, as shown in Fig. 7(a), so that the HF ripple in total inductor current i_L (shown in Fig. 7(b)) is decreased significantly (close to 10 A_{pp}, as shown in Fig. 7(c)). As a result, the voltage of the split capacitors v_{CN1} and v_{CN2} is stabilized with voltage ripple less than 10 V, which also meets the requirement in Table 1. In the proposed MVB, small neutral inductors and split capacitors are enough to stabilize the midpoint voltage, keeping the IGBTs in the proposed MVB under ZVS operation, while reducing HF current circulation in the split capacitors.

Fig. 6: Simulation results of the ACSB under asymmetric load. (a) Neutral inductor current i_{LN} . (b) Comparison of inductor current i_{LN} and neutral current i_N . (c) Charging/discharging current of split capacitors. (d) Voltage of the split capacitors v_{CN1} and v_{CN2} .

Fig. 7: Simulation results of the proposed MVB under the worst load asymmetry. (a) Neutral inductor current i_{LN1} and i_{LN2} . (b) Comparison of total inductor current i_L and neutral current i_N . (c) Charging/discharging current of split capacitors. (d) Voltage of the split capacitors v_{CN1} and v_{CN2} .

Experimental verification

A 20 kVA 3P4W shunt APF prototype, as shown in Fig. 8, has been built to verify the proposed MVB. The prototype is implemented using two three-phase IGBT power modules. Current and voltage signals acquisition and PWM generation are implemented in dSPACE MicroLabBox. An external dc voltage

source provides constant voltage to the input of the prototype. The 3P4W shunt APF has been tested in off-grid mode.

Fig. 8: Photograph of the 20 kVA 3P4W shunt APF prototype with proposed MVB.

Fig. 9 shows the experimental current waveforms of the proposed MVB, including the neutral inductor current i_{LN1} , i_{LN2} , and the total inductor current i_L , as well as the comparison between the total inductor current i_L and the neutral current i_N . Current ripple in the total inductor current i_L is much smaller than the individual neutral inductor current (i_{LN1} and i_{LN2}) because of the interleaved control, as shown in Fig. 9(a). The total inductor current i_L tracks the neutral current i_N well both in amplitude wise and phase wise, as shown in Fig. 9(b). According to (6), therefore, only close-to-zero current i_C is inject into the split capacitors, thus keeping the midpoint voltage stabilized.

Fig. 10 shows the experimental voltage waveforms of the proposed MVB including dc bus voltage V_{bus} and split capacitors voltage v_{CN1} , v_{CN2} . A neutral current transient of $66 \text{ A}_{\text{peak}}$ was added at 2.18 s to verify the dynamic performance of the proposed MVB. The voltage ripples of the split capacitors are around 10 V, which is within 1.5% of the total dc bus voltage. Therefore, the midpoint voltage of the APF prototype is well stabilized even under severe neutral current transient of $66 \text{ A}_{\text{peak}}$.

Fig. 9: Experimental current waveforms of the proposed MVB. (a) Neutral inductor currents i_{LN1} , i_{LN2} and total inductor current i_L . (b) Comparison of total inductor current i_L and neutral current i_N .

Fig. 10: Experimental voltage waveforms of the proposed MVB. (a) Voltage of the dc bus V_{bus} . (b) Voltage of the split capacitors v_{CN1} and v_{CN2} .

Conclusion

A neutral point is essential for 3P4W shunt APFs to compensate zero-sequence current component under voltage imbalance in power distribution networks. Existing solutions for neutral point creation include conventional split dc bus, fourth-switching-leg and ACSB. The ACSB approach is more promising in terms of dc current component handling, ease of development, EMC consideration and midpoint voltage stabilization performance. However, the shunt APF with ACSB only provides limited voltage imbalance correction under severe load asymmetry. Moreover, a large HF charging/discharging current circulates inside the split capacitors, which causes additional midpoint voltage variation as well as split capacitors overheating.

A dual-switching-leg based MVB is proposed in this paper. It provides fast voltage stabilization of the split dc bus midpoint in 3P4W shunt APFs. Due to the employment of the dual-switching-leg, the neutral current tracking capability is increased by 164% compared to that of the ACSB. Interleaved control is adopted in the proposed MVB to prevent HF current circulation in split capacitors, and to facilitate an accurate neutral current tracking. All IGBTs of the MVB operate in ZVS mode when the neutral current is smaller than the nominal phase current of the APF. The experimental results of a 20 kVA prototype showed that the midpoint voltage ripple was maintained within 1.5% of the total dc bus voltage, even under severe neutral current transient.

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