Low-frequency noise in modern semiconductor transistors
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Low-Frequency Noise in Modern Semiconductor Transistors

Hans Markus
Low-Frequency Noise in Modern Semiconductor Transistors
Dit proefschrift is goedgekeurd door de promotoren:

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Chapter 1

GENERAL INTRODUCTION

1.1 ELECTRICAL NOISE

noise (noiz) n. ... In communications, the confused sound caused by discordant vibrations or undesirable random voltages in a channel.

This is a definition of the term "noise" according to Webster's dictionary [1]. Probably this definition of (electrical) noise describes the common way people encounter noise in daily life. Since we are dealing with an undesirable phenomenon we are interested in reducing its influence.

This dissertation deals with the low-frequency noise in modern semiconductor devices. The noise in these devices can be observed either as fluctuations in the voltage across the device terminals or as fluctuations in the current through the device.

When these devices are applied in measurement circuits their noise sets a lower limit to the sensitivity and accuracy of these circuits. In high frequency oscillators, as used in telecommunication applications, the low-frequency noise spectrum originating from these devices is transformed to high frequencies, due to the non-linearity of these devices and circuits. This leads to the very undesirable phase noise. These are two examples of important technical arguments for studying the (low-frequency) noise of modern semiconductor devices.

Since noise stems from spontaneous fluctuations of physical quantities we cannot avoid it entirely. However, if we can understand the (physical) origin of the noise we can develop strategies for minimizing it or its influence.

In semiconductor devices four important kinds of noise exist: thermal noise, shot noise, generation-recombination noise, and flicker noise.

1) Thermal noise, Nyquist noise, or Johnson noise is due to the Brownian movement of the charge carriers. The power spectral density of the open circuit voltage fluctuations $S_V$ of an ohmic device is given by [2]

$$S_V = 4kTR$$

where $k$ is Boltzmann's constant, $T$ the temperature, and $R$ the resistance of the sample. The power spectral density is constant to frequencies up to $f \equiv 1/(2\pi RC)$ or $f \equiv 1/\tau_{coll} \equiv 10^{12}$ Hz. Here $C$ is the (parasitic) capacitance parallel to $R$, and $\tau_{coll}$ the collision time of the free charge carriers in the resistance. For this reason the thermal noise is called a white noise at low frequencies. There is also a quantum cut-off for the thermal noise at $f > kT/h = 6250$ GHz [3].

2) Shot noise is generated when charge carriers encounter a potential barrier and cross it independently of each other at random. The short circuit power spectral density is given by
\[ S_I = 2qI \] (1.2)

The power spectral density is constant up to \( f = 1/\tau_{\text{trans}} \) with \( \tau_{\text{trans}} \) the transit time across the barrier. In p-n diodes we have \( \tau_{\text{trans}} = 10^{-11} \) s. Therefore, shot noise is also called white noise.

3) Generation-recombination noise or g-r noise is due to fluctuations in the number \( N \) of free charge carriers in the conduction band and/or in the valence band. These fluctuations in the number of free carriers is caused by random trapping and detrapping of carriers. Fluctuations of the number of free charge carriers results in fluctuations in the conductance. These conductance fluctuations can be measured by passing a current through the sample. The power spectral density of the fluctuations in \( N \) is given by [2]

\[ S_N = \frac{4\tau \langle \Delta N^2 \rangle}{1 + \omega^2 \tau^2} \] (1.3)

where \( \tau \) is the relaxation time of the trapping process, \( \langle \Delta N^2 \rangle \) the variance of the fluctuations \( \Delta N \), and \( \omega \) the circular frequency. By reducing the number of traps we can reduce this type of noise. Equation (1.3) holds for a two level system, i.e. a conduction (valence) band and one trap level. If the g-r noise stems from one single trap it is called random telegraph noise (RTS noise).

4) 1/f Noise owes its name to its spectral density that is almost inversely proportional to the frequency over a wide frequency range down to very low frequencies \( (10^{-6} \) Hz). This noise is a fluctuation of the conductivity. It has been observed in carbon resistors [4], ion concentration cells [5], metals [6], superconductors [7–9], and semiconductors [10].

1.2 THE ORIGIN OF 1/f NOISE

Hooge presented an empirical relation for the 1/f noise in homogeneous samples of semiconductors and of metals [6]

\[ \frac{S_G}{G^2} = \frac{\alpha}{fN} \] (1.4)

where \( S_G \) is the noise power spectral density of the fluctuations in the conductance \( G \), \( N \) is total number of free charge carriers, and \( \alpha \) is a dimensionless parameter. The parameter \( \alpha \) is widely used as a normalized measure of 1/f noise in semiconductor devices.

1/f Noise is caused by fluctuations in the conductivity. In semiconductors the conductivity is given by

\[ \sigma = q(\mu_n n + \mu_p p) \] (1.5)

where \( q \) is the elementary charge, \( \mu_n \) and \( \mu_p \) are the mobility of electrons and holes, and \( n \) and \( p \) are the concentration of free electrons and holes, respectively. Hence
conductivity fluctuations can be caused by fluctuations of the number of free carriers or by fluctuations of the mobility.

At this time there is no generally accepted theory for the 1/f noise in semiconductors. There are three major schools of thought that will be discussed briefly in this paragraph.

A model that assumes that the 1/f noise is caused by fluctuations in the number of free carriers is the McWorther model [11]. The fluctuations in the number of free carriers are caused by spontaneous trapping and de-trapping of these carriers in interface states or traps located in oxides at some distance from the oxide semiconductor interface. Only traps within a few $kT$ of the Fermi-level are effective in generating noise. It is assumed that the density of traps in the oxide is constant though the oxide and the probability of penetrating the trap decreases exponentially with the distance from the interface. The trapping and de-trapping in these traps produce g-r spectra with distributed relaxation times $\tau$. The 1/f spectrum is a result of a weighted superposition of these g-r spectra.

A second school of thought considers carrier scattering at lattice vibrations to be the cause of 1/f fluctuations [10,12]. So here the mobility is assumed to fluctuate. Since in this process no traps are needed this model also implies that there is 1/f noise even if no traps are present [10,13].

The third school of thought is the quantum 1/f noise theory, as it was first proposed by Handel [14]. This theory ascribes the 1/f noise to electromagnetic effects, associated with any type of scattering of electrons. This leads to fluctuations in the mobility. The model is in agreement with Hooge's relation, but the model predicts $\alpha$-values that are much lower than the experimentally observed ones [15]. A later modification, introduced to reconcile calculated and experimental $\alpha$-values, suggests coherent quantum 1/f noise [16,17]. The validity of this theory is still under discussion [12,15,18-23].

In this thesis we shall use the empirical relation (1.4) without a further discussion of the three models.

1.3 LOW-FREQUENCY NOISE IN BIPOLAR JUNCTION TRANSISTORS

A large part of this thesis deals with the 1/f noise in bipolar transistors. In this section the main low-frequency noise generators and their location in a bipolar transistor will be discussed.

In conventional bipolar transistors the main low-frequency noise generators are generally accepted to be located between emitter and collector, and between emitter and base. In principle there is also a noise generator between collector and base, but the collector-base junction is normally operated in reverse bias, so that the base-collector current, and hence the noise in the base-collector current are negligible.

Due to the down-scaling of modern devices the parasitic base and emitter series resistances are becoming important, not only with respect to the DC and AC characteristics but as well because of the fact that these resistances can generate low-frequency noise.

In fig. 1.1 a hybrid-π model of a transistor is given. The main low-frequency noise generators and the parasitic series resistances are included. The current noise
generators $S_{I_b}$ and $S_{I_c}$ represent the spontaneous fluctuations in the base current and collector current, respectively. $S_{I,r_b}$ and $S_{I,r_e}$ represent the current noise generators in the parasitic series resistances.

The input impedance $r_\pi$ and the transconductance $g_m$ are defined by

$$r_\pi = \frac{\mathcal{A}_B}{\mathcal{V}_{be}} \quad \text{and} \quad g_m = \frac{\mathcal{A}_C}{\mathcal{V}_{be}}$$

(1.6)

where $V_{be}$ is the base-emitter voltage corrected for the voltage drop across the series resistances $V_{be} = V_{BE} - I_B r_b - I_E r_e$, where $I_B$ is the base current and $I_E$ is the emitter current.

Fig. 1.1 Hybrid-π model of a conventional transistor with low-frequency noise generators.

With the help of the transistor model of fig. 1.1 one can calculate the noise at the transistor contacts when the transistor is part of a measurement circuit [24].

Generally $S_{I_b}$ and $S_{I_c}$ consist of shot noise and 1/f noise

$$S_{I_b} = 2qI_B + S_{I_b}^{1/f} \quad \text{and} \quad S_{I_c} = 2qI_C + S_{I_c}^{1/f}$$

(1.7)

where $I_C$ is the collector current.

Expressions for $S_{I_b}^{1/f}$ and $S_{I_c}^{1/f}$ are given in [25-28].

Generally $S_{I,r_b}$ and $S_{I,r_e}$ consist of Nyquist noise and a contribution caused by the resistance noise $S_{r_b}$ and $S_{r_e}$:

$$S_{I,r_e} = \frac{4kT}{r_e} + I_E^2 \frac{S_{r_e}}{r_e^2} \quad \text{and} \quad S_{I,r_b} = \frac{4kT}{r_b} + I_B^2 \frac{S_{r_b}}{r_b^2}$$

(1.8)

where $S_{r_b}$ and $S_{r_e}$ can consist of g-r noise, RTS (random telegraph signal) noise, and 1/f noise.

1.4 LOW-FREQUENCY NOISE IN MODFETs AND MOSFETs

Due to the down-scaling of MOSFETs and Modulation Doped FETs (MODFETs) the influence of parasitic series resistance increases. This influence is not limited to the DC and AC characteristics. The series resistance can also generate low-frequency
noise. In Fig 1.2 the equivalent circuit of the channel of a MOSFET or MODFET in the ohmic region is given. $R_{ch}$ is the channel resistance, $R_{ss}$ is the series resistances at the source side is and $R_{sd}$ is the series resistance at the drain side. In this figure the current noise generators are included for the channel, denoted by $S_{I,R_{ch}}$, and for the series resistances, denoted by $S_{I,R_{ss}}$ and $S_{I,R_{sd}}$.

\[
S_{I,R_{ch}} = \frac{4kT}{R_{ch}} + I_D^2 \frac{S_{R_{ch}}}{R_{ch}^2},
\]
\[
S_{I,R_{ss}} = \frac{4kT}{R_{ss}} + I_D^2 \frac{S_{R_{ss}}}{R_{ss}^2},
\]
\[
S_{I,R_{sd}} = \frac{4kT}{R_{sd}} + I_D^2 \frac{S_{R_{sd}}}{R_{sd}^2},
\]

(1.9)

where $S_{R_{ch}}$, $S_{R_{ss}}$, and $S_{R_{sd}}$ can consist of 1/f noise, $\alpha$-noise, and RTS noise.

1.5 OUTLINE

In chapter 2 we start with an explanation of the procedure we follow for the determination of the dominant noise generators in bipolar junction transistors from the measurement of the voltage noise spectra at the emitter and collector contact. This procedure is applied to most bipolar transistors discussed in this thesis.

The main subject of chapter 2 is the investigation of the emitter geometry dependence of both the $I$-$V$ characteristics and the 1/f noise in a series of silicon transistors with a conventional emitter.

Chapter 3 deals with the 1/f noise in polysilicon-emitter bipolar junction transistors. We studied transistors with different emitter areas and different oxide layers at the monosilicon-polysilicon interface. One type of transistors has a native oxide at the polysilicon-monosilicon interface. The second type has a thermally grown oxide at the polysilicon-monosilicon interface.

In the second part of chapter 3 experiments are described for measuring the coherence between the base current 1/f noise and emitter series resistance 1/f noise in polysilicon-emitter bipolar transistors.
Chapter 1. General introduction

In chapter 4 we present the results of low-frequency noise measurements carried out on two series of GaInP/GaAs heterojunction bipolar transistors. The difference between the two series is the insulation of the emitter metal layer from the underlying implant insulated layer. The impact on the 1/f noise of the two production processes is investigated.

Chapter 5 is devoted to the low-frequency noise of modulation doped field effect transistors (MODFETs). In this chapter we will demonstrate some methods to characterize the 1/f noise of these devices. Two methods to determine the threshold voltage and the channel series resistance using the 1/f noise are presented. Both the 1/f noise in the two dimensional electron gas (2DEG) channel and the gate Schottky barrier are studied. A comparison is presented of devices made with different production processes and with different semiconductor materials.

In chapter 6 the results are presented of the I-V characteristics and low-frequency measurements on two so-called p-channel Gate-All-Around (GAA) Silicon-On-Insulator (SOI) MOSFETs.

References

Chapter 2

ON 1/f NOISE IN BJTS: INFLUENCE OF EMITTER GEOMETRY, EDGE EFFECTS, AND CURRENT CROWDING

Abstract - The DC I-V characteristics and the low-frequency noise of BJTs are investigated. Two wafers are studied with a set of 9 transistors with different emitter geometries. The main 1/f noise generator is the 1/f noise in the base current $S_{I_b}$. The 1/f noise is interpreted in terms of mobility fluctuations. The emitter area dependence of both the base current divided by the emitter area $(I_B/A_E)$, at constant base-emitter voltage, and the 1/f current noise $S_{I_b}$ at constant base current are interpreted in terms of a position-dependent minority carrier lifetime in the emitter. The latter explains also the anomalous base current dependence of $S_{I_b}$ when emitter current crowding is apparent.

2.1 INTRODUCTION

In most recent papers the 1/f noise in bipolar junction transistors (BJT) with a conventional emitter is mainly discussed in terms of mobility fluctuations [1]. The 1/f noise in BJTs has been interpreted in terms of two 1/f noise current generators: $S_{I_b}$ between emitter and base, and $S_{I_c}$ between emitter and collector. In principle there is also a source between base and collector. In practice the base-collector junction is reverse biased, so that the leakage base-collector current is small and its noise is negligible. Recently, Kleinpenning [2] derived formulas for low-frequency noise in BJTs, incorporating the noise sources present in the parasitic series resistances. Kooien et al. [3] studied the 1/f noise in BJTs that are similar to our transistors. They modeled the 1/f noise with $S_{I_b} = K_F I_{b1}^2/f + K_{FN} I_{b2}^2/f$, where $K_F$ and $K_{FN}$ are fitting parameters, $I_{b1}$ is the ideal base current, and $I_{b2}$ is the non-ideal base current. This model is not in agreement with the mobility fluctuation model that predicts $S_{I_b} = S_{I_b1} + S_{I_b2}$ with $S_{I_b1} \propto I_{b1}$ and $S_{I_b2} \propto I_{b2}$. In this paper we have investigated the 1/f noise in BJTs with a conventional emitter. The aim of this work was to check whether the mobility fluctuations model can provide an alternative for the Kooien [3] interpretation. Furthermore, special attention was paid to the emitter geometry dependence of the I-V characteristics and 1/f noise, and to the influence of current crowding on the 1/f noise. The results were interpreted in terms of mobility fluctuations.
2.2 EXPERIMENTAL RESULTS

A. Devices

The transistors are made by Philips Electronics. Transistors from two wafers were studied. On each wafer a set of 9 transistors with various geometries is present. The length of the emitter is in the range of $4.0 \, \mu m \leq L_e \leq 86 \, \mu m$ and its width in the range of $2.3 \, \mu m \leq H_e \leq 49.8 \, \mu m$ (see Table 2.1). The top dope of the emitter of all transistors is about $10^{20} \, cm^{-3}$. The pinched-base sheet resistance is $11.7 \, k\Omega$ for wafer 1 and $3.49 \, k\Omega$ for wafer 2. The junction depth is about $0.37 \, \mu m$. All transistors are n-p-n type.

Table 2.1. Emitter dimensions

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<th>1224</th>
<th>1290</th>
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<td>2.3</td>
<td>2.3</td>
<td>2.3</td>
<td>11.8</td>
<td>11.8</td>
<td>11.8</td>
<td>49.8</td>
<td>49.8</td>
</tr>
<tr>
<td>$L_e$ (µm)</td>
<td>4</td>
<td>8</td>
<td>20</td>
<td>86</td>
<td>4</td>
<td>20</td>
<td>86</td>
<td>4</td>
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B. I-V Characteristics

Figure 2.1 shows a typical $I$-$V$ curve of the base and collector current versus $V_{BE}$ at $V_{CB} = 3 \, V$.

Fig. 2.1. Typical $I$-$V$ curve for transistor 1224 of wafer 2.
The ideality factor for the base and collector current is 1. With the help of white noise measurements in the common collector configuration [2], we found the values of $4kT(r_e + r_b)$. From the deviation from the exponential behaviour of the $I-V$ characteristic we found $I_E r_e + I_b r_b$. Hence, the values of the internal emitter series resistance $r_e$ and the internal base resistance $r_b$ could be determined. The values found for $r_b$ agree well with the values calculated from the base sheet resistance given by the manufacturer, taking into account the part of $r_b$ that is located between base contacts and emitter edge. The value of $r_e$ depends on the emitter geometry. Also, the values of $r_e$ agreed well with the emitter sheet resistance given by the manufacturer.

In Fig. 2.2 a plot is made of $J_B = I_B / A_E$ of all transistors at $V_{be} = 0.7 \text{ V}$ versus the emitter area $A_E$. We observe a clear influence of the emitter geometry on the current density at constant $V_{be}$. Here, $V_{be}$ is the internal voltage across the base-emitter junction, obtained after correction for the voltage drop across the base and emitter series resistance.

![Fig. 2.2. The current density $J_B = I_B / A_E$ at $V_{be} = 0.7 \text{ V}$ versus the emitter area $A_E$.](image)

**C. Noise Measurements**

We made the noise measurements by putting the transistor in a circuit as shown in Fig. 2.3. The internal series resistances are given by $r_e$, $r_b$, and $r_c$ respectively. Three external metal film resistors $R_B$, $R_C$, $R_E$ can be inserted that have Nyquist noise ($4kT R$) only.
Chapter 2. On $1/f$ noise in BJTs: influence of emitter geometry...

Fig. 2.3. AC noise measurement circuit.

According to Kleinpenning [2] the $1/f$ voltage noise across $R_E$ and $R_C$ can be written as

$$ (Z / R_E)^2 S_v \ = \ [r_\pi - \beta (r_B + R_B)]^2 S_{1b} $$

$$ + [r_\pi + r_b + R_B]^2 S_{I_b} + (\beta + 1)^2 [I_B^2 S_{r_b} + I_E^2 S_{r_e}] \quad (2.1) $$

$$ (Z / R_C)^2 S_v = \beta^2 [r_b + R_B + r_e + R_E]^2 S_{I_b} $$

$$ + [r_\pi + r_b + R_B + r_e + R_E]^2 S_{I_c} + \beta^2 [I_B^2 S_{r_b} + I_E^2 S_{r_e}] \quad (2.2) $$

with

$$ Z = r_b + R_B + r_\pi + (\beta + 1)(r_e + R_E) \quad (2.3) $$

$$ r_\pi = \partial V_{be} / \partial I_B \quad (2.4) $$

$$ \beta = \partial V_{ce} / \partial I_B = g_{mc} \cdot r_\pi \quad (2.5) $$

Here, $g_{mc}$ represents the collector transconductance, $\beta$ the current amplification factor, and $r_\pi$ the input resistance of the intrinsic transistor. $S_{I_b}$ and $S_{I_c}$ represent the $1/f$ current noise spectral density at constant $V_{be}$ in the base and collector currents, respectively. The internal resistances $r_e$ and $r_b$ can have $1/f$ resistance noise. Their spectral densities are represented by $S_{r_b}$ and $S_{r_e}$, respectively. The Early effect has been neglected in the derivation of (2.1) and (2.2). This is permissible since $I_C$ was found to be almost completely independent of $V_{CB}$ at $V_{CB} > 1$ V.

In order to locate and characterize the $1/f$ noise sources, we carried out our measurements in both the common-emitter (C-E) and common-collector (C-C) configuration at various biasing conditions.

In the C-C configuration we took $R_E >> r_e, r_{\pi}, R_B$, so that $Z / R_E = \beta + 1$, and $R_C = 0$. Thus (2.1) is simplified to
Experimental results

\[ g_{me}^2 S_{V_E} = \left[ 1 - g_{mc} (r_b + R_B) \right]^2 S_I_b + \left[ 1 + (r_b + R_B) / r_\pi \right]^2 S_I_c \]

\[ + g_{me}^2 \left[ I_B^2 S_{r_b} + I_E^2 S_{r_e} \right] \]

(2.6)

Here, \( g_{me} = (\beta + 1) / r_\pi = \partial I_E / \partial V_{be} \) is the emitter transconductance of the intrinsic transistor.

In the C-E configuration we put \( R_E = 0, R_B >> r_b, r_\pi (\beta + 1) r_e, \) and \( R_C = 100 \, \Omega \), so that \( Z = R_B \). Then (2.2) reduces to

\[ S_{V_C} / R_C^2 = \beta^2 S_I_b + S_I_c + (\beta / R_B)^2 \left[ I_B^2 S_{r_b} + I_E^2 S_{r_e} \right] \]

(2.7)

The noise measurements were performed in the current ranges \( 0.1 \, \mu A \leq I_B \leq 100 \, \mu A \) and \( 10 \, \mu A \leq I_C \leq 10 \, mA \). In these current ranges the input resistance \( r_\pi = kT/qI_B \) varies from 250 \( \Omega \) to 250 k\( \Omega \), the collector transconductance \( g_{mc} = qI_C/kT \) from \( 4 \cdot 10^{-4} \, \Omega^{-1} \) to 0.4 \( \Omega^{-1} \), and the emitter transconductance \( g_{me} = g_{mc} + 1 / r_\pi \) from \( 4 \cdot 10^{-4} \, \Omega^{-1} \) to 0.4 \( \Omega^{-1} \). These parameters, being the parameters of the intrinsic transistor, are different from those of the complete transistor that are defined by \( \partial V_{BE} / \partial I_B, \partial I_C / \partial V_{BE} \) and \( \partial V_{BE} / \partial V_{BE} \), respectively, with \( V_{BE} = V_{be} + I_b r_b + I_e r_e \).

Spectral noise densities were measured from 1 Hz to 100 kHz. All devices showed 1/f noise. The 1/f spectral density was observed over at least two decades of frequency, but depending on emitter geometry and current reaching up to 4 decades of frequency. In Fig. 2.4 some typical noise spectra of \( S_{V_C} / R_C^2 \) versus the frequency, measured in the C-E configuration, are presented.

Fig. 2.4. Plot of the spectra of the current noise \( S_{V_C} / R_C^2 \) versus the frequency of transistor 1208 of wafer 2. The spectra are measured at a base current of A: 0.45 \( \mu A \), B: 1.7 \( \mu A \), C: 12 \( \mu A \), and D: 60 \( \mu A \).
With the help of (2.6) and (2.7) we can determine the dominant noise sources. In (2.6) both $S_{I_b}$ and $S_{I_c}$ have a prefactor of one at low currents, where $g_{mc}(r_b + R_B) << 1$ and $(r_b + R_B)/r_c << 1$. However in (2.7) the contribution of $S_{I_b}$ only is amplified by a factor $\beta^2$. Also the contributions of the resistance noise $S_{rb}$ and $S_{re}$ have different prefactors in (2.6) and (2.7). So by measuring both in the C-E and C-C configuration at low and high currents and analyzing the results with the help of (2.6) and (2.7), one can decide whether $S_{I_b}$, $S_{I_c}$, $S_{re}$ or $S_{rb}$ is dominant. Our measurements reveal that $S_{I_b}$ is dominant; the contributions from $S_{I_c}$, $S_{rb}$, and $S_{re}$ can be neglected.

In Fig. 2.5 some typical plots are presented of the spectral density of the base current noise $S_{I_b}$ at 1 Hz versus $I_B$. We observed that most transistors exhibit $S_{I_b} \propto I_B^{-1}$. Only the transistors (e.g. type A) with a large ratio $H/L$, i.e. a high pinched-base resistance, show $S_{I_b} \propto I_B^\gamma$ with $1 \leq \gamma \leq 2$.

![Fig. 2.5. Typical base current 1/f noise spectra of three transistors. A: 5008 wafer 1, B: 5090 wafer 1, and C: 1208 wafer 2.](image)

In Fig. 2.6 the 1/f noise $S_{I_b}/I_B$ from devices of both wafers is plotted versus the emitter area $A_E$. We observe that roughly $S_{I_b}/I_B \propto A_E^{-1}$.

2.3 DISCUSSION

A. I-V Characteristics

The junction depth of the emitter base junction is 0.37 µm. The hole lifetime in the emitter is roughly $10^{-10}$ s, and the diffusivity is 1.2 cm²/s [4]. So the diffusion length
of holes in the emitter is 0.1 µm. Thus we use the long diode approximation of the base current density given by

$$J_B = \frac{q n_i^2 \sqrt{D_p}}{N_E \sqrt{\tau_p}} \exp \left( \frac{q V_{be}}{kT} \right)$$

(2.8)

Fig. 2.6. A plot of $S_{I_B}/I_B$ measured at 1 Hz versus the emitter area $A_E$.

Here, $\tau_p$ is the hole lifetime, $D_p$ the diffusivity of holes, $N_E$ the doping of the emitter, and $n_i$ the intrinsic carrier concentration in the emitter. In Fig. 2.2 we observe that the average base current density, defined by $I_B/A_E$ and measured at $V_{be} = 0.7$ V depends on the emitter geometry. This can be ascribed to a distributed hole lifetime in the emitter. At the edge of the emitter this lifetime might be smaller than in the central part of the emitter [5]. The emitter can be modeled using two hole lifetimes $\tau_c = \tau_p$ for the emitter center area $A_c$, and an effective lifetime $\tau_e$ for the area of the emitter edge $A_e$. According to (2.8) this effective lifetime $\tau_e$ is related to the average value of $1/\tau_p^{1/2}$ at the emitter edge, so that

$$\frac{1}{\tau_e^{1/2}} = \left( \frac{1}{\tau_p^{1/2}} \right)_{A_e}$$

(2.9)

For the total base current we find

$$I_B = I_{Be} + I_{Bc} = C_0 \left[ \frac{A_e}{\sqrt{\tau_e}} + \frac{A_c}{\sqrt{\tau_c}} \right]$$

with

$$C_0 = \frac{q n_i^2 \sqrt{D_p}}{N_E} \exp \left( \frac{q V_{be}}{kT} \right)$$

(2.10)

where $I_{Be}$ and $I_{Bc}$ are the base currents through the emitter edge and through the central part of the emitter, respectively. We assume the edge area to extend to a length $l$ into the emitter, so that $A_e$ is roughly equal to $P\cdot l$, where $P$ is the emitter...
perimeter. A top-view of the emitter is given in Fig. 2.7a. The perimeter $P$ is roughly proportional to $\sqrt{A_E}$, and therefore in approximation $A_e \propto \sqrt{A_E}$. Hence, for $\tau_e \ll \tau_c$ and for small emitter areas, (2.10) predicts that $I_B/A_E$ measured at a constant $V_{be}$ is roughly proportional to $A_e/A_E \propto A_E^{-1/2}$.

![Fig. 2.7. Top view of the emitter. The shaded areas a) and b) represent $A_e$ with effective lifetime $\tau_e$ and $\tau_c^*$, the white areas represent $A_c$ with carrier lifetime $\tau_c$.](image)

For large emitter areas (2.10) predicts $I_B/A_E$ is independent of $A_E$. Applying (2.10) to the experimental results in Fig. 2.2 we obtain the two solid lines. We observe that $I_{Be} = I_{Be}$ for emitter areas of about 10 $\mu$m$^2$.

**B. 1/f noise**

Suppose one finds $S_{Ib} \propto I_B^k$ experimentally. Then, provided that both the current density and the noise sources are homogeneously distributed over the emitter area, one can derive [6]

$$S_{I_b} = I_B^k \cdot A_E^{1-k}$$

(2.11)

Mostly for our transistors $S_{I_b} \propto I_B$, so we expect $S_{Ib}/I_B$ to be independent of the emitter area. However, in Fig. 2.6 we already noticed that $S_{Ib}/I_B \propto A_E^{-1}$, roughly.

In section 2.3A we noted that the current density in the emitter is non-homogeneous, which we ascribed to a minority carrier lifetime that is smaller in the emitter edge than in the central part of the emitter. As a consequence, the mobility fluctuation model for a long diode [7] predicts that the 1/f noise generated per unit of current is higher in the emitter edge than in the central part of the emitter. For the total 1/f noise in the base current we have

$$S_{I_b} = S_{I_{Be}} + S_{I_{Be}} = \frac{\alpha q}{4f} \left[ \frac{I_{Be}}{\tau_e} + \frac{I_{Be}}{\tau_c} \right] = \frac{\alpha q C_0}{4f} \left[ \frac{A_e}{\tau_e^{1/2}} + \frac{A_c}{\tau_c^{3/2}} \right]$$

(2.12)
where $S_{IBe}$ and $S_{IBc}$ are the 1/f noise in the current through the emitter edge $I_{Be}$ and the central part of the emitter $I_{Bc}$, respectively, and $\alpha$ is the Hooge parameter. The effective lifetime $\tau_e^*$ is defined by

$$1/(\tau_e^{1/2}\tau_e^*) = 1/(\tau_p^{3/2})_{A_e}$$

(2.13)

Equation (2.13) follows from the proportionality $S_I \propto \tau_p^{-3/2}$ for homogeneous long diode and from (2.12). Combining (2.10) and (2.12) we obtain an expression for $S_{Ib}$ as a function of the emitter area.

$$S_{Ib} = \frac{\alpha q I_B}{4f\tau_c} \left( \frac{\tau_c - 1}{\tau_e - \frac{\tau_e}{\sqrt{\tau_c}} \frac{A_E}{A_e}} \right)$$

(2.14)

For large emitter areas, i.e. $A_E >> A_e$, both the current and the 1/f noise of the central part of the emitter are dominant. For small emitter areas, i.e. $A_E = A_e$, both the current and the 1/f noise of the emitter edge area are dominant. For intermediate emitter areas the current is dominated by the central part of the emitter and the 1/f noise by the emitter edge. In this intermediate range the 1/f noise of $S_{Ib}/I_B$ decreases with increasing emitter area.

We have defined an effective minority carrier lifetime at the emitter edge area $\tau_e$ by (2.9) for the current and $\tau_e^*$ by (2.13) for the 1/f noise. The latter can be much smaller than the first depending on the specific minority carrier lifetime distribution in the emitter edge area. However, in order to make an estimate of the values of $l, A_e, A_c, \tau_c$, and $\tau_e$ we assume $\tau_e^*/\tau_e = (\tau_p^{-1/2})_{A_e}/(\tau_p^{-3/2})_{A_e} = 1$.

On the basis of the results in Fig. 2.2 we already concluded that at $A_E = 10 \mu m^2$ we have $A_e/\sqrt{\tau_e} = A_c/\sqrt{\tau_c}$. Consequently the ratio $A_e/A_E$ at $A_E = 10 \mu m^2$ is found to be

$$\frac{A_e}{A_E} = \frac{1}{1 + \sqrt{\tau_c}/\tau_e}$$

(2.15)

For devices with $A_E = 10 \mu m^2$ substitution of (2.15) into (2.14) yields

$$\frac{S_{Ib}}{I_B} = \frac{\alpha q}{4f\tau_c} \left[ \frac{1 + \tau_c/\tau_e^*}{2} \right]$$

(2.16)

In Fig. 2.6 we observe that $S_{Ib}/I_B$ at $A_E = 10 \mu m^2$ is of the order of a factor 100 larger than at $A_E = 10^4 \mu m^2$. So we conclude that the factor in between brackets in
(2.16) is at least 100 and thus \( \tau_c / \tau_e^* \geq 10^2 \). With the help of (2.15) we obtain \( A_c = PL \leq 0.1AE \) and thus \( l \leq 0.1 \mu m \).

In Fig. 2.8 we have plotted \( I_B/A_c \) versus \( A_e/A_c \). The areas \( A_e \) and \( A_c \) are calculated using \( l = 0.1 \mu m \). On the basis of (2.10) we expect the plot to be linear. The value of \( \tau_e \) can be found from the intersection at \( A_e/A_c = 0 \). The value of \( \tau_c \) can be obtained from the slope. We found \( \tau_c = 6 \cdot 10^{-10} \) s, \( \tau_e = 1 \cdot 10^{-11} \) s for wafer 1, and \( \tau_c = 5 \cdot 10^{-10} \) s, \( \tau_e = 5 \cdot 10^{-12} \) s for wafer 2. It should be noted that these \( \tau_c \) values lead to diffusion lengths of approximately 0.2 \( \mu m \), thus the long diode approximation remains valid.

In Fig. 2.8 a plot is made of \( I_B/A_c \) (at \( V_{be} = 0.7 \) V) versus \( A_e/A_c \).

In Fig. 2.9 a plot is made of \( S_{I/B} \) versus \( A_e/A_c \). The solid lines represent the curves calculated with (2.14) using the above values for \( \tau_e \) and \( \tau_c \).

Fig. 2.8. A plot of \( I_B/A_c \) (at \( V_{be} = 0.7 \) V) versus \( A_e/A_c \).

Fig. 2.9. A plot of \( S_{I/B} \) measured at 1 Hz versus \( A_e/A_c \).
The Hooge parameter $\alpha$ is $3 \cdot 10^{-8}$ for wafer 1 and $5 \cdot 10^{-8}$ for wafer 2. These $\alpha$-values are rather low, but not exceptional for BJTs. The model gives fair agreement for the experimental results from transistors with large emitter areas. It is no more accurate for small emitter areas, i.e. where $A_e \geq 0.1A_E$.

A few remarks should be made

1) We assumed the Hooge parameter $\alpha$ to be constant in the whole emitter. However, it cannot be excluded that the parameter $\alpha$ is position dependent, i.e. $\alpha_e \neq \alpha_c$.

2) We assumed that the carrier lifetime at the emitter edge is shorter than in the central part. Furthermore, we supposed the effective lifetime to be the same both at the emitter edge parallel to the base contact and at the emitter edge near the oxide. The latter approximation needs some refinements.

C. Refined model

In Fig. 2.8, we observe that the measured data at $A_e/A_c = 0.06$ (transistor 5008) and $A_e/A_c = 0.1$ (transistor 2590), indicated with arrows, are systematically below the solid line. Transistor 5008 has a large $H_e/L_e$ ratio and transistor 2590 a large $L_e/H_e$ ratio. This implies that both transistors have a large $P/A_E$ ratio. Presumably we made an overestimation of the emitter edge area $A_e$ for transistors with a large emitter perimeter-to-area ratio. On the basis of these deviations we assume the following $\tau$ distribution: the carrier lifetime $\tau_c$ is constant in the whole central part of the emitter, but decreases rapidly when one approaches the four corner areas of the emitter. A model for this is given in Fig. 2.7b. In the central white part we have $\tau_p = \tau_c$ and in the shaded corners the effective lifetimes $\tau_e$ and $\tau_e^\ast$. The values of the lengths $p$ and $q$ are chosen to obtain the best fit to a straight line of all the measured data in Fig. 2.8, using the same values for $l$ and $\tau_e$ as in the previous section. The value of $p$ proves to be larger than $q$ so that the region with the low $\tau_e$ mainly extends over the emitter edge parallel to the base contacts. Applying this refinement to Fig. 2.9 results in a shift to smaller $A_e/A_c$ values for the points representing transistors with a large emitter perimeter, and in a better agreement between experimental results and calculated curves.

Since the $1/f$ noise is very sensitive to the value of the carrier lifetime, the $1/f$ noise is mainly generated in the four corner areas of the emitter. This can be checked against the experimental results. For the current we have

$$I_B = C_0 \int \frac{dA}{A_E \tau^{1/2}(r)} = C_0 A_E \cdot \langle 1/\tau^{1/2} \rangle_{A_E}$$

(2.17)

and for the $1/f$ noise

$$S_{I_B} = \frac{\alpha q}{4f} \int \frac{C_0 dA}{A_E \tau^{3/2}(r)} = \frac{\alpha q C_0 A_E}{4f} \cdot \langle 1/\tau^{3/2} \rangle_{A_E} = \frac{\alpha q I_B \cdot \langle 1/\tau^{3/2} \rangle_{A_E}}{4f} \cdot \langle 1/\tau^{1/2} \rangle_{A_E}$$

(2.18)

hence
\[ \frac{S_{I_b}}{I_B} = \frac{\alpha q}{4f} \left( \frac{1/\tau^{3/2}}{1/\tau^{1/2}} \right) \frac{A_E}{A_E} \]  \hspace{1cm} (2.19)

From Fig. 2.2 and (2.17) we obtain the emitter area dependence of \( \left( \frac{1}{\tau^{1/2}} \right)_A \)

From Fig. 2.6 and (2.19) we obtain the emitter area dependence of \( \left( \frac{\tau^{-3/2}}{A_E} \right) \left/ \left( \frac{\tau^{-1/2}}{A_E} \right) \right. \). Multiplying the values of \( I_B/A_E \) from Fig. 2.2 with the values of \( S_{I_b}/I_B \) from Fig. 2.6 yields \( S_{I_b}/A_E \) at constant \( V_{be} \). In Fig. 2.10 we have plotted \( S_{I_b}/A_E \) at \( V_{be} = 0.7 \) V versus \( A_E \).

From this plot we get the emitter area dependence of \( \left( \frac{1}{\tau^{3/2}} \right) \). We observe that \( S_{I_b}/A_E \) at constant \( V_{be} \) is proportional to \( 1/A_E \) for small emitter areas. For large emitter areas \( S_{I_b}/A_E \) at constant \( V_{be} \) tends to be constant. This leads to the conclusion that \( S_{I_b} \) at \( V_{be} = \text{cst.} \) consists of two contributions. One contribution is emitter area independent. So it can only be generated in the four very small corner areas of the emitter. A second contribution is proportional to the emitter area and is generated in \( A_c \) with carrier lifetime \( \tau_c \). Thus

\[ \frac{S_{I_b}}{A_E} \bigg|_{V_{be} = \text{cst.}} \propto \left( \frac{1}{\tau^{3/2}} \right) \frac{A_E}{A_E} = \frac{A_e^*}{\tau_e^{3/2}} \frac{1}{A_E} + \frac{1}{\tau_c^{3/2}} \]  \hspace{1cm} (2.20)

Here \( A_e^* \) represents the corner areas with effective lifetime \( \tau_e^* \). In Fig. 2.10 we observe that for large emitter areas \( S_{I_b}/A_E = 3 \times 10^{-20} A^2 \mu m^{-2} s \) for wafer 1 and
\[ S_{lb}/A_E = 6 \cdot 10^{-20} \text{A}^2\text{um}^{-2}\text{s} \] for wafer 2. From Fig. 2.2 and (2.17) we find \( C_0 = 1.2 \cdot 10^{-7} \) A\text{um}^{-2}\text{s}^{1/2} for both wafers. With the help of (2.18) and (2.20) we deduce \( \alpha = 10^{-7} \).

### 2.4 CURRENT CROWDING

When emitter-base current crowding occurs, i.e. when \( I_B > kT/qrbb \) with \( r_{bb} \) being the pinched-base resistance, the current is forced to flow through the emitter edge area that generates more 1/f noise per unit of current than the central part. So we expect that \( S_{lb} \propto I_B^\delta \), with \( \delta \) being a function of \( I_B \) and \( \delta \geq 1 \). In order to calculate \( S_{lb} \) as a function of \( I_B \), we calculate the current distribution in the emitter when current crowding is apparent. In this calculation we neglect current crowding within the corner areas \( A_e^* \). Furthermore, we assume that the current density is homogeneous over the emitter area except area \( A_e^* \) for sufficiently low \( V_{be} \), where current crowding is still negligible.

For transistors with a single base contact the base-emitter current \( I(x) \) at a distance \( x \) from the emitter edge is given by [8] (see Fig. 2.11)

\[
I(x) = I_{Be} \frac{\tan[Z(1-x/H_e)]}{\tan Z} = \frac{1}{2} \frac{H_e}{L_e} \rho_{sh} qI_{Be} \frac{kT}{l_{BB}}
\]

where \( \rho_{sh} \) is the base sheet resistance, and \( I_{Be} \) the base current at \( x = 0 \).

![Fig. 2.11. Geometry of the pinched base region of a transistor with a single base contact](image)

The base-emitter current density at \( x \) is

\[
J(x) = -\frac{1}{L_e} \frac{d}{dx} I(x) = \frac{ZI_{Be}}{A_e \tan Z \cos^2 Z(1-x/H_e)}
\]
\[ J(0) = J_{Be0} \exp \left( \frac{qV(0)}{kT} \right) = \frac{I_{Be}}{A_c} \frac{2Z}{\sin(2Z)} \]  

\[ V(0) = \frac{kT}{q} \ln \left( \frac{I_{Be}}{J_{Be0}A_c} \frac{2Z}{\sin(2Z)} \right) \]  

(2.23)

where \( J_{Be0} \) is the reverse leakage current density in the central part of the emitter. The current density in the emitter edge is

\[ J_{Be} = J_{Be0} \exp \left( \frac{qV(0)}{kT} \right) = \frac{J_{Be0}I_{Be}}{J_{Be0}A_c} \frac{2Z}{\sin(2Z)} \]  

(2.24)

where \( J_{Be0} \) is the reverse leakage current density in the edges of the emitter. The total base current is given by

\[ I_B = I_{Be} + I_{Be} = I_{Be} \left( 1 + \frac{J_{Be0}A_e^*}{J_{Be0}A_c} \frac{2Z}{\sin(2Z)} \right) \]  

(2.25)

\[ S_{I_B} \] as a function of \( I_B \) is given by the following relation

\[ S_{I_B} = S_{I_{Be}} + S_{I_{Be}} = \frac{aq}{4f} \left[ \frac{I_{Be}}{\tau_e^*} + \frac{I_{Be}}{\tau_c} \right] = \frac{aqI_B}{4f} \frac{K \tau_c/\tau_e^* + 1}{K + 1} \]  

(2.26)

with \( K = \frac{J_{Be0}A_e^*}{J_{Be0}A_c} \frac{2Z}{\sin(2Z)} \)

In Fig. 2.12 an example is given of \( S_{I_B} \) versus \( I_B \) of a transistor showing a clear influence of current crowding.

The solid line is calculated using (2.26) with the previously obtained values of \( \tau_c \) and \( \alpha \). After curve fitting we obtained \( \tau_e^* = 1.6 \times 10^{-12} \) s, and \( K (Z \downarrow 0) = 0.025 \). At low currents where current crowding is negligible, the value of \( S_{I_B}/I_B \) using the above mentioned parameters is \( 6 \times 10^{-17} \) A/Hz.

### 2.5 Conclusions

The dc I-V characteristics and the low-frequency noise of BJTs, made by Philips Electronics, were studied. The main 1/f noise generator is the 1/f noise in the base current \( S_{I_B} \). Both the base current density at a constant base-emitter voltage, and the 1/f noise turned out to depend on the emitter geometry. The emitter geometry dependence of the current density at a constant base-emitter voltage can be explained in terms of a position-dependent minority carrier lifetime. Assuming mobility fluctuations to be the source of the 1/f noise, a distributed minority carrier lifetime can also explain the observed emitter geometry dependence of the 1/f noise. A model was made that divides the emitter in two parts: a central part and an edge area around the emitter with a lower (effective) minority carrier lifetime than the central part. This model is in fair agreement with the experimental results for large
Conclusions

Fig. 2.12. Typical example of a transistor showing the influence of current crowding (5008 wafer 1, $A_E = 49.8 \times 4 \text{ µm}^2$).

emitter areas. Better agreement with the experimental results can be obtained by assuming that the minority carrier lifetime is the shortest in the four corners areas of the emitter. With this refinement the model can also explain the anomalous current dependence of $S_{f_b}$ when emitter current crowding occurs.

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References

Chapter 2. On $1/f$ noise in BJTs: influence of emitter geometry ...
Chapter 3

LOW-FREQUENCY NOISE IN POLYSILICON-EMITTER BIPOLAR TRANSISTORS
Low-Frequency Noise in Polysilicon Emitter Bipolar Transistors

H. A. W. Markus and T. G. M. Kleinpenning

Abstract—The low-frequency noise in polysilicon emitter bipolar transistors is investigated. Transistors with various geometries and various properties of the oxide layer at the monosilicon-polysilicon interface are studied. The main 1/f noise source proved to be located in the oxide layer. This source causes both 1/f noise in the base current $S_{1f}$ and 1/f noise in the emitter series resistance $S_{r}$. The magnitude of the 1/f noise source depends on the properties of the oxide layer. The 1/f noise is ascribed to barrier height fluctuations of the oxide layer resulting in transparency fluctuations for both minority and majority carriers in the emitter, giving rise to $S_{1f}$ and $S_{r}$, respectively. It is also shown that a low transparency of the oxide layer also reduces the contribution of mobility fluctuations to $S_{1f}$.

I. INTRODUCTION

In recent papers the 1/f noise in bipolar junction transistors (BJT) with a conventional emitter is mainly discussed in terms of mobility fluctuations. The 1/f noise in BJTs has been interpreted in terms of two 1/f noise current generators: $S_{1f}$ between emitter and base, and $S_{r}$ between emitter and collector. In practical cases the base-collector junction is reverse biased, so that the leakage base-collector current is small and its noise negligible. Recently, Kleinpenning [1] derived formulas for the low-frequency noise in BJTs incorporating the noise sources present in the parasitic series resistances.

Several authors have studied the low-frequency noise in polysilicon emitter BJTs [1]-[6]. The low-frequency noise always consists of white shot noise and 1/f noise. Sometimes burst noise is observed. Kleinpenning [1] found that the 1/f noise was located in the base current $S_{1f}$, and that its spectral density was proportional to the base current $I_{B}$. He interpreted the 1/f noise in terms of mobility fluctuations. Pong-Fei Lu [2] also found the 1/f noise to be located in the base current, but he found $S_{1f} \sim I_{B}^2$. Pawlikiewicz et al. [3] found $S_{1f} \sim I_{B}^2$ at higher currents and $S_{1f} \sim I_{B}$ at lower currents. Siabi-Shahrivar et al. [4] and Mounib et al. [5] showed that the 1/f noise is strongly related to the surface treatment prior to polysilicon deposition. Wai Shing Lau et al. [6] found $S_{1f} \sim I_{B}^2$. They suggested that transparency fluctuations of the oxide layer, present at the monosilicon-polysilicon interface, or two-step tunnelling via traps in the oxide is responsible for the observed 1/f noise. However, they did not give a detailed quantitative analysis.

This paper will deal with the location of the main 1/f noise source in polysilicon emitter BJTs with an oxide layer at the monosilicon-polysilicon interface. A model based on transparency fluctuations of the oxide layer, that can describe this noise source, will be presented. By means of this model, it will be shown that the contribution of the mobility fluctuations to $S_{1f}$ is overruled by transparency fluctuations.

II. EXPERIMENTAL RESULTS

A. Devices

The transistors are made by Philips Electronics. Transistors from 7 wafers were studied. On each wafer a set of transistors with various geometries is present. The length of the emitter (perpendicular to the base current) is in the range of $0.8 \mu m < L < 100 \mu m$, and its width (parallel to the base current) in the range of $0.3 \mu m < W < 100 \mu m$. For transistors from four wafers a HF dip is used to produce a native oxides layers at the polysilicon- monosilicon interface with an estimated thickness in the range of 10–15 Å. This native layer was removed from the other three wafers by a HF/H2O vapor etch in a cluster tool and, subsequently, a new layer was thermally grown with different oxidation times. The average thicknesses of the oxide layers given by the manufacturer are 3.8 Å, 7.5 Å and 8 Å, respectively. The emitter drive-in is a furnace anneal at 1173 K during 30 minutes. The top-doping of the emitter of all transistors is estimated to be $10^{20} \text{cm}^{-3}$. The junction depth is in the range of 57–71 nm. Only n-p-n type transistors made with this process were available.

B. I-V Characteristics

Fig. 1 shows a typical I-V curve of the base and collector current versus $V_{BE}$ at $V_{CB} = 3 \text{ V}$. The ideality factor for the base and collector current is 1. The current gain $\beta$ collapses for high currents, which is ascribed to high injection in the base. Current crowding is negligible in the studied current range.

With the help of white noise measurements in common-collector configuration [1], we found the values of $4kT(r_{e} + r_{b})$. From the deviation of the exponential behaviour of the I-V characteristics, we found $I_{EB} = I_{EB}$. Hence, the values of the emitter series resistance $r_{e}$ and the internal base resistance $r_{b}$ can be determined. The values found for $r_{b}$ agree well with the calculated values of the sum of the base sheet resistance given by the manufacturer, and the resistance between base contacts and emitter edge. At high currents the base sheet resistance can become bias dependent due to current crowding and high
injection. However, an important part of the base resistance is formed by the resistance between the base contacts and the emitter edge. As a result we expect the base resistance to be only weakly bias dependent in the studied current range. Our experimentally obtained I-V characteristic can be interpreted satisfactorily with a constant base resistance. The value of \( r_e \) depends on the emitter geometry and the oxide thickness, so it is obvious that the tunnel resistance of the oxide layer is an important part of the total emitter resistance. The experimentally obtained product of the emitter series resistance times the emitter area of \( 0.3 \times 45 \mu m^2 \). The grown oxide-layer thickness is 8 Å.

We made the noise measurements by putting the transistor in a circuit as shown in Fig. 2. The internal series resistances are given by \( R_b \), \( R_a \), and \( R_c \) respectively. Three external metal film resistors \( R_b \), \( R_c \), and \( R_E \) can be inserted which only have Nyquist noise (4kT/R). According to Kleinpenning [1], the 1/f voltage noise across \( R_E \) and \( R_C \) can be written as

\[
\left( \frac{Z}{R_E} \right)^2 V_{BE} = [r_e - \beta (r_b + R_B)]^2 S_{l_e} + [r_e + r_b + R_B]^2 S_{l_b} + (\beta + 1)^2 [S_{b} + S_{c} + S_{a}].
\]

(1)

\[
\left( \frac{Z}{R_C} \right)^2 V_{CE} = \beta^2 [r_e + R_B + r_a + R_E]^2 S_{l_e} + [r_e + r_b + R_B + r_a + R_E]^2 S_{l_b} + \beta^2 [S_{b} + S_{c} + S_{a}].
\]

(2)

with

\[
Z = r_b + R_B + r_a + (\beta + 1) (r_e + R_E)
\]

(3)

\[
r_e = \frac{dV_{BE}}{dR_B}
\]

(4)

\[
\beta = \frac{dI_C}{dI_B} = g_m c r_e
\]

(5)

where, \( g_m \) represents the collector transconductance, \( \beta \) the current amplification factor, and \( r_e \) the junction differential resistance of the intrinsic transistor. \( V_{BE} \) is the voltage drop across the emitter-base junction. \( S_{l_e} \) and \( S_{l_b} \) represent the 1/f current noise spectral density at constant \( V_{BE} \) in the base and collector currents, respectively. The series resistances \( r_e \) and \( r_b \) have 1/f resistance noise. Their spectral densities are represented by \( S_{l_e} \) and \( S_{l_b} \), respectively. The Early effect was ignored in the derivation of (1) and (2). This is permissible since \( I_C \) was found to be almost independent of \( V_{CE} > 1 \).  

In order to locate and characterize the 1/f noise sources, we carried out our measurements in both a common-emitter (C-E) configuration and a common-collector (C-C) configuration at various biasing conditions.

In the C-E configuration we took \( R_E \gg r_e, r_b, r_a, R_B \), so that \( Z/R_E = \beta + 1 \), and \( R_C = 0 \). Thus, (1) simplifies to

\[
g_m c V_{BE} = [1 - g_m c (r_e + R_B)]^2 S_{l_e} + [1 + (r_b + R_B)/r_e]^2 S_{l_b} + g_m c^2 [S_{b} + S_{c} + S_{a}].
\]

(6)

Here, \( g_m = (\beta + 1)/r_e = dI_C/dV_{BE} \) is the emitter transconductance of the intrinsic transistor. 

In the C-C configuration we put \( R_E = 0, R_B \gg r_b, r_a, (\beta + 1)/r_e \), and \( R_C = 100 \Omega \), so that \( Z = R_B \). Then, (2) reduces to

\[
S_{V_{CE}}/R_C^2 = \beta^2 S_{l_e} + S_{l_b} + (\beta/R_B)^2 [S_b + S_c + S_a].
\]

(7)

The noise measurements were performed in the current ranges \( 0.1 \mu A \leq I_B \leq 100 \mu A \) and \( 10 \mu A \leq I_C \leq 10 mA \). In these current ranges the input resistance \( r_e = kT/Q_B \) varies from 250 kΩ to 250 kΩ, the collector transconductance \( g_m c = Q_C/Q_B \) from \( 4 \times 10^{-4} \Omega^{-1} \) to \( 4 \times 10^{4} \Omega^{-1} \), and the emitter transconductance \( g_m = g_m c + 1/r_e \) from \( 4 \times 10^{-4} \Omega^{-1} \) to 0.4 Ω⁻¹. These parameters, being the parameters of the transistor without series resistances, are different from those of the complete transistor that are defined by \( dV_{BE}/dI_B, dI_C/dV_{BE} \), and \( dI_E/dV_{BE} \), respectively, with \( V_{BE} = V_{be} + I_B r_b + I_C r_c \). 

Spectral noise densities were measured from 1 Hz to 100 kHz. All devices showed 1/f noise. The 1/f spectral density was observed over at least one decade of frequency, but depending on emitter geometry and current reaching up to 5 decades of frequency. Using (6) and (7), we can determine the location of the dominant noise sources. In (6) both \( S_{l_e} \) and \( S_{l_b} \) have a prefactor of 1 at low currents, where \( g_m c (r_e + R_B) \ll 1 \) and \( (r_b + R_B)/r_e \ll 1 \). However in (7) the contribution of \( S_{l_b} \) only is amplified by a factor \( \beta^2 \). In (6) the noise contribution
of the series resistances $S_{r_e}$ and $S_{r_b}$ is amplified by a factor $\beta^2$, whereas in (7) it is only amplified by $(\beta/R_B)^2$. Hence, by measuring both in the C-E and C-C configuration at various values of $V_{be}$ and $R_B$, one can decide whether $S_{r_b}$ or $S_{r_e}$, or the contribution of the series resistances is dominant. Our measurements revealed that $S_{r_b}$ and $S_{r_e}$ are dominant.

In Fig. 3 some typical plots are presented of the spectral density of the base current $1/f$ noise $S_{I_B}$ at 1 Hz versus $I_B$. The results presented were obtained from transistors with a grown oxide layer of 7.5 Å and various emitter areas. One can observe that $S_{I_B} \approx I_B^2$. Only the transistors with a large emitter area show a deviation from this square law at low currents.

In Fig. 4 the relative noise $S_{I_B}/I_B^2$ from the same devices is plotted versus the emitter area $A_E$. One can observe that $S_{I_B}/I_B^2 \approx A_E^{-3}$.

In Fig. 5 the relative noise $S_{I_B}/I_B^2$ from the transistors with grown oxide layers and an emitter area of $8.8 \times 48 \, \mu$m$^2$ is plotted versus the oxide thickness. One can observe a clear influence of the oxide layer thickness on the $1/f$ base current noise.

The contribution of resistance fluctuations of the parasitic emitter and base resistance can be measured in the C-C configuration. By taking $R_B = 0$ we can approximate expression (6) for high currents, where $I_C \gg kT/qn_b$, by

$$S_{V_E} \approx r_2^2 S_{I_B} + I_B^2 S_{r_e} + I_B^2 S_{r_b}. \tag{8}$$

For transistors with a small emitter area, the $S_{V_E}$ measured was up to 3 orders of magnitude higher than $r_2^2 S_{I_B}$. Here, the values of $S_{I_B}$ were used that were measured in the C-E configuration. So, at high currents $S_{V_E}$ is determined either by base resistance fluctuations or by emitter resistance fluctuations. In Section IV we will discuss this in more detail.

A. General Remarks

Suppose one finds $S_{I_B} \sim I_B^k$ experimentally. If the current density, $J_B$, is homogeneously distributed over the emitter area and the noise sources are also homogeneously distributed over the emitter area and are spatially uncorrelated, then one can derive the following spectral noise density of $J_B$ [7]:

$$S_{J_B} \sim J_B^k = (I_B/A_E)^k$$

which leads to

$$S_{I_B} \sim A_E S_{J_B} = I_B \cdot A_E^{1-k}. \tag{9}$$

We found $S_{I_B} \sim I_B^k$ experimentally (see Fig. 3). As a result (9) predicts $S_{I_B}/I_B^2 \sim A_E^{-k}$ which agrees well with our experiments (see Fig. 4). This is a strong indication for homogeneously distributed $1/f$ noise sources.

In conventional p-n junctions the $1/f$ noise can be interpreted in terms of mobility fluctuations. The mobility fluctuation model [8] predicts a linear relationship between $S_{I_B}$ and $I_B$. However, we found $S_{I_B} \sim I_B^2$. As a consequence, our results cannot be explained in terms of mobility fluctuations.
only. A new model for $S_h \sim I_B^2$ will be presented in Section III-B.

In Fig. 3 we observe deviations from the square law for the larger emitter areas at small currents. In this region $S_h$ seems to be proportional to $I_B$, so that mobility fluctuations might be the dominant noise source here. In Section III-D, a relation will be derived for the contribution of mobility fluctuations to $S_h$, taking into account the influence of the oxide layer at the polysilicon-monosilicon interface.

A linear relation between $S_h$ and $I_B$ can also be found when the ideal base current dominates the base current and the non-ideal base current (with ideality factor 2) dominates the 1/f noise, provided that the 1/f noise is proportional to the non-ideal base current squared. Such a quadratic dependence is not predicted by the mobility fluctuation model.

B. Transparency Fluctuation Model

One of the 1/f model predicting $S = I^2$ is the tunnel diode model proposed by Kleinpenning [9], [10]. He assumed that the Nyquist noise of the insulator layer modulates the barrier height and hence the tunneling probability, or transparency, of carriers. He derived the following relation for the relative noise in the transparency, that is valid for a bias voltage much lower than the effective barrier height.

$$ \frac{S}{I^2} = \frac{2mkT^2}{3V_0h^2} \text{Re}(Z) \tan \theta \quad (10) $$

Here, $t$ is the transparency of the oxide layer, $m$ the effective mass of the carrier, $T$ the temperature, $L$ the thickness of the oxide layer, $V_0$ the barrier height, $C$ the capacitance of the oxide layer, $\text{Re}(Z)$ the real part of the impedance of the layer, and $\tan \theta$ the loss factor of the oxide.

Fluctuations of the barrier height of the oxide at the polysilicon-monosilicon interface results in fluctuations of the transparency of the barrier for the holes injected in the emitter, and so in base current fluctuations.

The following calculation yields the relation between the relative noise in the transparency, given by (10), and the relative noise in the short circuit base current. In Fig. 6 a schematic plot is given of the emitter structure of a polysilicon emitter.

$$ I = qAE \sqrt{\frac{kT}{2m^*_h T_p}} f_0[p(x_2) - p(x_1)]e^{-qV/kT}. \quad (14) $$

Here, $m^*_h$ is the effective mass of holes in the oxide, $f_0$ is the tunneling probability or transparency for holes and $V$ the voltage across the barrier.

For intermediate emitter currents where $V \ll kT/q$, (14) can be approximated by

$$ I = qAE s_{oxp} [p(x_1) - p(x_2)]. \quad (15) $$

Here, $s_{oxp}$ is the oxide recombination velocity of holes given by

$$ s_{oxp} = \sqrt{\frac{kT}{2m^*_h T_p}}. \quad (16) $$

Solving (11)–(13) and (15) for $I$ yields

$$ I = \frac{qAE}{s_{oxp} + s_m + W_m/T_m + W_p/T_p, \text{ with } s_{oxp}, \text{ and } s_m \text{ being the hole lifetime in the monosilicon and polysilicon layer, respectively, and provided that } s_{oxp} > W_m/T_m, s_m > W_m/T_m, \text{ and } s_m > W_p/T_p, \text{ with } s_{oxp}, \text{ and } s_m \text{ being the hole lifetime in the monosilicon and polysilicon layer, respectively, and provided that } s_{oxp} > W_m/T_m, s_m > W_m/T_m, \text{ and } s_m > W_p/T_p, \text{ with } s_{oxp}, \text{ and } s_m \text{ being the hole lifetime in the monosilicon and polysilicon layer, respectively, and provided that } s_{oxp} > W_m/T_m, s_m > W_m/T_m, \text{ and } s_m > W_p/T_p, \text{ with } s_{oxp}, \text{ and } s_m \text{ being the hole lifetime in the monosilicon and polysilicon layer, respectively, and provided that } s_{oxp} > W_m/T_m, s_m > W_m/T_m, \text{ and } s_m > W_p/T_p, \text{ with } s_{oxp}, \text{ and } s_m \text{ being the hole lifetime in the monosilicon and polysilicon layer, respectively, and provided that } s_{oxp} > W_m/T_m, s_m > W_m/T_m, \text{ and } s_m > W_p/T_p, \text{ with } s_{oxp}, \text{ and } s_m \text{ being the hole lifetime in the monosilicon and polysilicon layer, respectively, and provided that } s_{oxp} > W_m/T_m, s_m > W_m/T_m, \text{ and } s_m > W_p/T_p, \text{ with } s_{oxp}, \text{ and } s_m \text{ being the hole lifetime in the monosilicon and polysilicon layer, respectively, and provided that } s_{oxp} > W_m/T_m, s_m > W_m/T_m, \text{ and } s_m > W_p/T_p, \text{ with } s_{oxp}, \text{ and } s_m \text{ being the hole lifetime in the monosilicon and polysilicon layer, respectively, and provided that } s_{oxp} > W_m/T_m, s_m > W_m/T_m, \text{ and } s_m > W_p/T_p, \text{ with } s_{oxp}, \text{ and } s_m \text{ being the hole lifetime in the monosilicon and polysilicon layer, respectively, and provided that } s_{oxp} > W_m/T_m, s_m > W_m/T_m, \text{ and } s_m > W_p/T_p, \text{ with } s_{oxp}, \text{ and } s_m \text{ being the hole lifetime in the monosilicon and polysilicon layer, respectively, and provided that } s_{oxp} > W_m/T_m, s_m > W_m/T_m, \text{ and } s_m > W_p/T_p, \text{ with } s_{oxp}, \text{ and } s_m \text{ being the hole lifetime in the monosilicon and polysilicon layer, respectively, and provided that } s_{oxp} > W_m/T_m, s_m > W_m/T_m, \text{ and } s_m > W_p/T_p, \text{ with } s_{oxp}, \text{ and } s_m \text{ being the hole lifetime in the monosilicon and polysilicon layer, respectively, and provided that } s_{oxp} > W_m/T_m, s_m > W_m/T_m, \text{ and } s_m > W_p/T_p, \text{ with } s_{oxp}, \text{ and } s_m \text{ being the hole lifetime in the monosilicon and polysilicon layer, respectively, and provided that } s_{oxp} > W_m/T_m, s_m > W_m/T_m, \text{ and } s_m > W_p/T_p, \text{ with } s_{oxp}, \text{ and } s_m \text{ being the hole lifetime in the monosilicon and polysilicon layer, respectively, and provided that } s_{oxp} > W_m/T_m, s_m > W_m/T_m, \text{ and } s_m > W_p/T_p, \text{ with } s_{oxp}, \text{ and } s_m \text{ being the hole lifetime in the monosilicon and polysilicon layer, respectively, and provided that } s_{oxp} \begin{align*}
\frac{S_{oxp}}{\frac{S}{I^2}} &= \frac{S_{oxp}}{I^2} = \frac{2m^*_h qkT^2}{3V_0h^2}. \quad (19)
\end{align*}
Barrier height fluctuations of the oxide layer also modulate the tunneling probability, or transparency $\alpha$, for the majority carriers and hence generates 1/f noise in the emitter series resistance. For the barrier in the ohmic region, we have

$$S_{\alpha}/r_\alpha^2 = S_{\alpha}/r_e^2 \approx S_{\alpha}/r_e^2$$  \hspace{1cm} (20)

provided that the emitter resistance $r_e$ is determined by the tunnel resistance $r_\alpha$.

C. Two-Step Tunneling

In Section III.B we ascribed the 1/f noise to fluctuations in the barrier height of the oxide. Another explanation for the 1/f noise generated in the oxide layer is proposed by Kumar et al. [12]. They propose that two-step tunneling via traps in the oxide is responsible for the 1/f noise. They assume that the oxide contains electrically chargeable states which communicate with interface states by tunneling and have time constants dependent on the depth of the traps in oxide. Very specific requirements with respect to the trap distribution have to be met in order to obtain a 1/f spectrum. The current dependence is $S_I \propto I^2$. Application of this theory also yields reasonable results. Both theories predict a different dependence on the oxide layer thickness. However, the range of oxide layer thicknesses of our transistors is too small to distinguish between both theories.

D. Mobility Fluctuations

In the appendix the contribution of mobility fluctuations to $S_{\alpha}$ is calculated to be

$$S_{\alpha}(f) = \frac{\alpha m W_{m}^{[X]} \ln \left[ \frac{p(0)}{p(x_1)} \right] + \alpha \sigma_{\alpha} W_{p}^{[X]} \ln \left[ \frac{p(x_2)}{p(x_3)} \right]}{(W_{m} + W_{p} + \frac{1}{D_{m} + D_{p}} + \frac{1}{s_{\sigma_{\alpha}} + s_{m}})^2}.$$  \hspace{1cm} (21)

Here, $\alpha m$ and $\alpha \sigma_{\alpha}$ are the Hooge parameters of the monosilicon and polysilicon, respectively.

From the expressions (11)–(13) and (15), we can find the ratio $p(0)/p(x_1)$ and $p(x_2)/p(x_3)$ for $qV_{be} > kT$ being

$$p(0)/p(x_1) = 1 + \frac{W_{m}}{D_{m}} \left( \frac{1}{s_{\sigma_{\alpha}}} + \frac{1}{s_{m}} + \frac{1}{D_{p}} \right)^{-1}$$

and

$$p(x_2)/p(x_3) \approx 1 + \frac{s_{m} W_{p}}{D_{p}}.$$  \hspace{1cm} (22)

IV. DISCUSSION OF NOISE RESULTS

With the aid of (21) and (22) we are able to calculate the contribution of mobility fluctuations. For highly doped ($10^{20}$ cm$^{-3}$) silicon the diffusivity of holes is around 1 cm$^2$/s. The surface recombination velocity at the metal contact is in the order of $10^3$ cm/s. The hole recombination velocity at the oxide layer depends on its thickness. For a thickness of 7.5 Å–8 Å we take [13] $s_{\sigma_{\alpha}} \approx 3 \times 10^4$ cm/s and for 3.8 Å we take $s_{\sigma_{\alpha}} \approx 8 \times 10^4$ cm/s. We use $W_{m} \approx W_{p} \approx 0.1 \mu m$.

With $\alpha m = \alpha \sigma_{\alpha} = \alpha$, at $f = 1$ Hz we obtain $S_{\alpha} \approx 3 \cdot 10^{-11} a I_B$ for the total mobility fluctuation contribution. If we ascribe the deviations from the square law at low currents in Fig. 3 to mobility fluctuations, we obtain $\alpha$ values in the range of $10^{-6}$ to $10^{-1}$. These values are quite low. With the values of $s_{\sigma_{\alpha}}$ used here, the conditions $s_{\sigma_{\alpha}} \gg W_{m}/W_{p}$, and $s_{\sigma_{\alpha}} > W_{p}/r_{\alpha}$, that were used in the derivation of (17) and (21), are not entirely met. However, a numerical simulation of the base current density $J_B$, as a function of the oxide recombination velocity $s_{\sigma_{\alpha}}$, using a reasonable doping profile, given in Fig. 7, proved that recombination of holes in the emitter becomes the dominant current contribution for $s_{\sigma_{\alpha}} < 10^4$ cm/s. Hence, if no great accuracy is required, application of (17) and (21) is permissible for $s_{\sigma_{\alpha}} > 10^4$ cm/s and thus for oxide layers with a thickness of less than 13 Å [13].

From (17) it is obvious that the oxide recombination velocity $s_{\sigma_{\alpha}}$ is the current limiting factor, provided that $s_{\sigma_{\alpha}} \ll s_{m}, D_{m}/W_{m}, D_{p}/W_{p}$. In that case the influence of the mobility on the base current is weak. As a result, the 1/f noise caused by fluctuations in the mobility, which is found in the base current, is reduced. The contribution of transparency fluctuations can be calculated with (18). Using the data previously mentioned, we find $S_{\alpha}/I_B^2 \approx 0.3 \cdot S_{\sigma_{\alpha}}/I_B^2 = 0.3 \cdot s_{\sigma_{\alpha}}/I_B^2$ for 7.5 Å–8 Å oxide layer thickness and $S_{\alpha}/I_B^2 \approx 0.1 \cdot s_{\sigma_{\alpha}}/I_B^2$ for 3.8 Å thickness. With (10) we can calculate the loss factor $\Delta$ using $V_{be} = 1.1$ V, and $m_{e}^* = 0.42 m_0$, where $m_0$ is the electron rest mass. The capacitance of the oxide layer is given by

$$C = \varepsilon A E/L.$$  

By applying this to the experimental data at high currents, presented in Fig. 5, we obtain values for $\tan \delta$. We find $\tan \delta$ to be 4 for the transistors with 3.8 Å oxide layer, and 0.6 for transistors with 7.5 Å and 8 Å oxide layer. These values are rather high compared to the values reported in literature, that are of the order of $10^{-4}$ for quartz. However, the latter data are taken from bulk oxide material, whereas the oxide layers in our transistors only have thicknesses of a few atom layers.
Moreover, the thickness and structure of the layer may not be completely uniform over the emitter area and the layer may even be interrupted at some spots, causing difficulty in the evaluation of (10).

In the derivation of (10) image force was neglected. However, the image force reduces the effective barrier height significantly for very thin oxide layers, causing an increase in the 1/f noise. Thus, neglecting the image force leads to an overestimate of the \( \tan \delta \).

In Section II C we mentioned that the 1/f noise, measured in the C-C configuration at high currents, was either ascribed to base resistance fluctuations or emitter resistance fluctuations. The contribution of emitter resistance fluctuations is claimed to be dominant for two reasons.

1) With only base resistance fluctuations we find the Hooge 1/f noise parameter \( \alpha \) to be in the range of \( 10^{-2} \) to \( 10^{-1} \), which is quite high.

2) \( S_{V_2} \) depends on the oxide layer thickness at the polysilicon-mosilicon interface. \( S_{V_2} \) is independent of the oxide thickness.

The emitter series resistance consists of three parts, a part located in the monosilicon \( (r_m) \), in the oxide layer \( (r_{ox}) \), and in the polysilicon layer \( (r_p) \), thus

\[
r_s = r_m + r_{ox} + r_p.
\]

(23)

The same holds for the 1/f noise.

\[
S_{r_s} = S_{r_m} + S_{r_{ox}} + S_{r_p}.
\]

(24)

The contribution of the 1/f noise stemming from the monosilicon region was calculated using the Hooge relation [14].

\[
S_{r_m} = \alpha r_m^2 / f N_m.
\]

(25)

Here, \( N_m \) is the total number of major carriers in the monosilicon region.

De Graaff et al. [15] studied the 1/f noise in polysilicon resistors with a dopant concentration in the range of \( 10^{15} \text{ cm}^{-3} \) to \( 10^{20} \text{ cm}^{-3} \). Their theoretical model has been improved by Luo et al. [16]. They derived the following relation for the 1/f noise generated in the polysilicon.

\[
\frac{S_I}{f^2} = \frac{1}{N_{eff}} \left( \frac{\nu_c}{\nu_f} \right)^2 \frac{qd\alpha}{3ekT} \exp \left( \frac{q\Phi_B}{kT} \right).
\]

(26)

Here, \( N_{eff} \) is the effective number of large-barrier grains in the conduction path, \( \nu_c \) the emission velocity over a grain boundary barrier, given by \( (kT/2\pi m^*)^{1/2} \), \( \nu_f \) the diffusion velocity, \( d \) the depletion layer width, \( \alpha \) the Hooge parameter, \( A \) the cross section of the polysilicon material, and \( \Phi_B \) the grain boundary barrier height. For a dopant concentration of \( 10^{20} \text{ cm}^{-3} \) De Graaff et al. [15] found a barrier height \( \Phi_B \) of approximately 10 mV. They took \( \nu_c \approx 2\nu_f = 1/4\nu_{thermal} \). Applying (26) to the experiments of De Graaff et al. [15] yields an \( \alpha \) value in the order of \( 10^{-5} \cdot (N/N_{eff}) \), with \( N \) being the total number of grain boundaries in the conduction path. If we ascribe the measured noise in the emitter series resistance to the monosilicon region and apply (26), we obtain \( \alpha \) values in the order of \( 10^{-2} \cdot N_{eff} \). With a grain thickness of roughly 0.1 \( \mu \text{m} \) we get a value for \( N \) of about 5, and \( N_{eff} \leq 5 \), which leads to a discrepancy between our results and those of [15].

If we ascribe the measured 1/f noise to the monosilicon region only and apply (25), we obtain \( \alpha \) values in the range of \( 0.1 \leq \alpha \leq 1 \), which are very high. In all probability the primary 1/f noise source is located in the oxide layer.

In order to verify whether the measured 1/f noise in the emitter series resistance can be ascribed to transparency fluctuations as predicted by our model (20), we plotted \( S_{r_s}/r_s^2 \) versus \( S_{I_I}/I_0^2 \) for transistors with various oxide layer properties. Both \( S_{r_s}/r_s^2 \) given by (20) and \( S_{I_I}/I_0^2 \) given by (18) are proportional to the relative noise in the transparency. As a result the plot of \( S_{r_s}/r_s^2 \) versus \( S_{I_I}/I_0^2 \) has to be linear. The plot is given in Fig. 8. We observe that the plot is indeed linear.

A few remarks should be made.

1) \( S_{r_s}/r_s^2 \) is about factor 10 higher than \( S_{I_I}/I_0^2 \). This can be ascribed, first of all, to the prefactor \( (d\ln I_0/d\ln s_{oxP})^2 \) in (18), previously calculated to be 0.3 for the transistors presented in Fig. 8. Secondly, the effective oxide barrier height for holes (1.1 eV) is higher than for electrons (0.6 eV). From (10) we conclude that \( S_{r_s}/r_s^2 \) is smaller than \( S_{I_I}/I_0^2 \).

2) We note that the factor \( (d\ln I_0/d\ln s_{oxP})^2 \) in (18) depends on \( s_{oxP} \). Consequently, the plot in Fig. 8 is only expected to be linear for transistors with nearly the same value of \( s_{oxP} \), and thus for transistors with approximately the same oxide layer thickness. Since the emitter series resistance of the transistors presented in Fig. 8 have the same order of magnitude, it is assumed that all have about the same oxide layer thickness of nearly 8 \( \AA \).

3) Application of (20) is permissible provided that \( r_s \) is determined by \( r_m \). Therefore, we have to certify that this condition is satisfied. In the monosilicon region \( r_m A_E = \rho_m W_m \) is of the order of \( 10^{-1} \Omega \mu \text{m}^2 \). Here, \( \rho_m \) is the resistivity of the monosilicon. The product \( r_p A_E \) of the polysilicon region under low biasing...
conditions (i.e. \( V_p \ll kT/q \) where \( V_p \) is the voltage across a grain boundary) is given by [16]

\[
N_{em}kT/q^2 n(d) \exp \left( \frac{q\Phi_d}{kT} \right).
\]

(27)

Here, \( n(d) \) denotes the electron density in the quasi-neutral regions.

By substituting the values mentioned previously, we obtain a value for \( r_{\tau}A_E \) of the order of \( 10^{-11} \cdot N_{em} \Omega \mu m^2 \).

Comparison of both \( r_{\tau}A_E \) and \( r_{\tau}A_E \) with the values measured in the range of \( 43 \Omega \mu m^2 \) to \( 160 \Omega \mu m^2 \) reveals that \( r_e \approx r_{\tau} \). Hence, the emitter resistance is determined by the tunnel resistance and \( S_{re}/r_{re}^2 \approx S_{re}/r_{re}^2 \).

V. STRESS EXPERIMENTS

Application of a sufficiently high reverse bias voltage to a emitter-base junction leads to an increase in the non-ideal base current. Generally, this also leads to an increase in the noise generated in the emitter-base junction. Thus, when we apply a reverse bias to the transistors studied here, we only expect the noise produced in the emitter-base junction to increase. The noise produced in the oxide layer at the monosilicon-polysilicon interface should not change since the stress is applied to the emitter-base junction only. In Fig. 9 the noise in the base current \( S_{IB} \) is plotted versus \( I_B \), measured under different stress conditions. We observe that only the branch of the curves proportional to \( J^2 \) increases, whereas the branch of the curves proportional to \( I_B^2 \) is unchanged. These results confirm the existence of two different noise sources involved in the generation of \( S_{IB} \). The fact that application of stress does not affect the branch of \( S_{IB} \) proportional to \( I_B^2 \) agrees with our model.

VI. CONCLUSIONS

The \( 1/f \) noise of the polysilicon emitter bipolar transistors investigated in this study stems from noise in the base current \( S_{IB} \) and in the emitter series resistance \( S_{re} \). By considering the \( 1/f \) noise in \( S_{IB} \) as a function of the emitter geometry, we found that its \( 1/f \) noise sources are homogeneously distributed over the emitter area. The \( 1/f \) noise in \( S_{IB} \) and in \( S_{re} \) increases with the thickness of the oxide layer present at the monosilicon-polysilicon interface. Grown oxide layers show less noise in both \( S_{IB} \) and \( S_{re} \) than native oxide layers.

The \( 1/f \) noise in \( S_{IB} \) can be explained in terms of transparency fluctuations, due to barrier height fluctuations of the oxide layer barrier at the polysilicon-monosilicon interface. These transparency fluctuations also cause the \( 1/f \) noise in the emitter series resistance. Strong support for our model can be found in the fact that both \( S_{IB} \) and \( S_{re} \) have the same dependence on the oxide layer properties.

Due to the low transparency of the oxide layer, the base current is almost independent of the diffusivity of minority carriers in the emitter. Thus the contribution of diffusivity (mobility) fluctuations to \( S_{IB} \) in the monosilicon region and the polysilicon region is reduced.

ACKNOWLEDGMENT

The transistors were manufactured by Philips Research Laboratories. The authors would like to thank Dr. G. A. M. Hurks and J. de Boet, staff members of Philips, for providing the transistors and for their close cooperation.

APPENDIX

RELATION FOR THE CONTRIBUTION OF MOBILITY FLUCTUATIONS TO \( S_{IB} \)

By means of (11)-(15) the current fluctuations around the steady-state due to diffusivity fluctuations are found to be

\[
\Delta I(x, t) = \frac{I}{D_{m,p}} \Delta D_{m,p}(x, t) - qAD_{m,p} \frac{\Delta p(x, t)}{dt}
\]

(A1)

\[
\Delta I(x, t) = q \lambda_{m,p} \Delta p(x, t)
\]

(A2)

and

\[
\Delta I(x, t) = \Delta I(x, t) = q \lambda_{m,p} \Delta p(x, t) - \Delta p(x, t).
\]

(A3)

Integrating (A1) over the monosilicon and polysilicon region yields

\[
\Delta I(t) = \frac{1}{W_p} \int_0^{x_p} \Delta D_{m,p}(x, t) dx - qA \frac{D_{m,p}}{W_p} \Delta p(x, t)
\]

(A4)

and thus

\[
\Delta I(t) = \frac{1}{W_p} \int_0^{x_p} \Delta D_{m,p}(x, t) dx - qA \frac{D_{m,p}}{W_p} \Delta p(x, t)
\]

(A5)

If the junction is short circuited, \( p(0) \) does not fluctuate, thus \( \Delta p(0, t) = 0 \). With the help of (A2) the fluctuation...
\( \Delta p(x_3, t) \) in (A5) can be expressed in terms of \( \Delta I(t) \). With \( \Delta \) the fluctuation \( \Delta p(x_3, t) \) in (A5) can be expressed in \( \Delta p(x_1, t) \). Now (A5) consists of two equations with two unknown parameters: \( \Delta p(x_1, t) \) and \( \Delta I(t) \). For \( \Delta I(t) \) we obtain

\[
\Delta I(t) = \frac{I}{D_m} \int_0^t \frac{\Delta D_m(x, t)}{D_m} dx + \frac{I}{D_p} \int_0^t \frac{\Delta D_p(x, t)}{D_p} dx.
\]

(A6)

By making a Fourier transform, and using the cross-correlation spectral noise density in the diffusivity, given by [14]

\[
S_D(x, x', f) = \frac{\alpha D^2}{fA p(x)} \delta(x - x')
\]

with \( \alpha \) the Hooge parameter, and \( \delta \) the Dirac delta function, we obtain (21).

REFERENCES

ON THE 1/f NOISE IN POLYSILICON-EMITTER BIPOLAR TRANSISTORS: COHERENCE BETWEEN BASE CURRENT NOISE AND EMITTER SERIES RESISTANCE NOISE

Abstract - The 1/f noise in polysilicon-emitter bipolar transistors is investigated. The main 1/f noise source was found to be located in the oxide layer. This source causes both 1/f noise in the base current $S_Ib$ and 1/f noise in the emitter series resistance $S_{re}$. The 1/f noise is ascribed to barrier height fluctuations of the oxide layer resulting in transparency fluctuations for both minority and majority carriers in the emitter, giving rise to $S_Ib$ and $S_{re}$, respectively. This model predicts that $S_Ib$ and $S_{re}$ are fully correlated. Our experimental results show a correlation factor in the range of 0.3 to 0.5. The deviation from full correlation is ascribed to local inhomogeneities in the oxide layer.

I INTRODUCTION

Several authors have studied the low-frequency noise in polysilicon-emitter BJTs [1-7]. The low-frequency noise always consists of white shot noise and 1/f noise. Sometimes burst noise is observed. Kleinpenning [1] found that the 1/f noise was located in the base current $S_Ib$ and that its spectral density was proportional to the base current $I_B$. He interpreted the 1/f noise in terms of mobility fluctuations. Pong-Fei Lu [2] also found the 1/f noise to be located in the base current, but he found $S_Ib \propto I_B^2$. Pawlikiewicz et al. [3] found $S_Ib \propto I_B^2$ at higher currents and $S_Ib \propto I_B$ at lower currents. Siabi-Shahrivar et al. [4] and Mounib et al. [5] showed that the 1/f noise is strongly related to the surface treatment prior to polysilicon deposition. Wai Shing Lau et al. [6] found $S_Ib \propto I_B^2$. They suggested that transparency fluctuations of the oxide layer, present at the monosilicon-polysilicon interface, or two-step tunneling via traps in the oxide is responsible for the observed 1/f noise. However, they did not give a detailed quantitative analysis. Recently, a study of the 1/f noise in polysilicon-emitter bipolar transistors was published in a paper by Markus and Kleinpenning [7]. It was found that the dominant 1/f noise generators are the base current noise $S_Ib$ and the emitter series resistance noise $S_{re}$. At high currents the 1/f noise in the base current was proportional to the base current squared, i.e. $S_Ib \propto I_B^2$. Only at low currents it was proportional to $I_B$. The latter was ascribed to mobility fluctuations. A model for the high current regime was proposed that assumes that the fluctuations of the barrier height of the oxide layer, present at the monosilicon-polysilicon interface, lead to fluctuations of the tunneling probability, or transparency, for holes and electrons. The transparency fluctuations give rise to
fluctuations in the base current and in the emitter series resistance. The spectral density of the fluctuations has a $1/f$ frequency dependence. Since the bandgap of the oxide layer is constant, we expect that the fluctuations of the transparency for holes and electrons are correlated and thus that the base current noise (at high currents) and the emitter series resistance noise are correlated.

The experimental fact that most strongly supports the proposed model, as discussed in ref. [7], is given in Fig. 1. In this figure the relative $1/f$ noise in the emitter series resistance is plotted versus the relative $1/f$ noise in the base current. Results are presented for transistors having different oxide layer properties. We observe that both $1/f$ noise generators have a similar dependence on the oxide layer properties. However, from Fig. 1 we cannot conclude that both noise generators are correlated. For instance we can have two independent (i.e. uncorrelated) noise sources located in the oxide layer, whose spectral densities have a similar dependence on the oxide properties.

The transparency fluctuation model predicts full correlation between both noise generators. Absence of this correlation implies that the results cannot be interpreted in terms of the transparency fluctuation model.

The purpose of the work presented in this paper is to obtain experimental evidence for the correlation between $1/f$ noise in the base current and $1/f$ noise in the emitter series resistance.

![Graph](image)

**Fig. 1** Relative $1/f$ noise in the emitter series resistance versus the relative $1/f$ noise in the base current. $A_E$ is the emitter area. Details on the devices are given in section II.

### II Devices

The transistors are made by Philips Electronics. The oxide layer at the polysilicon-monosilicon interface was removed using a HF/H$_2$O vapour etch in a cluster tool. A new layer was grown thermally. According to the manufacturer the average
thickness of this layer is 7.5 Å and 8 Å. We studied two devices with an emitter area of 0.3×48 µm² and two with an emitter area of 1.3×48 µm². With the help of the Gummel plots and the white noise measurements, we determined the values of the base series resistance, the emitter series resistance and the current gain. The results are presented in table 1. More details can be found in [7].

III Correlation Measurements

The correlation spectra were measured by putting the transistor in the circuit given in Fig. 2. The correlation spectral density was measured between the voltage fluctuations at the base contact and at the emitter contact. The formulae for the voltage fluctuations at the base and emitter contacts, taking only the 1/f fluctuations into account in the base current and in the emitter series resistance, are given by [1].

\[
\Delta V_B = \Delta I_B R_B = R_B \cdot \frac{[r_\pi + \beta (r_e + R_E)] \Delta I_{be} - I_E \Delta r_e}{Z}
\]

\[
\Delta V_E = \Delta I_E R_E = R_E \cdot \frac{[r_\pi - \beta (r_b + R_B)] \Delta I_{be} - (\beta + 1) I_E \Delta r_e}{Z}
\]

with \( Z = r_\pi + R_B + r_b + (\beta + 1)(R_E + r_e) \)

Here \( r_\pi = \partial V_{be}/\partial I_B \) is the dynamic input resistance, \( \beta \) is the dynamic current gain, \( \Delta I_{be} \) and \( \Delta r_e \) are the spontaneous 1/f fluctuations in the base current and in the emitter series resistance, respectively.

In our experiments we took \( R_E >> r_e, r_b, R_B, r_\pi \) so that \( Z = (\beta + 1)R_E \). For (1) we then obtain with \( \beta >> 1 \).

\[
\Delta V_B = R_B \Delta I_{be} - \frac{I_E R_B}{\beta R_E} \Delta r_e
\]

\[
\Delta V_E = \frac{[r_\pi - \beta (r_b + R_B)]}{\beta} \Delta I_{be} - I_E \Delta r_e
\]
The cross product can be approximated by

\[ \langle \Delta V_B \Delta V_E \rangle = R_B \left[ \frac{r \pi - \beta (r_b + R_B)}{\beta} \langle \Delta I_{be}^2 \rangle + \frac{I_E^2}{\beta R_E} \langle \Delta r_e^2 \rangle - I_E \langle \Delta I_{be} \Delta r_e \rangle \right] \]  

(3)

The values of \( \langle \Delta I_{be}^2 \rangle \) and \( \langle \Delta r_e^2 \rangle \) were measured as described in [7]. Assuming a correlation factor \( \Gamma \) between \( \Delta I_{be} \) and \( \Delta r_e \), i.e. \( \langle \Delta I_{be} \Delta r_e \rangle = \Gamma \sqrt{\langle \Delta I_{be}^2 \rangle \cdot \langle \Delta r_e^2 \rangle} \), we can calculate the three contributions of \( \langle \Delta I_{be}^2 \rangle \), \( \langle \Delta r_e^2 \rangle \), and \( \langle \Delta I_{be} \Delta r_e \rangle \) in (3). In Fig. 3 the absolute value of the sum of the contributions owing to \( \langle \Delta I_{be}^2 \rangle \) and \( \langle \Delta r_e^2 \rangle \), and the absolute value of the contribution owing to \( \langle \Delta I_{be} \Delta r_e \rangle \) with \( \Gamma = 1 \) are plotted versus \( I_E \) for a 1.3x48 \( \mu \)m² transistor. For the sake of readability of Fig. 3 the power spectral densities are divided by \( I_E^2 \).

From this plot we can determine the emitter current range where the contribution owing to \( \Delta I_{be} \Delta r_e \) can be dominant in (3), in this current range we have to perform the correlation measurement. From Fig. 3 we also have an impression of the detection limit of the correlation factor \( \Gamma \). In case of the transistor presented in Fig. 3 correlation factors of 0.1 and higher can be accurately detected in the emitter current range of \( 10^{-5} - 10^{-1} \) A.
With the help of Fig. 3 the emitter current range where the contribution owing to \(\langle \Delta I_{be} \Delta r_e \rangle\) is dominant can be determined graphically. For this emitter current range we want to have analytical expressions for the conditions to impose on the emitter current and on the values of the external resistances. If \(\Gamma = 1\) the cross product term in (3) is dominant if we choose in (2)

\[
|\Delta I_{be}| \gg \frac{I_E}{\beta R_E} |\Delta r_e| \\
\left| r_\pi - \beta (r_b + R_B) \right| |\Delta I_{be}| \ll I_E |\Delta r_e|
\]

(4)

If these conditions are satisfied the equations (2,3) reduce to \(\Delta V_B = R_B \Delta I_{be}\), \(\Delta V_E = -I_E \Delta r_e\), and \(\langle \Delta V_B \Delta V_E \rangle = -R_B I_E \langle \Delta I_{be} \Delta r_e \rangle\), so that \(\langle \Delta I_{be}^2 \rangle\), \(\langle \Delta r_e^2 \rangle\), and \(\langle \Delta I_{be} \Delta r_e \rangle\) and thus \(\Gamma\) can be obtained directly from the measurement of \(\langle \Delta V_B^2 \rangle\), \(\langle \Delta V_E^2 \rangle\), and \(\langle \Delta V_B \Delta V_E \rangle\).

When \(\Delta r_e\) and \(\Delta I_{be}\) are fully correlated we have

\[
\frac{\Delta I_{be}}{I_B} = \gamma \frac{\Delta r_e}{r_e}
\]

(5)

Here, \(\gamma\) is a factor that can be determined from the ratio between the relative noise in the base current and the relative noise in the emitter series resistance. From the experimental results in Fig. 1 it is found that \(\gamma = 0.3\). The sign in (5) is positive because an increase in the barrier height for electrons is coupled to a decrease in the barrier height for holes. So, an increase in the emitter resistance is accompanied by an increase of the base current.

Substitution of (5) in (4) yields

\[
R_E \gg \frac{r_e I_E}{\gamma} \beta I_B \equiv \frac{r_e}{\gamma} \\
\left| r_\pi - \beta (r_b + R_B) \right| \ll \frac{r_e \beta I_E}{\gamma I_B} \equiv \beta^2 \frac{r_e}{\gamma}
\]

(6)

These conditions have to be satisfied to obtain

\[
\frac{\langle \Delta V_B \Delta V_E \rangle}{\sqrt{\langle \Delta V_B^2 \rangle \cdot \langle \Delta V_E^2 \rangle}} = \frac{R_B I_E \cdot \langle \Delta I_{be} \Delta r_e \rangle}{\sqrt{\langle R_B \Delta I_{be}^2 \rangle \cdot \langle I_E \Delta r_e^2 \rangle}} = \frac{\langle \Delta I_{be} \Delta r_e \rangle}{\sqrt{\langle \Delta I_{be}^2 \rangle \cdot \langle \Delta r_e^2 \rangle}} = \Gamma
\]

(7)

IV EXPERIMENTAL RESULTS AND DISCUSSION

With the transistor parameters given in table 1 it is possible to satisfy the conditions (6).
Experimental results and discussion

Table 1: Transistor parameters and correlation factor

<table>
<thead>
<tr>
<th>transistor</th>
<th>oxide thickness (Å)</th>
<th>$\beta$</th>
<th>$r_b$ (Ω)</th>
<th>$r_e$ (Ω)</th>
<th>$\Gamma$</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1 (0.3x48 µm²)</td>
<td>7.5</td>
<td>315</td>
<td>494</td>
<td>9</td>
<td>0.4</td>
</tr>
<tr>
<td>T2 (0.3x48 µm²)</td>
<td>8</td>
<td>530</td>
<td>410</td>
<td>11</td>
<td>0.3</td>
</tr>
<tr>
<td>T3 (1.3x48 µm²)</td>
<td>8</td>
<td>650</td>
<td>430</td>
<td>7</td>
<td>0.5</td>
</tr>
<tr>
<td>T3 (1.3x48 µm²)</td>
<td>7.5</td>
<td>330</td>
<td>433</td>
<td>3</td>
<td>0.4</td>
</tr>
</tbody>
</table>

We measured the correlation factor $\Gamma$ of all transistors at different biasing conditions. The correlation factor proved to be independent of the current, within the studied current range. The value of $\Gamma$ is given in table 1. The transparency fluctuation model predicts the value of $\Gamma$ to be one. If in addition to the transparency fluctuations there are contributions of other noise generators that do not lead to a correlated contribution to $S_{I_b}$ and $S_{re}$, we get a lower overall correlation factor. However, we found no experimental evidence for the presence of such an extra noise source, whose influence is large enough to account for the low correlation factor. At low currents we found a second 1/f noise source for $S_{I_b}$ that we ascribed to mobility fluctuations, but its contribution is negligible in the current range where we performed the correlation measurements.

If transparency fluctuations are the only noise source for both $S_{I_b}$ and $S_{re}$ we can explain the deviation from $\Gamma=1$ by supposing the presence of local inhomogeneities in the oxide layer.

In ref. [7] it was concluded that the 1/f noise sources were homogeneously distributed across the emitter area. This conclusion was based on the emitter area dependence of the 1/f noise in both base current and emitter series resistance. However this method can not show (local) inhomogeneities that could be present on a smaller scale than the smallest emitter area studied in [7], which is 1 µm².

In case of local inhomogeneities, parts of the emitter area contributing most to the measured base current 1/f noise do not necessarily coincide with the areas that contribute most to the emitter series resistance 1/f noise. As a result, even if there is full correlation between the local 1/f noise sources of the base current and emitter series resistance, one can get an overall correlation factor that is lower than one. In other words if the ratio between the relative noise in the base current and the relative noise in the emitter series resistance is position dependent, an overall correlation factor lower than one will be found.

Below we shall present arguments for local inhomogeneities and derive an expression for $\Gamma$. In order to find a physical explanation or origin for the local inhomogeneities we have to consider the expressions for $S_{I_b}$ and $S_{re}$ that were derived in [7].

$$\frac{S_{I_b}}{I_B^2} = \frac{1}{\sqrt{2\pi m_h^*} t_h} \left( \frac{1}{s_m} + \frac{W_m}{D_m} + \frac{W_p}{D_p} \right)^{-2} \cdot \frac{m_h^* k T L^3 \cdot \tan(\delta)}{3\pi e A_{E}V_{0h} k^2 f}$$ (8)
\[ S_{r_e} = \frac{m_e^* q k T L^3 \cdot \tan(\delta)}{r_e^2} \cdot \frac{3 \pi A E V_{0e, h} h^2 f}{9} \] (9)

Here, \( t_h \) is the tunneling probability for holes, \( s_m \) is the metal contact recombination velocity, \( W_{m,p} \) and \( D_{m,p} \) are the width and the diffusivity of holes in the monosilicon and polysilicon-emitter region, \( m_{e,h}^* \) is the effective mass of electrons and holes in the oxide, \( V_{0e,h} \) is the barrier height of the oxide for electrons and holes, \( L \) is the thickness of the oxide layer, \( A_E \) is the emitter area, and \( \tan(\delta) \) is the loss tangent of the oxide.

Possible inhomogeneities resulting in a position dependent relative 1/f noise in the base current and emitter series resistance are a position dependent band line-up between oxide and silicon, a position dependent barrier height (both through \( V_{0e,h} \) and \( t_h \)), and a position dependent oxide layer thickness (through \( t_h \)).

A calculation of the correlation factor of an inhomogeneous oxide layer is made in the Appendix. In this calculation we consider an inhomogeneous oxide layer that is modelled with two homogeneous parts with different properties. The resulting expression for \( \Gamma \) is

\[ \Gamma = \frac{1}{\sqrt{1 + \left( \frac{x y - 1}{\sqrt{x y + 1}} \right)^2}} \text{ with } x = \frac{\Delta I_{be1}^2}{\Delta I_{be2}^2}, \text{ and } y = \frac{\Delta r_{e2}^2}{\Delta r_{e1}^2} \cdot \frac{r_{e2}^4}{r_{e1}^4} \] (10)

Here, the indices 1 and 2 refer to the two different parts of the oxide area. A plot of \( \Gamma \) versus the parameters \( x \) and \( y \) is presented in Fig. 4.

![Fig. 4 Correlation factor \( \Gamma \) as a function of \((x,y)\).](image)

We observe that \( \Gamma \)-values in the range of 0.3-0.5 can only be obtained for limited areas in the \( x, y \) plane. It should be noted that (10) applies for the most elementary case of inhomogeneity. Stronger inhomogeneity leads to lower values of \( \Gamma \).
V CONCLUSIONS

The 1/f noise of polysilicon-emitter bipolar transistors with a continuous oxide layer can be explained in terms of transparency fluctuations of the oxide layer. These transparency fluctuations lead to base current fluctuations and emitter series resistance fluctuations. This model predicts that the fluctuations in the base current and the emitter series resistance are fully correlated. The correlation factor between the 1/f noise in the base current and the 1/f noise in the emitter series resistance was measured. Experimentally the correlation factor was found to be in the range 0.3-0.5. The fact that the correlation factor is smaller than one can be ascribed to local inhomogeneities in the oxide layer.

Appendix

COHERENCE IN AN INHOMOGENEOUS OXIDE LAYER

Let us suppose that we can model the local inhomogeneities by dividing the oxide into two parts. Each part is homogeneous and has full correlation between \( \Delta I_{be} \) and \( \Delta r_e \). The quantities in each part are referred to with an index 1 and 2. We have

\[ \Delta I_{be} = \Delta I_{be1} + \Delta I_{be2} \]  

(A1)

Since \( 1/r_e = 1/r_{e1} + 1/r_{e2} \) we obtain

\[ \Delta r_e = \left( \frac{r_e}{r_{e1}} \right)^2 \Delta r_{e1} + \left( \frac{r_e}{r_{e2}} \right)^2 \Delta r_{e2} \]  

(A2)

According to the definition in (7) the correlation factor \( \Gamma \) becomes

\[ \Gamma = \frac{(r_e/r_{e1})^2 \langle \Delta I_{be1} \Delta r_{e1} \rangle + (r_e/r_{e2})^2 \langle \Delta I_{be2} \Delta r_{e2} \rangle}{\sqrt{\langle \Delta I_{be1}^2 \rangle} \cdot \sqrt{\langle \Delta r_{e1}^2 \rangle} + (r_e/r_{e1})^4 \langle \Delta I_{be1}^2 \rangle + (r_e/r_{e2})^4 \langle \Delta I_{be2}^2 \rangle} \]  

(A3)

With full correlation in each part we obtain

\[ \Gamma = \frac{(r_e/r_{e1})^2 \sqrt{\langle \Delta I_{be1}^2 \rangle} \cdot \sqrt{\langle \Delta r_{e1}^2 \rangle} + (r_e/r_{e2})^2 \sqrt{\langle \Delta I_{be2}^2 \rangle} \cdot \sqrt{\langle \Delta r_{e2}^2 \rangle}}{\sqrt{\langle \Delta I_{be1}^2 \rangle} + (r_e/r_{e1})^4 \langle \Delta I_{be1}^2 \rangle + (r_e/r_{e2})^4 \langle \Delta I_{be2}^2 \rangle} \]  

(A4)

After some manipulations we find

\[ \Gamma^2 = \frac{\kappa x + \kappa^{-1} \nu + 2\sqrt{x} \nu}{\kappa x + \kappa^{-1} \nu + \kappa^{-1} x \nu + \kappa^{-1} \nu} \text{ with } \kappa = \left( \frac{r_{e2}}{r_{e1}} \right)^2, x = \left( \frac{\Delta I_{be1}^2}{\Delta I_{be1}^2} \right), \text{ and } \nu = \left( \frac{\Delta r_{e2}^2}{\Delta r_{e1}^2} \right) \]  

(A5)

From expression (A5) we can obtain the following expression for \( \Gamma \)
\[
\Gamma = \frac{1}{\sqrt{1 + \left(\frac{\sqrt{xv/\kappa^2} - 1}{\sqrt{x} + \sqrt{v/\kappa^2}}\right)^2}} \quad \text{(A6)}
\]

Note that for the homogeneous case, i.e. \(x = v = \kappa = 1\), we obtain \(\Gamma = 1\). For \(xv \neq 1\) we have \(\Gamma < 1\).

Substitution of \(y = v/\kappa^2\) in (A6) leads to expression (10).

References

Chapter 4

LOW-FREQUENCY NOISE IN Ga0.5In0.5P/GaAs HETEROJUNCTION BIPOLAR TRANSISTORS

4.1 INTRODUCTION

Excellent microwave performance makes the HBT (Heterojunction Bipolar Transistor) a very interesting device for many applications at RF (radio frequency) and microwave bands. However, the low-frequency noise of the devices used in such circuits can limit the bandwidth and the stability of the circuit operation at high speed [1]. It also causes phase noise in oscillators.

The low-frequency noise of HBTs is reported to be very low. In recent papers [2],[3] the 1/f noise of these devices was ascribed to fluctuations in the surface recombination velocity at the extrinsic base of the HBT. This noise source was found to be dominant in small size HBTs. Also a 1/f noise contribution from the emitter series resistance has been reported [4]. Up to now relatively little experimental data has been published on the low-frequency noise of GaInP/GaAs HBTs [2]. The fact that the low-frequency noise of GaInP/GaAs HBTs is still an open field is the main motivation for our work.

In this chapter we present the results of a low-frequency noise study on Ga0.5In0.5P/GaAs heterojunction bipolar power transistors with different emitter geometries. The low-frequency noise results are obtained from two different series of transistors. Both series have been made with basically the same production process. However, series 2 has an improved insulation of the metal connecting the emitter to the bonding pad. The influence of this improved insulation on the I-V characteristics and on the 1/f noise will be investigated.

4.2 EXPERIMENTAL RESULTS

A. Devices

In Table 4.1 the layer structure of the devices is given. The transistors are multiple emitter structures. The emitters have a finger structure with a finger length in the range of 20-40 µm, and a width of 2 µm. The number of fingers is between 2 and 18. These transistors belong to series 1. Devices of series 2 are made with basically the same production process. The only difference is an improved insulation between the transistor and the metal layer connecting the emitter contact to the bonding pad. From this series of devices only two emitter geometries were available. The transistors are single emitter transistors with an emitter length of 20 µm or 40 µm, and an emitter width of 2 µm.
Table 4.1 Layer structure of the GaInP/GaAs HBTs

<table>
<thead>
<tr>
<th>Material</th>
<th>Composition</th>
<th>Thickness (µm)</th>
<th>Dopant (cm⁻³)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaAs</td>
<td>-</td>
<td>0.28</td>
<td>Si 4.10¹⁸</td>
</tr>
<tr>
<td>GaₓIn₁₋ₓP emitter</td>
<td>0.5</td>
<td>0.02</td>
<td>Si 2.10¹⁸</td>
</tr>
<tr>
<td>GaₓIn₁₋ₓP</td>
<td>0.5</td>
<td>0.1</td>
<td>Si 3.10¹⁷</td>
</tr>
<tr>
<td>GaAs base</td>
<td>-</td>
<td>0.1</td>
<td>C 3.10¹⁹</td>
</tr>
<tr>
<td>GaAs collector</td>
<td>-</td>
<td>0.7</td>
<td>Si 1.10¹⁶</td>
</tr>
<tr>
<td>GaAs collector</td>
<td>-</td>
<td>0.5</td>
<td>Si 4.10¹⁸</td>
</tr>
</tbody>
</table>

semi-insulating GaAs substrate

B. **DC characteristics**

Fig. 4.1 presents a typical plot of the $I$-$V$ characteristic of a transistor with 10 emitter fingers of 20 µm length.

![Graph of I-V characteristic](image)

Fig. 4.1 Typical plot of the $I$-$V$ characteristics of a transistor of series 1 with 10 emitter fingers of 20µm length.

We observed that the ideality factor of the base current $I_B$ is current-dependent for all transistors. We decompose the current $I_B$ in two current components: an ideal component with ideality factor 1 and a non-ideal component with an ideality factor higher than unity that varies from transistor to transistor. The values of the ideality factor of the non-ideal component are in the range of 1.5-2.8. The ideality factor of the collector current $I_C$ is found to be 1. At low currents there is a leakage collector current which is (nearly) independent of the base-emitter voltage $V_{be}$. Thus the base current and collector current can be described by
Experimental results

\[ I_B = I_{B0i}[\exp(V_{be}/V_t)-1] + I_{B0ni}[\exp(V_{be}/\eta V_t)-1] \]  
\[ I_C = I_{C0}[\exp(V_{be}/V_t)-1] + I_{C1} \]  

(4.1)

Here, \( I_{B0i} \) and \( I_{B0ni} \) are the reverse saturation current of the ideal base current component and the non-ideal base current component, respectively, \( I_{C1} \) is the base-emitter voltage independent contribution to the collector current. \( V_t = kT/q \) is the thermal voltage, \( V_{be} \) is the voltage across the base-emitter junction, and \( \eta \) is the ideality factor of the non-ideal base current. Most devices show a deviation from exponential behavior at high currents which is mainly ascribed to the influence of the emitter series resistance (see Fig. 4.3 for an example). The value of the emitter series resistivity is in the range 60-160 \( \Omega \mu m^2 \). The solid lines in Fig. 4.1 represent the best fit using the Eqs. (4.1).

During measurement of the \( I-V \) curves the non-ideal base current increased at constant base-emitter bias. Also the ideality factor increased during measurement. This degradation during the measurements causes problems for the accuracy of the measurements and hence impedes a detailed analysis of the results.

In Fig. 4.2 the values of \( I_{B0i} \) and \( I_{C0} \) are plotted versus the emitter area. We observe that both currents are proportional to the emitter area.

\[ A_E (\mu m^2) \]

\[ I_{B0i}, I_C (A) \]

Fig. 4.2 Reverse saturation current of ideal base current \( I_{B0i} \) and collector current \( I_{C0} \) versus the emitter area \( A_E \). Results are obtained from series 1.

Our choice for decomposition of the base current in an ideal part (with ideality factor 1.0) and a non-ideal part seems artificial because we never observe a part in the \( I_B-V_{BE} \) curves that exactly has an ideality factor of 1.0, due to the roll-off caused by the emitter series resistance. However, the fact that \( I_{B0i} \) is found to be proportional to the emitter area supports our choice for this decomposition.

In Fig. 4.3 the \( I-V \) curve of a transistor of series 2 is presented. Analogous to the devices of series 1, we split the base current as given by (4.1) in an ideal part and a non-ideal part with \( \eta = 1.7 \). The emitter series resistance is found to be 8.5 \( \Omega \), which
leads to a series resistivity of 340 \( \Omega \mu \text{m}^2 \). When we compare both the \( I-V \) curves presented in Fig. 4.1 and Fig. 4.3 at constant \( I_C = 10^{-4} \) A we observe that the base current is non-ideal for both devices and that \( I_B = 2 \times 10^{-5} \) A for both devices. So we observe no significant influence of the improved insulation on the \( I-V \) characteristics of these devices.

![Graph](image)

**Fig. 4.3** \( I-V \) curve of a transistor of series 2 with one emitter of 20 \( \mu \text{m} \) length.

### C. Noise measurements

The transistor is part of the AC circuit given in Fig. 4.4.

![Diagram](image)

**Fig. 4.4** AC noise measurement circuit.

The formulae for the voltage noise at the base, emitter, and collector contact are given in [5]. We carried out the measurements in a common-emitter circuit, i.e. we take \( R_B >> r_e + r_b + (\beta+1)r_e \) and \( R_E = 0 \), then the formulae for the voltage noise at the collector contact \( S_{V_C} \) and the voltage noise at the base contact \( S_{V_B} \) simplify to

\[
S_{V_C} \equiv R_C^2 \left\{ \beta^2 S_{I_b} + S_{I_c} + \left( \frac{\beta}{R_B} \right)^2 \left[ I_B^2 S_{rb} + I_E^2 S_{re} \right] \right\}
\]

\[
S_{V_B} \equiv [r_e + \beta r_e]S_{I_b} + r_b S_{I_c} + I_B^2 S_{rb} + I_E^2 S_{re}
\]
where $r_{b,c,e}$ are the parasitic series resistance of the base, collector and emitter. $R_B,C,E$ are the external resistances (metal film), $r_\pi$ is the dynamic input resistance and $\beta$ is the dynamic gain. $S_{I_B}$ is the current noise generator located between base and emitter, $S_{I_C}$ is the current noise generator located between collector and emitter, $S_{r_B}$ and $S_{r_E}$ are the noise generators of the base series resistance and emitter series resistance, respectively.

With these two equations we can determine which noise generators are dominant. The combination of $S_{V_C}$ and $S_{V_B}$ has been chosen because the noise at the base and collector contact can be measured simultaneously in a common-emitter circuit. This is desirable because the $I$-$V$ characteristics of these transistors, and consequently their dynamic parameters $r_\pi$ and $\beta$, keep changing. Simultaneous measurement of $S_{V_C}$ and $S_{V_B}$ guarantees that both are measured with equal dynamic parameters. Also the possible changes of the noise generators $S_{I_B}$, $S_{I_E}$, $S_{r_E}$, and $S_{r_B}$, due to the steady degradation do not compromise the analysis of $S_{V_C}$ and $S_{V_B}$ with the help of (4.2), when both noises are measured simultaneously.

The values of the dynamic gain $\beta$ and the input resistance $r_\pi$ are calculated with the help of the approximation of the DC characteristics as described by (4.1). We measured the noise from 1 Hz to 25 kHz. We observed $1/f$ noise only. The spectral density is proportional to $1/f^\gamma$ with $\gamma$ in the range of 1.0-1.2. In Fig. 4.1 some typical spectra are plotted of the current noise $S_{V_B}/r_\pi^2$ versus the frequency.

![Graph](image)

Fig. 4.5 Spectral density of the current noise $S_{V_B}/r_\pi^2$ versus the frequency. Spectra are from a transistor of series 1 with 2 emitter fingers of 20 $\mu$m length, at base currents of A: 53 $\mu$A, B: 11 $\mu$A, and C: 2.6 $\mu$A.

By measuring the $1/f$ noise at the collector and base contact and analyzing the results with (4.2), we found the $1/f$ noise in the base current $S_{I_B}$ to be the dominant noise generator for the transistors of both series 1 and series 2. This analysis goes
along the following lines. For instance we assume that the base current noise $S_{I_b}$ is dominant compared to the other three noise generators. We calculate $S_{I_b}$ with the help of the first equation in (4.2), thus $S_{I_b} = S_{V_C}/(\beta R_C)^2$. This calculated value of $S_{I_b}$ is substituted in the second equation of (4.2) and $S_{V_B}$ is calculated with

$$S_{V_B} = (r_n + \beta r_e)^2 S_{I_b}.$$ 

The calculated value of $S_{V_B}$ is compared to the measured value of $S_{V_B}$. If good agreement is obtained for the whole current range we conclude that $S_{I_b}$ is the dominant noise generator. If no agreement is obtained we have to try the same procedure with one of the other noise generators or a combination of noise generators.

In Fig. 4.6 the 1/f base current noise $S_{I_b}$ is plotted versus the base current for a 16 finger emitter transistor of series 1 (30 µm finger length). For all transistors of series 1 the base current noise $S_{I_b}$ is proportional to $I_B^2$ at low currents. At high currents there is a roll-off. In section 4.3 the roll-off will be discussed.

![Fig. 4.6](image)

In Fig. 4.6 the 1/f base current noise $S_{I_b}$ versus the base current $I_B$ of a transistor of series 1 with 16 emitter fingers of 30 µm length.

In Fig. 4.7 the 1/f noise $S_{I_b}$ is plotted versus the base current of a transistor of series 2. We observe that $S_{I_b}$ of this transistor is much lower than the noise of the transistor of series 1 in Fig. 4.6. The base-current dependence of $S_{I_b}$ is similar to the devices of series 1, i.e. at low current $S_{I_b} \propto I_B^2$ and at high currents there is a roll-off.

**D. Emitter geometry dependence**

The current and the fluctuations in the current are given by

$$I(t) = \int J(r,t)dr \quad \text{and} \quad \Delta I(t) = \int \Delta J(r,t)dr$$

(4.3)
where \( A \) is the area where the current \( I \) flows through, and \( J(r) \) the current density at position \( r \).

![Figure 4.7](image)

**Fig. 4.7** The 1/f noise in the base current versus the base current of a single-emitter transistor with series 2 (40 µm emitter length).

The spectral density of the current fluctuations is

\[
S_I(f) = \int \int S_J(r, r', f) \, dr \, dr'
\]

with \( S_J(r, r', t) \) the cross-correlation spectral density of the current density fluctuations. Provided that the noise sources are spatially uncorrelated we have

\[
S_J(r, r', f) = K(r, f) \delta(r - r') \quad \text{and thus} \quad S_I(f) = \int K(r, f) \, dr
\]

with \( K(r, f) \) a function related to the spectral density of the current density fluctuations at \( r \). If both current density and noise sources are distributed homogeneously and if \( S_J \propto J^\gamma \) and thus \( K \propto J^\gamma \) we have

\[
S_I = \int K \, dr \propto \int J^\gamma \, dr = \int (I/A) \gamma \, dr = I^\gamma A^{1-\gamma}
\]

Now we compare (4.6) with the experimental results. Therefore we plot \( S_{I_b} \) measured at \( f = 1 \) Hz and \( I_B = 1 \) µA base current versus the emitter area \( A_E \), see Fig. 4.8. At \( I_B = 1 \) µA the non-ideal base current is dominant for all transistors and \( S_{I_b} \) is proportional to \( I_B^2 \), so we expect \( S_{I_b} \propto A_E^{-1} \). There is a large spread in the results. The experimental data does not exclude \( S_{I_b} \propto A_E^{-1} \), but results are too scattered to be conclusive. The scattering in the results decreases with increasing number of emitters. Presumably this is due to an averaging of the contributions of all emitters.
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Fig. 4.8 The $1/f$ noise $S_{I_b}$ measured at 1 µA base current versus the emitter area $A_E$. Results are obtained from transistors of series 1.

Now we focus on the relation between the $1/f$ noise and the emitter length. Therefore we compare devices with 16 emitters in order to have the least scattering in the results. We studied 2 devices of 20 µm emitter length, 3 devices with 30 µm emitter length, and 3 devices of 40 µm emitter length. The average value of the $1/f$ noise at $f = 1$ Hz and $I_B = 1$ µA is $3.0 \cdot 10^{-17}$ A$^2$/Hz for 20 µm emitters, $3.3 \cdot 10^{-17}$ A$^2$/Hz for 30 µm emitters, and $2.3 \cdot 10^{-17}$ A$^2$/Hz for 40 µm emitters. So the value of the $1/f$ noise averaged over a large number of emitters is more or less independent of the emitter length. In case of a homogeneous distribution of current density and $1/f$ noise sources we expect an inverse proportionality with the emitter length. Hence the $1/f$ current noise sources are not homogeneously distributed across the emitter area or along the emitter perimeter.

From series 2 we only had single emitter devices available. So we could not study the noise as a function of the emitter geometry, and hence we cannot gain insight in the location of the non-ideal base current and the $1/f$ noise sources for the devices of series 2.

4.3 INTERPRETATION

The experimental results presented in the previous section can be explained by assuming that the $1/f$ noise in the base current is associated with the non-ideal base current $I_{Bni}$, and that $S_{I_b} \propto I_{Bni}^2$.

Here we give the arguments.

1) At low currents we found that $S_{I_b} \propto I_B^2$ for all devices (see Fig. 4.6 and Fig. 4.7).

At low currents the base current is dominated by the non-ideal part, i.e. $I_B \equiv I_{Bni}$, and thus $S_{I_b} \propto I_{Bni}^2$. At high currents we observed a roll-off in the plot of $S_{I_b}$ versus $I_B$. At high currents the base current is dominated by the ideal base
current $I_{Bi}$. We then have $S_{I_b} \propto I_{Bni}^2 \propto I_{Bi}^{2/\eta} \equiv I_{B}^{2/\eta}$, where $\eta$ is the ideality factor of the non-ideal base current. An example of a plot of $S_{I_b}$ versus $I_{Bni}$ is given in Fig. 4.9. We observe that $S_{I_b} \propto I_{Bni}^2$ in the whole current range.

![Graph showing 1/f noise in base current versus non-ideal base current.](image)

**Fig. 4.9** The 1/f noise in the base current versus the non-ideal base current of a single emitter transistor of series 2 (40 \( \mu \)m emitter finger length).

2) The ideality factor of the non-ideal base current is different from device to device, but for all devices of series 1 we observed $S_{I_b} \propto I_{B}^2$ at low currents.

3) From the emitter geometry dependence of the 1/f noise in the base current $S_{I_b}$ we suppose that the noise sources are not homogeneously distributed across the emitter area or along the emitter perimeter. The fact the 1/f noise at constant current is more or less independent of the emitter length and the fact that the improved insulation of the transistors of series 2 leads to a considerable reduction in the 1/f noise suggest that the 1/f noise is located at the emitter-finger tips [6]. A schematic top view of the emitter where the possible location of the noise sources is indicated by the shaded areas is given in Fig. 4.10.

![Schematic top view of a transistor.](image)

**Fig. 4.10** schematic top view of a transistor
Since all devices of both series 1 and 2 show $S_{I_b} \propto I_{Bni}^2$, we use the value of $S_{I_b}/I_{Bni}^2$ for comparison between the devices. We found that the 1/f noise for the improved devices (series 2) is approximately a factor $10^4$ lower than for devices with the same emitter layout of series 1.

4.4 COMPARISON WITH LITERATURE

The empirical relation $S_{I_b} \propto I_{Bni}^2$ for HBTs can also be found in literature.

Kleinpenning et al. [4] studied the low-frequency noise of three GaAs/AlGaAs HBTs. He found that the dominant 1/f noise generators were $S_{I_b}$ and $S_{I_c}$ at low to moderate currents and $S_{r_e}$ at high currents. The ideality factor of the base current was 2 for the whole studied current range, so no current component with an ideality factor close to unity was observed. For two devices he found $S_{I_b} \propto I_B^2$. For the third device an exact relation between $S_{I_b}$ and $I_B$ could not be established from his experimental results. The values of $S_{I_b}/I_{Bni}^2$ at $f = 1$ Hz were $4 \times 10^{-9}$ Hz$^{-1}$ and $8 \times 10^{-9}$ Hz$^{-1}$, which were slightly lower than the values of our devices of series 2, $(10^{-8}$ Hz$^{-1}$ at 1 Hz). Here we also should consider that the emitter area and perimeter were about a factor 4 smaller, so presumably the noise sources in the AlGaAs/GaAs devices in [4] are considerably weaker than in the devices of series 2 (see Eq (4.6)).

Jin-Ho Shin et al. [2] studied the 1/f noise in GaInP/GaAs HBTs. In Fig. 4.11 the values of $S_{V_B}/(r + \beta r_e)^2$ and $S_{V_C}/(\beta R_C)^2$, as extracted from the data in [2], are plotted versus the collector current.

Fig. 4.11 Current noise spectral density versus collector current. Data after Jin-Ho Shin [2].
According to (4.2) these two expressions are equal to $S_{1b}$ provided that $S_{1b}$ is the dominant noise generator. At low currents we observe that both curves in Fig. 4.11 coincide and we conclude that the dominant 1/\$f\$ noise generator is located in the base current $S_{1b}$. At high currents we observe a saturation of the value of $S_{V_B}/(r_{\pi} + \beta r_e)^2$, whereas the value of $S_{V_C}/(\beta R_C)^2$ does not saturate. Jin-Ho Shin et al. ascribe this saturation to the gain creeping effect of the HBT originating from the persistent band discontinuity [7]. At high forward bias, when the junction space charge has collapsed, the injection of carriers can no longer increase. The forward bias then is controlled by the persistent band discontinuity at the heterojunction. When this occurs, the collector current increases with the square root of the collector emitter bias, i.e. $\Delta I_C \propto \Delta V_{CE}^2$. This phenomenon is called the gain creep.

Jin-Ho Shin et al. [2] did not give a quantitative analysis of the gain creep effect. Here we will give a quantitative analysis and we will show that the gain creep effect is an unlikely candidate for explaining the experimental results completely. The data in Fig. 4.11 is plotted versus the collector current. However, we are interested in the behavior of $S_{1b}$, and hence in the behavior of $S_{V_B}/(r_{\pi} + \beta r_e)^2$ as a function of the base current. The value of $S_{V_B}/(r_{\pi} + \beta r_e)^2$ shows a saturation at high currents, not only as a function of the collector current (see Fig. 4.11), but also as a function of the base current. A possible explanation of this anomalous behavior can be the fact that the formulae (4.2) may no longer be accurate if gain creeping occurs. The formulae for a transistor in a common-emitter circuit with $S_{1b}$ as dominant 1/\$f\$ noise generator, taking into account the influence of the gain creeping effect, are derived in the appendix. We obtain

$$S_{V_B} = \left(\frac{\beta r_e}{1+\delta(R_C + r_c + r_e)}\right)^2 S_{1b}$$

and

$$S_{V_C} = \left(\frac{\beta R_C}{1+\delta(R_C + r_c + r_e)}\right)^2 S_{1b}$$

where $\delta = \partial I_C/\partial V_{CE}$ is a factor describing the gain creeping effect.

At high currents the term $\beta r_e$ in the denominator of $S_{V_B}/(r_{\pi} + \beta r_e)^2$ is of the order of magnitude of $r_{\pi}$ or larger. So if $\delta(R_C + r_c + r_e) >> 1$ the difference between the formulae (4.2) and (4.7) for calculating $S_{1b}$ is significant. In [2] no data is supplied about the values of $R_C$ and $\delta$ so we cannot check whether there still is saturation of $S_{1b}$ as a function of $I_B$ when we calculate $S_{1b}$ with the help of (4.7) instead of (4.2).

The ratio of the values of $S_{V_B}/(r_{\pi} + \beta r_e)^2$ and $S_{V_C}/(\beta R_C)^2$, that are given in Fig. 4.11, can be calculated using (4.7).
\[
\frac{S_{V_B}}{(r_\pi + \beta r_e)^2} \left( \frac{\beta R_C}{S_{V_C}} \right)^2 = \left( 1 + \frac{r_\pi \delta (R_C + r_e + r_e)}{r_\pi + \beta r_e} \right)^2 \tag{4.8}
\]

This ratio is equal to 1 or larger so if \( S_{I_b} \) is the dominant noise generator and gain creep occurs we expect the value of \( S_{V_B}/(r_\pi + \beta r_e)^2 \) to be equal to or larger than the value of \( S_{V_C}/(\beta R_C)^2 \) at high currents. The opposite is observed in Fig. 4.11. Possibly this effect at high currents has to be ascribed to a second noise generator. In the appendix the contributions of \( S_{I_c} \), \( S_{r_b} \), and \( S_{r_e} \) to \( S_{V_B} \) and to \( S_{V_C} \) are calculated in (A16), (A17).

In case there is a dominant contribution of \( S_{I_c} \) at high currents we calculate the ratio of the value of \( S_{V_B}/(r_\pi + \beta r_e)^2 \) and \( S_{V_C}/(\beta R_C)^2 \), using (A16), to be

\[
\frac{S_{V_B}}{(r_\pi + \beta r_e)^2} \left( \frac{\beta R_C}{S_{V_C}} \right)^2 = \left( \frac{\beta r_e}{r_\pi + \beta r_e} \right)^2 \tag{4.9}
\]

This ratio is approximately equal to 1 at high currents, so the divergence between the two curves in Fig. 4.11 cannot be explained in terms of a contribution of \( S_{I_c} \).

From the parasitic series resistances \( S_{r_b} \) and \( S_{r_e} \) only \( S_{r_e} \) can lead to the observed divergence at high currents if \( \beta/R_B + \delta \gg 1/r_e \). However, if this is the case we have \( \beta r_e/R_B >> 1 - \delta r_e \equiv 1 \), so that the condition \( R_B >> \beta r_e \) is no longer met and the approximations made for the calculation of (4.7), (A16) and (A17) are no longer valid. In [2] no values of \( R_B \) are given. However, from the data in [2] we find that \( \beta r_e < 400 \) and \( I_B < 1 \, \text{mA} \), so if \( R_B \) is of the order of magnitude of \( \beta r_e \) the voltage drop across \( R_B \) is lower than 0.4 V. Usually the voltage drop across \( R_B \) is approximately equal to the voltage of the batteries used in the measurement circuit. So it is unlikely that the values of \( R_B \) as low as \( \beta r_e \) were used in the experiments of Jin-Ho Shin et al. [2].

Summarizing, our quantitative analysis shows that it is unlikely that the experimental results at high currents can be ascribed to only the current creep effect.

The \( I-V \) curve of the base current of this transistor [2] consists of two current components with ideality factor 1.6 (here called \( I_{Bni} \)) and 1.07. The ideality factor of the collector current is 1.0. If we suppose that \( S_{I_b} \) is associated with the non-ideal base current we have

\[
S_{I_b} \approx I_{Bni}^2 \approx I_{n}^2/\eta_{B} = I_{C}^{1.25}, \tag{2.17}
\]

with \( \eta_{B} \) the ideality factor of \( I_{Bni} \). In Fig. 4.11 the slope 1.25 for the collector current is indicated. At low currents the data points fit reasonably well to a curve with the slope of 1.25. Also for this transistor the \( 1/f \) noise in the base current may be associated with the non-ideal base current \( I_{Bni} \) and proportional to this current squared.

The value of \( S_{I_b}/I_{Bni}^2 \) is \( 2 \times 10^{-7} \, \text{Hz}^{-1} \) at 1 Hz for this device, which is a factor 10 higher than the value found for our devices of series 2. Furthermore the device in
Comparison with literature

[2] is a large emitter area devices (120×120 µm²). Referring to (4.6) the noise sources presumably are considerably stronger than our devices of series 2.

Jin-Ho Shin et al. [2] also carried out measurements on an AlGaAs/GaAs device of the same emitter geometry. Also this device can be interpreted in terms of $S_{rb} \propto I_{Bni}^2$ with a value for $S_{rb}/I_{Bni}^2$ of $7 \cdot 10^{-10}$ Hz⁻¹ at 1 Hz.

Comparing the results in terms of $S_{rb}/I_{Bni}^2$ of the AlGaAs/GaAs HBTs [2],[4] with the results of GaInP/GaAs from [2] and our devices of series 2, we find that the AlGaAs/GaAs devices have less 1/f noise than the GaInP/GaAs devices. However, such a comparison of 1/f noise between devices made of AlGaAs/GaAs and of GaInP/GaAs gains significance if the noise is stemming from the intrinsic transistor and not if the noise is in the recombination current at the extrinsic base surface, because then the results may depend very strongly on the surface passivation applied. A study of the emitter geometry dependence of the 1/f noise of both types of devices is necessary to determine the exact location of the dominant 1/f noise sources.

We do not have a theoretical interpretation for the empirical relation $S_{rb} \propto I_{Bni}^2$, but the fact that we find this relation for all devices discussed in this chapter, gives a firm basis for this empirical relation. This is surprising since the devices have a large spread in the ideality factor of the non-ideal base current and have a spread in the base-current dependence of $S_{rb}$.

4.5 CONCLUSIONS

The $I-V$ characteristics and the 1/f noise of Ga0.5In0.5P/GaAs heterojunction bipolar power transistors have been studied. The ideality factor of the collector current is 1 at high currents. At low currents the collector current is independent of the base-emitter bias for the devices of series 1. The $I-V$ curve for the base current shows a high ideality factor at low currents and a lower ideality factor at high currents. We obtain reasonably accurate results with a description in terms of two base current contributions, one non-ideal with a high ideality factor (in the range of 1.5-2.8), and an ideal one with ideality factor 1.

From the noise measurements we found that the 1/f noise in the base current $S_{rb}$ is the dominant noise generator. At low currents, where the base-current ideality factor is high, we find that $S_{rb}$ is proportional to $I_B^2$. At high currents, where the ideality factor decreases, there is a roll-off.

Our interpretation of the roll-off is that $S_{rb}$ is associated with the non-ideal base current. We find that $S_{rb}$ is proportional to the non-ideal base current squared over the whole studied current range, without a roll-off.

There is a large spread in the 1/f noise magnitude for different transistors of series 1. Due to this spread it is difficult to be conclusive about the emitter area dependence of the 1/f noise. However, from devices with a large number of emitters, having less spread in the noise magnitude, we found that the 1/f noise magnitude is independent of the emitter finger length. Based on this experimental fact we
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suppose that the dominant 1/f noise generators are located at the emitter finger tips.

For the devices with the improved insulation (series 2) we found that $S_I\textsubscript{b}$ is the dominant 1/f noise generator. Also for these devices we found $S_I\textsubscript{b}$ to be proportional to the non-ideal base current squared. Due to the improved insulation a huge reduction in the 1/f noise is obtained. Using the relative 1/f noise in the non-ideal base current for comparison between devices of comparable emitter geometry, we find a reduction of a factor $10^4$ in the noise for the devices of series 2 compared to those of series 1.

A comparison is made between experimental results obtained from our devices and results presented in literature from AlGaAs/GaAs and from GaInP/GaAs devices. It is found that AlGaAs/GaAs devices have less 1/f noise than GaInP/GaAs devices.

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Appendix

**CALCULATION OF VOLTAGE SPECTRAL DENSITIES FOR TRANSISTORS EXHIBITING THE GAIN CREEPING EFFECT**

If we suppose that that $S_I\textsubscript{b}$ is the dominant 1/f noise generator, and that the transistor is put in a common-emitter circuit, i.e. $R_E = 0$, we have the following set of equations

\[ \Delta I_C = g_m \Delta V_{be} + \delta V_{ce} \]  
\[ \Delta I_B = \Delta I_{be} + \frac{\Delta V_{be}}{r_\pi} \]  
\[ \Delta I_E = \Delta I_B + \Delta I_C \]  
\[ \Delta V_{be} = -(R_B + r_\beta)\Delta I_B - r_\pi \Delta I_E \]  
\[ \Delta V_{ce} = -(R_C + r_\epsilon)\Delta I_C - r_\pi \Delta I_E \]

where $\Delta I_{be}$ represents the spontaneous fluctuations in the base current, $g_m = \partial I_C/\partial V_{be}$ the transconductance, and $\delta = \partial I_C/\partial V_{ce}$ a factor describing the gain creeping effect. Combining (A2), (A3), and (A4) leads to
\[\Delta I_C = \Delta I_{ce} + g_m \Delta V_{be} + \delta V_{ce}\]  \hspace{1cm} (A12)

\[\Delta I_B = \Delta I_{be} + \frac{\Delta V_{be}}{r_{\pi}}\]  \hspace{1cm} (A13)

\[\Delta V_{be} = -(R_B + r_b)\Delta I_B - r_e \Delta I_E - I_E \Delta r_e - I_B \Delta r_b\]  \hspace{1cm} (A14)

\[\Delta V_{ce} = -(R_C + r_c)\Delta I_C - r_e \Delta I_E - I_E \Delta r_e\]  \hspace{1cm} (A15)
Chapter 4. Low-frequency noise in Ga0.5In0.5P/GaAs HBTs

For the contribution of $S_{Ic}$ we obtain, following (A6) through (A11) and taking $R_B \gg r_b, r_n, \beta r_e$

$$S_{V_B} \equiv \left[ \frac{r_e}{1 + \delta (R_C + r_e + r_e)} \right]^2 S_{Ic}$$  \hspace{1cm} (A16)

$$S_{V_C} \equiv \left[ 1 + \delta (R_C + r_e + r_e) \right]^2 R_C^2 S_{Ic}$$

For the contribution of the series resistance fluctuations we find

$$S_{V_B} \equiv I_E^2 S_{r_e} + I_B^2 S_{rb}$$  \hspace{1cm} (A17)

$$S_{V_C} \equiv \frac{[R_C (\beta + \delta R_B)]^2 I_E^2 S_{r_e} + [R_C (\beta - \delta r_e)]^2 I_B^2 S_{rb}}{R_B^2 [1 + \delta (R_C + r_e + r_e)]^2}$$

References


[6] Private communication with staff members of the manufacturer.

Chapter 5

LOW-FREQUENCY NOISE IN MODULATION DOPED FIELD EFFECT TRANSISTORS

5.1 INTRODUCTION

The extremely low noise in the microwave frequency range is one of the main features of the modulation doped field effect transistors (MODFET). Nevertheless, the low-frequency noise characteristics are also important, since this type of noise leads to the very undesirable phase noise in oscillators.

Several authors have studied the low-frequency noise of MODFETs. Peransin et al. [1] studied the influence of the series resistance on the low-frequency characteristics of the MODFET biased in the ohmic region. They presented a method to determine whether the noise stems from the channel or from the series resistance. Py et al. [2] studied delta doped MODFETs. They found that both the two dimensional electron gas (2DEG) mobility and the channel 1/f noise parameter \( \alpha \) depend on the 2DEG electron concentration. They ascribe these dependencies to the screening effect of the 2DEG. Rojo-Romeo et al. [3] presented a comparison between devices based on different semiconductor materials. They interpret the 1/f noise in terms of carrier number fluctuations. They express their results as a function of an effective trap density \( N_t \). Dependent on the semiconductor materials used \( N_t \) varies over two decades.

In this chapter we present the experimental results obtained from MODFETs based on different semiconductor materials and made with different production processes. The chapter is divided in two parts. In the first part we consider the \( I-V \) characteristics and the 1/f noise in the 2DEG channel biased in the ohmic region. This part starts with a presentation of the methods to analyze the experimental results. A method will be presented to determine the location of the dominant 1/f noise source. Two methods for extraction of the value of the series resistance and the threshold voltage with the help of the 1/f noise will be shown. The first part ends with a comparison between devices made with different fabrication processes and based on different semiconductor materials.

In the second part we consider the \( I-V \) characteristics and the 1/f noise of the Schottky barrier in between gate and channel. An interpretation will be presented of the 1/f noise in the current through the Schottky barrier. This interpretation is made in terms of fluctuations in the tunneling probability of electrons through the oxide layer present between the semiconductor and the metal contact. These tunneling probability fluctuations give rise to fluctuations in the current through the barrier. At the end of the second part a comparison is made between the
experimental results obtained from devices based on different semiconductor materials and made with different production processes.

5.2 DEVICES

Experiments have been carried out on three types of MODFETs. One type (type A) is based on AlGaAs/GaAs material combination. The second (type B) is based on GaAs/AlGaAs material in combination with an InGaAs channel. The third (type C) is based on InAlAs/InGaAs material combination on top of an InP substrate. The MODFETs were made by IMEC (Louvain Belgium). We studied two series of AlGaAs/GaAs MODFETs (type A). The first series denoted by 2T4 and 2T5 is made using etching fluids for defining the gate area. The second series denoted by 7T4 and 7T5 is made using plasma etching for defining the gate area. All AlGaAs/GaAs devices have a gate width of 50 µm. The gate length is 0.3 µm for the 2T4 and the 7T4, and 0.7 µm for the 2T5 and 7T5 devices. For comparison we also studied a Fujitsu FHX31 MODFET (type A) with 280 µm gate width and 0.25 µm gate length. From the GaAs/AlGaAs MODFETS with InGaAs channel (type B) we studied three devices denoted by Q12, M12, and R12. The gate length is 0.2 µm and the gate width is 12.5 µm for all three devices. From the InAlAs/InGaAs on InP MODFETs (type B), designated with MIX5 we studied 6 devices with different gate width in the range of 25 to 175 µm. The gate length is 0.2 µm for all MIX5 devices. For the MIX5 devices the gate area is defined using etching fluids.

5.3 EXPERIMENTAL RESULTS OBTAINED FROM THE 2DEG CHANNEL

A I-V characteristics and 1/f noise at low drain-source bias

At low drain-source bias the total resistance between source and drain $R_{DS}$ at gate-source voltages above threshold voltage $V_T$ is given by [1]

$$R_{DS} = R_{ch} + R_s = \frac{L_G |V_T|}{W_G q \mu n_{ch} V_G} + R_s$$

(5.1)

where $R_{ch}$ is the channel resistance, $R_s$ the series resistance, $L_G$ is the gate length, $W_G$ the gate width, $\mu$ the mobility of the electrons in the 2-D gas, $n_{ch}$ the characteristic concentration of electrons in the 2-D gas at $V_G = V_T$, and $V_G$ the effective gate voltage $V_G = V_{GS} - V_T$, with $V_{GS}$ the applied gate-source voltage. The conductance $G_{DS} = 1/R_{DS}$ at low drain bias is measured as a function of the applied gate-source bias $V_{GS}$. The threshold voltage $V_T$ is determined from the extrapolation of $G_{DS}$ to $G_{DS} = 0$. An example of such a plot is given in Fig. 5.1. The solid line represents an estimate of the linear part of the curve. Its intersection with the $V_{GS}$ axis gives the threshold voltage. At high $V_{GS}$ the deviation from the solid line is ascribed to the series resistance. In the sub-threshold region the conductance is exponentially dependent on the applied gate-source bias. Once the threshold voltage is known we determine the series resistance value $R_s$ by plotting
Experimental results obtained from the 2DEG channel

the total channel resistance $R_{DS}$ versus the reciprocal value of the effective gate voltage $1/V_G$. This plot yields a straight line where we find $R_s$ at the intersection for $1/V_G = 0$.

![Graph](image)

Fig. 5.1 A plot of the conductance of the channel versus the applied gate-source voltage (FHX31).

Experimentally the 1/f noise in the drain-source voltage $S_{VDS}$ is found to be proportional to the drain current squared $I_D^2$. The 1/f noise $S_{VDS}$ consists of a contribution of the noise generated in the 2DEG channel plus a contribution from the series resistances at the drain and the source contact.

Peransin et al. [1] proposed a method for determining whether the channel or the series resistance contains the dominant 1/f noise generator. They considered $S_{ID}/I_D^2$ as a function of the effective gate voltage. Dependent on whether the noise stems from the channel or the series resistance and dependent on whether the total resistance between drain and source contacts is determined by the channel or series resistance we obtain four different slopes in the relation of $S_{ID}/I_D^2$ versus $V_G$.

Here we present an alternative method. Since the noise generators of the channel and the series resistance are in series it is more convenient to analyze voltage fluctuations rather than current fluctuations.

We have

$$S_{VDS}/I_D^2 = S_{R_{ch}} + S_{R_s}$$  \hspace{1cm} (5.2)

where $S_{R_{ch}}$ represents the 1/f noise in the channel resistance and $S_{R_s}$ the 1/f noise in the series resistance. With the help of Hooge’s relation [4] we obtain the following expressions for $S_{R_{ch}}$ and $S_{R_s}$:

$$S_{R_{ch}} = \frac{\alpha_{ch} R_{ch}^2}{f N_{ch}} = \frac{\alpha_{ch} q \mu R_{ch}^3}{f L_G^2} \propto V_G^{-3}$$  \hspace{1cm} (5.3)
Chapter 5. Low-frequency noise in MODFETs

and

\[ S_{R_s} = \frac{\alpha_s R_s^2}{f N_s} \propto V_G^0 \]  \hspace{1cm} (5.4)

where \( N_{ch} \) and \( N_s \) are the number of carriers in the channel and the series resistance, respectively, \( \alpha_{ch} \) and \( \alpha_s \) the Hooge parameters for the channel and series resistance, respectively, and \( \mu \) is the mobility. Here we assume that the mobility and \( \alpha_{ch} \) are constant throughout the channel, so that we consider the channel to be homogeneous.

In Fig. 5.2 a plot is made of \( S_{V_{DS}} / I_D^2 \) measured at 1 Hz versus the effective gate voltage \( V_G \). According to (5.2)-(5.4) this plot has two regions with different slopes. In the region with slope -3 the channel \( 1/f \) noise is dominant. In the region with slope 0 the series resistance contains the dominant \( 1/f \) noise generator. In Fig. 5.2 these two regions can be observed clearly.

![Fig. 5.2 A plot of \( S_{V_{DS}} / I_D^2 \) measured at 1 Hz versus the effective gate voltage \( V_G \) of the 7G4.](image)

The plot in Fig. 5.2 is traced as a function of the effective gate voltage \( V_G \). Therefore we need an accurate value of the threshold voltage \( V_T \). On the basis of the \( I-V \) characteristics as presented in Fig. 5.1 it can be rather difficult to make a good estimate of \( R_s \) and \( V_T \). When the series resistance is high, the region where the total resistance is dominated by the series resistance and the region with the exponential sub-threshold behavior are not well separated by the region with \( G_{DS} \propto V_G \). If this is the case the method for determination of \( V_T \) as presented in Fig. 5.1 does not lead to accurate results. An alternative method, using the \( 1/f \) noise in the drain-source voltage, will be presented in the next section.
B. Parameter extraction with the help of 1/f noise

With the help of the 1/f noise of the channel in the ohmic region it is possible to determine the values of the series resistance and the threshold voltage. Let us suppose that the noise from the series resistance is negligible. We then have

$$\frac{S_{VDS}}{I_D^2} = \frac{\alpha_{ch} q \mu R_{ch}^3}{f L_G^2}$$  \hspace{1cm} (5.5)

The channel resistance can be expressed as $R_{ch} = R_{DS} - R_s$, with $R_{DS}$ the total resistance between drain and source contact. Substitution of $R_{ch}$ in (5.5) and raising to the power 1/3 yields

$$\left( \frac{S_{VDS}}{I_D^2} \right)^{1/3} = \left( \frac{\alpha_{ch} q \mu}{f L_G^2} \right)^{1/3} \cdot (R_{DS} - R_s)$$  \hspace{1cm} (5.6)

By plotting $\left( \frac{S_{VDS}}{I_D^2} \right)^{1/3}$ versus $R_{DS}$ we obtain the series resistance from the intersection at $\left( \frac{S_{VDS}}{I_D^2} \right)^{1/3} = 0$. An example is given in Fig. 5.3. Note that $R_{DS}$ is varied by varying $V_G$. This method can be used provided that $S_{R_{ch}} >> S_{R_s}$, then we obtain a straight line in Fig. 5.3.

Fig. 5.3 Plot for determination of $R_s$ (transistor Q12).

Since $R_{ch} \propto \frac{1}{V_G}$ we can rewrite (5.5)

$$\frac{S_{VDS}}{I_D^2} \propto \frac{\alpha_{ch} q \mu}{f L_G^2 V_G^3} \propto (V_{GS} - V_T)^{-3} \quad \text{or} \quad \left( \frac{S_{VDS}}{I_D^2} \right)^{-1/3} \propto (V_{GS} - V_T)$$  \hspace{1cm} (5.7)
By plotting \( (S_{VDS}/I_D^2)^{-1/3} \) versus \( V_{GS} \) we obtain the threshold voltage from the extrapolation of \( (S_{VDS}/I_D^2)^{-1/3} \) to \( (S_{VDS}/I_D^2)^{-1/3} = 0 \). An example is given in Fig. 5.4.

![Figure 5.4](image)

**Fig. 5.4** Plot for determination of \( V_T \) (transistor Q12).

The deviation from the straight line at low \( V_{GS} \) in Fig. 5.4 is caused by the fact that at sub-threshold the channel resistance is exponentially dependent on \( V_{GS} \), so that (5.7) no longer holds.

To check the accuracy of the parameters \( R_s \) and \( V_T \) obtained with the help of the two methods presented we plot \( 1/(R_{DS} - R_s) = 1/R_{ch} \) versus \( V_{GS} \). In Fig. 5.5 the values of \( 1/R_{ch} \) and \( 1/R_{DS} \) are plotted versus \( V_{GS} \) for transistor Q12. We observe that the calculated channel conductance \( 1/R_{ch} \) is proportional to \( V_G \). The value of \( V_T \) found in Fig. 5.4 coincides with the intersection for \( 1/R_{ch} = 0 \) in Fig. 5.5, and thus the values for \( R_s \) and \( V_T \) found using these methods are quite accurate. This example clearly illustrates the difficulty in finding accurate values for \( R_s \) and \( V_T \) with only the \( I-V \) characteristic as described in section 5.3A.

**Accuracy and systematic errors**

In appendix A an estimate of the accuracy of both methods is made. We only take into account the random errors. With the help of (A5.9) we find that the series resistance determined from Fig. 5.3 is 33.5±2 \( \Omega \), and that the threshold voltage determined from Fig. 5.4 is 30±10 mV. In Fig. 5.4 we only took into account the 6 measurement points with the highest \( V_{GS} \).

For both equations (5.6) and (5.7) we took a constant value for the mobility and hence we neglected the fact that the channel mobility depends on the electron concentration in the 2DEG channel. When the electron density in the 2DEG
Experimental results obtained from the 2DEG channel

channel increases the Coulomb scattering due to charged impurities is reduced by the increased screening of the 2DEG.

Py et al. [2] have measured the mobility of the 2DEG as a function of the electron concentration with the help of a gated Hall-bar structure. At room temperature they found an increase in $\mu$ of a factor 2 for an increase in $n_s$ from $1.2 \cdot 10^{11}$ cm$^{-2}$ to $7 \cdot 10^{11}$ cm$^{-2}$ for GaAs. On the basis of a power-law dependence of the mobility given by

$$
\mu = \mu_0 \left( \frac{n_s}{n_{s0}} \right)^k
$$

they found $k = 0.4$. On the other hand they also found that the Hooge parameter $\alpha$ depends on the electron concentration in the 2DEG. Furthermore they found that $\alpha$ is inversely proportional to the mobility. The mobility and the Hooge parameter appear as a product in the equations (5.3), (5.5)-(5.7). Hence the dependence of $\alpha$ and $\mu$ on $n_s$ cancels in these equations. The measurements presented by Py [2] are carried out on GaAs 2D electron gasses. To our knowledge no experimental data has been published of $\alpha$ and $\mu$ as a function of $n_s$ in InGaAs 2D electron gasses. Even if there is a slight dependence of the product $\alpha \mu$ on $n_s$ for InGaAs it only leads to a small error in the methods for determination of $R_s$ and $V_T$ because in (5.6) and (5.7) the product $\alpha \mu$ is raised to the power 1/3 and to the power -1/3, respectively, which makes the methods rather insensitive to the behavior of $\alpha \mu$ as a function of $n_s$.

Another consequence of carrier density dependence of the mobility is the fact that the channel resistance no longer is inversely proportional to the effective gate voltage. We have

$$
R_{ch} = \frac{L_G^2}{q\mu_0 (n_s/n_{s0})^k N_{ch}} = \frac{L_G n_{s0}^k}{q\mu_0 W_G n_s^{1+k}} \propto n_s^{-1-k} \propto V_G^{-1-k}
$$
Equation (5.3), which describes the 1/f noise for the case of a dominant noise generator located in the channel, modifies to

\[ S_{R_{ch}} = \frac{\alpha_{ch} R_{ch}^2}{f N_{ch}} = \frac{\alpha_{ch} q \mu R_{ch}^3}{f L_{G}^2} \propto V_G^{-3(1+k)} \]  

Here we suppose \( \alpha \mu \) to be independent of \( n_s \). The slope of the plot of \( S_{V_D S}/I_{D}^2 \) versus \( V_G \) in the region where \( S_{R_{ch}} \) is dominant, is quite sensitive to the value of \( k \). So with the help of the slope of this plot we can get an impression of the value of \( k \).

In Fig. 5.2 an example of such a plot was presented and the results were described with a part having a slope of -3 and a part with a slope 0. If we fit the expression

\[ f S_{V_D S}/I_{D}^2 = A V_G^{-3(1+k)} + B, \] with \( A \) and \( B \) constant, to the data of Fig. 5.2 we find \( k = 0.2 \). For all our devices \( k \) is found to be in the range of 0 to 0.2.

Once we have an estimate for the value of \( k \) the method for determination of \( V_T \) can be improved by replacing (5.7) by

\[ \left( \frac{S_{V_D S}}{I_{D}^2} \right)^{-\frac{1}{3(1+k)}} \propto \left( \frac{\alpha_{ch} q \mu}{f L_{G}^2} \right)^{-\frac{1}{3(1+k)}} (V_{GS} - V_T) \]  

C. Parallel channel

Provided that the influence of the series resistance is negligible, i.e. \( R_s \ll R_{ch} \) and \( R_{DS} \approx R_{ch} \), the relative 1/f noise in \( V_{DS} \) is given by

\[ \frac{S_{V_D S}}{V_{DS}^2} = \frac{\alpha}{f N_{ch}} = \frac{\alpha q \mu R_{ch}}{f L_{G}^2} \]  

At high values of \( R_{ch} \) the transistors 7T4 and 2T5 show a deviation from this relation. In Fig. 5.6 the relative 1/f noise \( S_{V_D S}/V_{DS}^2 \) is plotted versus \( R_{ch} \) for the 7T4. The deviation from the solid line can be ascribed to the influence of a leakage resistance parallel to the channel. Let us suppose that the dominant 1/f noise generator is located in the channel. The resistance \( R_{DS} \) is determined by the channel resistance \( R_{ch} \) and the parallel leakage resistance \( R_p \). We then have the following set of equations

\[ \Delta V_{DS} = I_{ch} \Delta R_{ch} + R_{ch} \Delta I_{ch} \]  

\[ \Delta V_{DS} = \Delta I_p R_p \]  

\[ \Delta I = 0 \]  

\[ \Delta I_p = -\Delta I_{ch} \]  

where \( I_{ch} \) is the current through the channel, \( I_p \) is the current through the parallel leakage, and \( I \) is the total current, which is the sum of both.
Experimental results obtained from the 2DEG channel

We solve for $\Delta V_{DS}$

$$\Delta V_{DS} = \frac{I_{ch} \Delta R_{ch}}{1 + R_{ch}/R_p} \quad (5.14)$$

We calculate the power spectral density of $\Delta V_{DS}$. With (5.3) and the relation $1/R_{DS} = 1/R_{ch} + 1/R_p$ we find

$$S_{V_{DS}} = \frac{\alpha_{ch} q \mu R_{DS}}{f L_G} \left( 1 - \frac{R_{DS}}{R_p} \right) \quad (5.15)$$

If $R_p$ is independent of $V_{GS}$, a plot of $S_{V_{DS}}/R_{DS} V_{DS}^2$ versus $R_{DS}$ yields a straight line, which intersects the horizontal axis at $R_{DS} = R_p$. This plot is presented in Fig. 5.7. We observe that the results do not follow a straight line, so the parallel resistance may be dependent on $V_{GS}$. With the help of (5.15) we can calculate the value of $R_p$ as a function of $R_{DS}$

$$R_p = \frac{R_{DS}}{1 - \left( \frac{\alpha_{ch} q \mu}{f L_G^2} \right)^{-1} S_{V_{DS}}/R_{DS} V_{DS}^2} \quad (5.16)$$

With both $R_{DS}$ and $R_p$ determined we calculate $R_{ch}$. In Fig. 5.8 the values of $G_{DS} = 1/R_{DS}$, $G_p = 1/R_p$, and $G_{ch} = 1/R_{ch}$ are plotted versus $V_G$. We observe that the sub-threshold channel conductance $G_{ch}$ shows an exponential dependence on $V_G$, which is in agreement with the results obtained from devices with no parallel leakage.
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Fig. 5.7 Plot of $S_{V_{DS}}/R_{DS}V_{DS}^2$ versus $R_{DS}$ for transistor 7T4.

Fig. 5.8 Plot of conductance $G_{DS}$, $G_{ch}$, and $G_p$ versus $V_G$ for transistor 7T4

We have

$$G_{ch,\text{sub-threshold}} \propto \exp\left(qV_G/\eta kT\right)$$ (5.17)

The extracted ideality factor $\eta = 1.7$ is comparable to results obtained from other devices, that are in the range of 1.7 to 3.5.

In Fig. 5.8 we only plotted a limited number of values of $G_p$ because the method (5.16) for calculation of $R_p$ becomes very inaccurate for small values of $R_{DS}$. As a result we cannot establish an exact relation between $R_p$ and $V_{GS}$. We observe that $R_p$ decreases by a factor 2 when $V_G$ increases from -0.1 to 0.1 V.
D. Comparison of devices.

Using the methods described in the previous section we analyzed the 1/f noise in $V_{DS}$ of all MODFETs. We define a series resistivity as the product of the series resistance and the gate width $R_sW_G$. The values of $R_sW_G$ are presented in Table 5.1.

<table>
<thead>
<tr>
<th>MODFET type</th>
<th>$V_T$ (V)</th>
<th>$R_sW_G$ (Ω·µm)</th>
<th>$\alpha$</th>
</tr>
</thead>
<tbody>
<tr>
<td>FHX31 A</td>
<td>-0.3</td>
<td>$7.6 \cdot 10^2$</td>
<td>$1 \cdot 10^{-4}$</td>
</tr>
<tr>
<td>2T4 A</td>
<td>0.2</td>
<td>$1 \cdot 10^3$</td>
<td>$5 \cdot 10^{-3}$</td>
</tr>
<tr>
<td>2T5 A</td>
<td>0.3</td>
<td>$1 \cdot 10^3$</td>
<td>$5 \cdot 10^{-3}$</td>
</tr>
<tr>
<td>7T4 A</td>
<td>-0.1</td>
<td>$1 \cdot 10^3$</td>
<td>$1 \cdot 10^{-3}$</td>
</tr>
<tr>
<td>7T5 A</td>
<td>0.2</td>
<td>$1 \cdot 10^3$</td>
<td>$1 \cdot 10^{-3}$</td>
</tr>
<tr>
<td>Q12 B</td>
<td>0.040</td>
<td>$4.6 \cdot 10^2$</td>
<td>$8 \cdot 10^{-5}$</td>
</tr>
<tr>
<td>M12 B</td>
<td>0.15</td>
<td>$6.9 \cdot 10^2$</td>
<td>$3 \cdot 10^{-4}$</td>
</tr>
<tr>
<td>MIX5 C</td>
<td>-0.7 to -1</td>
<td>$1 \cdot 10^3$ to $2 \cdot 10^3$</td>
<td>$5 \cdot 10^{-4}$ to $1 \cdot 10^{-3}$</td>
</tr>
</tbody>
</table>

We observe that all transistors have a series resistivity of roughly $10^3$ Ω·µm. Only the FHX31 and the GaAs/AlGaAs devices with InGaAs channel M12 and Q12 have slightly lower values.

Within the drain-source current range studied, the 1/f noise in all MODFETs is dominated by the 1/f noise generated in the channel. Only device 7T4 shows a dominant 1/f noise source in the series resistance at high currents (see Fig. 5.2). The $\alpha$-values are calculated with (5.12) and the results are presented in Table 5.1. We observe that of the AlGaAs/GaAs devices the plasma etched devices 7T4 and 7T5 show a somewhat lower $\alpha$-value than the fluid etched devices 2T4 and 2T5. All IMEC AlGaAs/GaAs devices have higher $\alpha$-values than the FHX31. The lowest $\alpha$-values for GaAs channels (FHX31) and InGaAs channels (Q12) are almost the same. The observed $\alpha$-values agree with values of the order of magnitude of $10^{-3}$ reported in literature [5].

5.4 Experimental Results obtained from the Schottky Barrier

A. I-V Characteristics and 1/f noise

In Fig. 5.9 a plot is made of the I-V characteristics of the gate Schottky barrier of three MODFET's. These measurements are carried out with the source and drain in short-circuit. At high currents we observe an exponential behavior. At low currents there is a deviation from the exponential law. This deviation is caused by a leakage current that adds to the current through the Schottky barrier. As suggested by
Vandamme et al. [6] this current could flow through a thin conductive path at the semiconductor surface between the gate electrode and source and drain electrode.

![Gate current voltage characteristic of A) FHC31FA, B) 2G4, and C) 7G4.](image)

Fig. 5.9 Gate current voltage characteristic of A) FHC31FA, B) 2G4, and C) 7G4.

At low currents the characteristic in Fig. 5.9 is linear, i.e. $I_G \propto V$. Hence the gate can be modeled with a Schottky barrier with ideality factor $\eta$ and a parallel ohmic resistance $R_p$, thus $I = I_0 [\exp(qV/\eta kT) - 1] + V/R_p$. The extracted values of $\eta$, $R_p$ and the reverse saturation current $I_0$ can be found in Table 5.2. In Fig. 5.10 the $1/f$ noise in the gate current $S_{IG}$ of the same devices as in Fig. 5.9 is plotted versus the gate current $I_G$.

![Gate current noise $S_{IG}$ versus gate current $I_G$ of A) FHX31FA, B) 2T4, and C) 7T4.](image)

Fig. 5.10 Gate current noise $S_{IG}$ versus gate current $I_G$ of A) FHX31FA, B) 2T4, and C) 7T4.
Experimental results obtained from the Schottky barrier 69

At high currents $S_{IG}$ is proportional to $I_G^2$. At low currents the 2T4 and 7T4 show deviations from the quadratic behavior.

From the analysis of the $I$-$V$ characteristics we concluded that at low currents an ohmic leakage current is apparent. This leakage current also contains a $1/f$ noise generator. We have

$$I_G = I_R + I_D \quad \text{and} \quad f S_{IG} = f S_{IR} + f S_{ID} = A \cdot I_D^2 + B \cdot I_R^2$$ \hspace{1cm} (5.18)

Here, $S_{IR}$ and $S_{ID}$ are the $1/f$ current noise stemming from the parallel leakage resistance and the Schottky barrier, respectively, $A$ is the relative $1/f$ current noise of the Schottky barrier and $B$ the relative $1/f$ current noise of the leakage resistor at $f = 1$ Hz. $I_R$ and $I_D$ are the current through the parallel leakage resistance and the Schottky barrier, respectively. We have 4 possibilities.

a) The gate conductance and the $1/f$ noise are dominated by the parallel leakage resistance, $S_{IR} > S_{ID}$ and $I_R > I_D$, so that $S_{IG} \approx S_{IR} \propto I_R^2 \equiv I_G^2$.

b) The conductance and the $1/f$ noise are dominated by the Schottky barrier, $S_{IR} < S_{ID}$ and $I_R < I_D$, so that $S_{IG} \equiv S_{ID} \propto I_D^2 \equiv I_G^2$.

c) The conductance is dominated by the resistance and the $1/f$ noise by the Schottky barrier, $S_{IR} < S_{ID}$ and $I_R > I_D$, so that

$$S_{IG} = S_{ID} \propto I_D^2 = I_0^2 \left[ \exp \left( I_R R_p / \eta V_{th} \right) - 1 \right]^2 \propto \left[ \exp \left( I_G R_p / \eta V_{th} \right) - 1 \right]^2$$

d) The conductance is dominated by the Schottky barrier and the $1/f$ noise by the resistance, $S_{IR} > S_{ID}$ and $I_R < I_D$, so that (if $I_D > I_0$)

$$S_{IG} = S_{IR} \propto I_R^2 = \left[ \eta V_{th} / R \cdot \ln (I_D / I_0) \right]^2 \propto \ln^2 (I_D) \equiv \ln^2 (I_G).$$

Here $V_{th}$ is the thermal voltage.

In Fig. 5.10 we observed that at high currents all devices follow a square law. From Fig. 5.9 we know that for high currents the Schottky barrier determines the $I$-$V$ characteristic, so we have situation b). At low currents we observed that the devices 2T4 and 7T4 show a deviation from the square law. At the lowest currents the noise tends to follow a square law again for these devices. At the lowest currents we know from Fig. 5.9 that the parallel leakage resistance determines the $I$-$V$ characteristics of device 2T4 and 7T4, so we have situation a). At intermediate currents we have situation d) for the devices 2T4 and 7T4. The solid lines of the transistors 2T4 and 7T4 represent the best fit with (5.18) using the values of $\eta$, $I_0$, and $R_p$ given in Table 5.2. The fitting parameters are $A$ and $B$ and are also given in Table 5.2.

The other devices incorporated in this study show similar behavior both with respect to the $I$-$V$ curves and with respect to the $1/f$ noise in the gate current.

In Fig. 5.11 the relative noise in the gate current $S_{IG} / I_G^2$ is plotted versus the gate width $W_G$ of a series of MIX5 devices. We observe that the relative gate current noise is inversely proportional to the gate width. Since the gate length of all MIX5 devices is 0.2 $\mu$m, the gate area is proportional to the gate width. If the gate-current density is homogeneously distributed over the gate-area and if the noise sources are
homogeneously distributed across the gate-area and spatially uncorrelated we have [7]

\[ S_{I_G}/I_G^2 \propto A_G^{1} \]  

(5.19)

where \( A_G \) is the gate area. Since (5.19) agrees with the experimental results of Fig. 5.11 we conclude that in all probability the noise sources are homogeneously distributed across the gate area (at least with respect to the gate width).

Table 5.2 extracted data gate Schottky barrier

<table>
<thead>
<tr>
<th></th>
<th>( \eta )</th>
<th>( R_p (\Omega) )</th>
<th>( I_0 (A) )</th>
<th>( A )</th>
<th>( B )</th>
</tr>
</thead>
<tbody>
<tr>
<td>FHX31</td>
<td>1.3</td>
<td>1.4 \times 10^8</td>
<td>1.0 \times 10^{-15}</td>
<td>1.8 \times 10^{-9}</td>
<td>- *)</td>
</tr>
<tr>
<td>2T4</td>
<td>2.7</td>
<td>3.4 \times 10^5</td>
<td>4.0 \times 10^{-9}</td>
<td>1.2 \times 10^{-8}</td>
<td>1.8 \times 10^{-7}</td>
</tr>
<tr>
<td>2T5</td>
<td>1.7</td>
<td>- *)</td>
<td>2.0 \times 10^{-11}</td>
<td>1.2 \times 10^{-8}</td>
<td>- *)</td>
</tr>
<tr>
<td>7T4</td>
<td>2.6</td>
<td>3.0 \times 10^5</td>
<td>3.0 \times 10^{-9}</td>
<td>3.9 \times 10^{-8}</td>
<td>2.3 \times 10^{-6}</td>
</tr>
<tr>
<td>7T5</td>
<td>3.3</td>
<td>7.0 \times 10^6</td>
<td>5.0 \times 10^{-9}</td>
<td>4.0 \times 10^{-7}</td>
<td>- *)</td>
</tr>
</tbody>
</table>

*) the symbol - means value could not be determined from our experimental data

Fig. 5.11 Relative noise in the gate current versus the gate width \( W_G \).

In order to get information about the homogeneity with respect to the gate length we study the noise in the gate current as a function of the drain-source bias. When a drain-source bias is applied the current distribution across the gate is no longer homogeneous. If the drain bias is low, i.e. the channel is ohmic, we can calculate the current density distribution.

\[ J(x) = \frac{I_0}{A_G} \exp \left( \frac{V(x)}{\eta V_{th}} \right) \text{ with } V(x) = V_0 - R_{ss} I_S - \frac{V_{ch}}{L_G} x \]  

(5.20)
Experimental results obtained from the Schottky barrier

where $V_0$ is the applied gate-source bias, $x$ is the position in the channel ($x = 0$ at the source side of the channel), $R_{ss}$ is the series resistance at the source side, $I_S$ is the source current, and $V_{ch}$ is the voltage across the channel resistance, i.e. $V_{ch} = V_{DS} - I_D R_s - I_G R_{ss}$, where $R_s$ is the total series resistance, $I_D$ is the drain current, and $I_G$ is the gate current.

The total gate current is

$$I_G = W_G \frac{L_G}{0} J(x) dx = \frac{I_0 \eta V_{th}}{V_{ch}} \left[1 - \exp \left(\frac{-V_{ch}}{\eta V_{th}}\right)\right] \exp \left(\frac{V_0 - R_{ss} I_S}{\eta V_{th}}\right)$$

(5.21)

This calculation is only valid if the gate current is small enough, i.e. the extra voltage drop $\Delta V$ across the channel due to the gate current is much smaller than $\eta k T / q$. Thus $\Delta V < I_G R_{ch} \ll \eta k T / q$.

If the noise sources are spatially uncorrelated and distributed homogeneously across the gate area (with respect to $x$), the $1/f$ noise is given by

$$S_{I_G} \propto \int_0^{L_G} J^2(x) dx \propto \frac{1}{V_{ch}} \left[1 - \exp \left(-2 \frac{V_{ch}}{\eta V_{th}}\right)\right] \exp \left(\frac{2V_0 - 2R_{ss} I_S}{\eta V_{th}}\right)$$

(5.22)

or

$$\frac{S_{I_G}}{I_G^2} \propto \frac{1 - \exp \left(-2 \frac{V_{ch}}{\eta V_{th}}\right)}{\left[1 - \exp \left(- \frac{V_{ch}}{\eta V_{th}}\right)\right]^2} V_{ch}$$

(5.23)

In Fig. 5.12 a plot is presented of the relative $1/f$ noise in the gate current versus $V_{ch}$. The solid line represents (5.23) where the value for $\eta$ is found from the $I$-$V$ characteristic of the gate. We observe that there is an excellent agreement between (5.23) and the experimental results, so we conclude the $1/f$ noise sources are homogeneously distributed across the gate area.

![Fig. 5.12 Relative 1/f noise in the gate current versus $V_{ch}$. The gate current is kept constant at $7.4 \times 10^{-7}$ A.](image-url)
Here it should be noted that a comparison of the $1/f$ noise in the gate current between the MIX5 devices and the devices presented in Table 5.2 can only be made taking into account the gate area that is different for all devices (see section 5.4.C).

**B. Origin of the $1/f$ noise in the Schottky barrier**

Our experiments show that the gate current noise $S_{IG}$ is proportional to $I_{G}^{2}$. From the gate area dependence and the dependence on the applied drain-source bias we found that in all probability the noise sources are homogeneously distributed across the gate area (see Fig. 5.11 and Fig. 5.12).

When mobility fluctuations cause the $1/f$ noise we have [8]

$$S_{IG} \propto I_{G} \sqrt{V_{D} - V} \quad (5.24)$$

where $V_{D}$ is the diffusion voltage, and $V$ the applied voltage across the Schottky barrier. Hence our experimental results can not be interpreted in terms of mobility fluctuations.

Eq. (5.24) is derived for a Schottky barrier where no interfacial oxide is present at the metal semiconductor interface. In view of the high values of the ideality factor observed for the gate $I$-$V$ characteristics and the fact that in the production process of these MODFETs there is no treatment for removal of an eventual interfacial oxide, we expect a native oxide layer to be present. This interfacial oxide can be responsible for the gate current noise. One of the $1/f$ noise models predicting $S_{I} \propto I^{2}$ is the tunnel diode model proposed by Kleinpenning [9], [10] as described previously in chapter 3. Another model is the “two step tunneling” model proposed by Kumar et al. [11] as described in chapter 3. Both models predict fluctuations in the transparency of the oxide for electrons.

The following calculation yields a relation between the relative noise in the transparency and the relative noise in the short-circuit gate current.

The forward $I$-$V$ characteristic of a not too heavily doped Schottky barrier is dominated by three mechanisms, i.e. thermionic emission of electrons over the barrier, drift and diffusion in the space charge region, and tunneling through the interfacial oxide. The thermionic emission and drift-diffusion mechanism are considered to be in series [12].

For the drift-diffusion current we can write

$$I_{d} = \frac{A_{g} k T \mu N_{c} \left[ \exp \left( \frac{q V}{k T} \right) - \exp \left( \frac{q \xi(x_{m})/k T}{x_{m}} \right) \right]}{\int_{x_{m}}^{W} \exp \left( \frac{q E_{c}/k T}{x} \right) dx} \quad (5.25)$$

where $N_{c}$ is the effective density of states in the conduction band, $\xi(x_{m})$ the quasi-Fermi-level of electrons at the barrier maximum located at position $x_{m}$, $W$ the width of the space charge region, $E_{c}$ the conduction band energy, $V$ the applied bias to the barrier, $\mu$ the mobility of electrons, and $A_{g}$ the barrier area. The thermionic emission current density can be described as [12]

$$J_{te} = q v_{f} \left[ n(x_{m}) - n_{0}(x_{m}) \right] \quad (5.26)$$
where $v_r$ is a "recombination velocity" of electrons on the top of the barrier, $n_0(x_m)$ the equilibrium electron density at the top of the barrier at zero bias, and $n(x_m)$ the electron density at bias $V$.

The interfacial layer leads to a reduction of the "recombination velocity" $v_r$ due to the electron tunneling probability $t_n$. In this case the current density $J_{te}$ and the current $I_{te}$ are given by

\[ J_{te} = qv_r t_n [n(x_m) - n_0(x_m)] \]  \quad (5.27)

\[ I_{te} = q A G N_c v_r t_n \exp(-q \phi_b/kT) \{ \exp[q \xi(x_m)/kT] - 1 \} \]  \quad (5.28)

In (5.28) the bias dependence of $n_0$ due to a bias dependent barrier height is neglected. This approximation limits the validity of (5.28) to biases well above $kT/q$, which is the bias range of interest for our noise analysis.

Combination of (5.25)-(5.28) yields the total current $I$ to be

\[ I = \frac{q A G N_c v_r t_n \exp(-q \phi_b/kT) \{ \exp(qV/kT) \}}{1 + \frac{v_r t_n}{v_d}} \]  \quad (5.29)

where $v_d$ is the effective velocity due to drift and diffusion of electrons at the top of the barrier given by

\[ v_d = \left[ \frac{q}{\mu kT} \exp(-q \phi_b/kT) \int_{x_m}^{W} \exp(qE_c/kT) dx \right]^{-1} \]  \quad (5.30)

Now we can calculate the contribution of transparency fluctuations of the interfacial oxide to the short-circuit gate current fluctuations. Since $\Delta I = (dI/dt_n) \Delta t_n$, we have

\[ \frac{S_I}{I^2} = \left( \frac{d \ln I}{d \ln t_n} \right)^2 \frac{S_{t_n}}{t_n^2} = \left[ 1 + \frac{v_r t_n}{v_d} \right]^{-2} \frac{S_{t_n}}{t_n^2} \]  \quad (5.31)

In GaAs Schottky barriers generally the effective velocity due to drift and diffusion $v_d$ is high and the current voltage characteristic is dominated by thermionic emission [12]. As a consequence for our Schottky barriers the factor between square brackets in (5.31) is close to unity.

The tunnel diode model of Kleinpenning [9,10] predicts

\[ \frac{S_t}{t^2} = \frac{mqkT L^3}{3 \pi f \varepsilon A G V_0 h^2} \tan \delta \]  \quad (5.32)

where $t$ is the transparency of the oxide layer, $m$ the effective mass of the electron in the oxide, $L$ is the oxide thickness, $V_0$ is the barrier height, $\tan \delta$ is the loss factor of the oxide, and $\varepsilon$ the dielectric constant of the oxide.
Chapter 5. Low-frequency noise in MODFETs

In order to compare Eqs. (5.31) and (5.32) with experimental data we need an estimate of the barrier height $V_0$ and the oxide layer thickness $L$. For $V_0$, which is the difference between the conduction band of the oxide and the top of the Schottky barrier at $x_m$, we suppose $V_0 < 0.5$ V. If no special precautions are taken during the processing of the gate the thickness of the spontaneous interfacial layer easily reaches 10 Å. Another problem is the value of the effective mass and the dielectric constant. We use the bulk material values but we should bear in mind that in thin layers between conductive materials these values may deviate considerably from the bulk material values.

Using these values and with the help of the relation $S_i/t^2 \equiv S_i/t^2$ we can extract the values for $\tan \delta$. For example for transistor Q12 we obtain an upper limit of $\tan \delta = 0.5$. The other devices will be discussed in section 5.4C. This value is rather high compared to the values obtained for bulk oxide material (e.g. quartz: $\tan \delta = 10^{-4}$), but more reasonable for thin films. The same order of magnitude of $\tan \delta$ is found in the polysilicon emitter bipolar transistors as described in chapter 3.

Here a few remarks should be made:

1) In the derivation of (5.32) image force lowering of the barrier is neglected. Image force lowers the effective barrier height significantly for thin oxide layers. Neglecting this leads to an overestimate of $\tan \delta$.

2) Eq. (5.32) is derived for the case that the applied bias across the interfacial layer is small compared to the barrier height $V_0$. Since the barrier height $V_0$ is the difference between the bottom of the oxide conduction band and the top of the Schottky barrier at $x_m$, this condition may not always be satisfied. If the applied bias approaches $V_0$ the noise can be more than a factor 3 larger than predicted by (5.32) (see fig. 1. Ref. [10]).

3) The structure of the spontaneous oxide layer presumably is quite inhomogeneous at a detailed scale much smaller than the gate area. Local oxide thickness variations constrict the current to the thinner areas. In this case Eq. (5.32), which applies for a homogeneous oxide layer, cannot be used.

4) The ideality factor depends on the oxide layer thickness. So according to (5.32) a higher ideality factor goes hand in hand with a higher 1/f noise. This is not confirmed by our experiments (see for example Table 5.2). However this relation can only be expected if the oxide structure is the same for all transistors. This is presumably not the case as mentioned before.

Another interpretation for barrier height or transparency fluctuations is the two-step tunneling model [11]. Here carriers are trapped in states at the semiconductor-oxide interface. The second step is a tunneling process to states within the oxide layer. The noise contribution of each individual trap has a lorentzian power spectral density, whose characteristic time constant depends on the position in the oxide and the energy level of the trap. When the trap distribution within the oxide is homogeneous with respect to the depth in the oxide or with respect to the energy level distribution of the traps around the Fermi-level, the power spectral density of the transparency fluctuations has a 1/f frequency dependence.
Experimental results obtained from the Schottky barrier

The high effective velocity due to drift-diffusion $v_d$ also suppresses the contribution of mobility fluctuations to the gate current noise. As can be concluded from (5.30) mobility fluctuations lead to fluctuations in $v_d$. A similar calculation that leads to (5.31) gives a relation between current fluctuations and fluctuations in $v_d$

$$\frac{S_{IG}}{I_G^2} = \left[1 + \frac{v_d}{v_tr_n}\right]^{-2} \frac{S_{vd}}{v_d^2}$$

(5.33)

Now the prefactor in (5.33) is much smaller than 1, since the sum between square brackets in (5.33) is much larger than 1. Hence the contribution of mobility fluctuations is attenuated by the presence of an interfacial oxide.

C. Comparison of devices.

For the AlGaAs/GaAs devices we observe that the plasma etched gates (7T4 and 7T5) have a slightly higher 1/f noise than the fluid etched devices (see Table 5.2). In order to make a comparison between these and the other devices we need to take into account the fact that the gate area is different for different devices. We assume that the 1/f noise sources are homogeneously distributed over the emitter area for all devices. Hence we compare the values of the normalized 1/f noise $\beta = f A_G S_{IG} / I_G^2$ for all devices ($A_G$ in $\mu m^2$). The value of $\beta$ for the AlGaAs/GaAs devices is in the range of $2 \cdot 10^{-7}$ - $10^{-5}$ $\mu m^2$. The AlGaAs/GaAs devices with InGaAs channel have the lowest 1/f noise with $\beta$ in the range of $8 \cdot 10^{-9}$ - $2 \cdot 10^{-8}$ $\mu m^2$. The values obtained for the MIX5 devices are about $10^{-6}$ $\mu m^2$, for the FHX31 we obtained $1.4 \cdot 10^{-7}$ $\mu m^2$.

There is a large spread of about a factor $10^3$ in $\beta$-values between the devices. In terms of the transparency fluctuation model we ascribe this spread to a spread in the oxide layer thickness and microscopic inhomogeneities of the oxide layer (see remark 3 in section 5.4 B). According to (5.32) the relative current noise is proportional to the oxide layer thickness cubed, so a small spread in thickness leads to a large spread in the relative current noise. If the oxide layer contains the dominant noise generator it is mainly the treatment prior to metal deposition that determines the 1/f noise properties of the gate Schottky barrier rather than the technique used for the definition of the gate area. Apart from the process of oxide formation only the choice of the semiconductor layer underneath the metal might affect the 1/f noise properties of the gate.

5.5 CONCLUSIONS

We have investigated the $I-V$ characteristics and low-frequency noise of MODFETs made with different gate etching processes and different semiconductor materials. Both the properties of the 2DEG channel and the gate Schottky barrier have been studied. The 1/f noise in the channel can be described by the Hooge relation with a constant value of $\alpha$. Comparison of the $\alpha$-values for the 1/f noise in the channel between
devices with different channel materials learns that the lowest $\alpha$-values are approximately equal to $10^{-4}$. These values are obtained for both GaAs channels and InGaAs channels. These lowest values are in agreement with values reported in literature.

We have presented a method to determine whether the dominant 1/f noise generator is located in the 2DEG channel or in the series resistance. We have demonstrated that measuring the 1/f noise makes it possible to extract the values of the threshold voltage and the series resistance, provided that the 1/f noise stems from the 2DEG channel and not from the series resistance.

We interpreted the 1/f noise in the gate current in terms of transparency fluctuations of electrons tunneling through the interfacial oxide between the metal contact and the semiconductor layer underneath. These transparency fluctuations are caused by the Nyquist noise in the oxide layer. The transparency fluctuations have a 1/f spectral density if the loss tangent of the oxide is frequency independent over a wide range of frequencies. The loss tangent values we calculate are high compared to the values reported for bulk oxide materials, but the values are comparable with data of thin films. Furthermore the values for tan $\delta$ are comparable to the values we calculated for polysilicon emitter bipolar transistors in chapter 3 of this dissertation. Another interpretation giving reasonable results is the two step tunneling model where carriers tunnel through the oxide layer via traps. In order to have a 1/f spectral density specific requirements have to be fulfilled for the distribution of traps within the oxide.

Due to the fact that the presumably present oxide layers are native and hence may have a very different structure from device to device, it is difficult to be conclusive about a possible impact of the gate etching process or semiconductor material choice on the 1/f noise in the gate current.

Acknowledgment
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Appendix

PARAMETER EXTRACTION ACCURACY

For the analysis of the low-frequency noise in MODFETs it is essential to have accurate values of the threshold voltage and the series resistance. Obtaining these values from the $I$-$V$ characteristics is difficult as shown in section 5.3A. The methods using the 1/f noise look promising. Now it is interesting to have an estimate of the accuracy of these methods.

The parameters $V_T$ and $R_s$ are extracted from intersections of straight lines through a series of measurement points. Let the straight line passing through a series of $N$ data points $(x_1, y_1), (x_2, y_2), \ldots, (x_N, y_N)$ be given by
\[ y = a + bx \]

The intersection and the slope are calculated from

\[
a = \frac{\sum w_i x_i^2 \sum w_i y_i - \sum w_i x_i \sum w_i y_i}{\Delta}
\]

\[
b = \frac{\sum w_i \sum w_i x_i y_i - \sum w_i x_i \sum w_i y_i}{\Delta}
\]  

(A5.2)

Here \( \Delta = \sum w_i \sum w_i x_i^2 - (\sum w_i x_i)^2 \), \( w_i = 1/\sigma_i^2 \), and the symbol \( \Sigma \) represents the summation from 1 to \( N \).

The weighted mean for \( x \) is defined as

\[
\langle x \rangle = \frac{\sum w_i x_i}{\sum w_i}
\]  

(A5.3)

In order to facilitate the calculation of the error we transform the \( x \) coordinate, so that the weighted mean \( \langle x \rangle \) is at the origin.

\[
x' = x - \langle x \rangle
\]

\[
y = a' + bx'
\]  

(A5.4)

where \( a' \) is the height at the position \( \langle x \rangle \). After this transformation the errors in \( a' \) and \( b \) are uncorrelated [13].

We are interested in the error of the value of \( x \) for \( y = 0 \). The error in \( x \) is equal to the error in \( x' \). The error in \( x' \) can be calculated with the principle of error propagation. The error in the quantity \( p \) due to an error in \( q \) is given by

\[
\sigma_p = \left| \frac{dp}{dq} \right| \sigma_q
\]  

(A5.5)

For the error in \( x \), which is equal to the error in \( x' \), we obtain

\[
\sigma_x^2 = \sigma_{x'}^2 = \left( \frac{\partial x}{\partial a'} \right)^2 \sigma_{a'}^2 + \left( \frac{\partial x}{\partial b} \right)^2 \sigma_b^2
\]  

(A5.6)

With \( y = 0 \) we get

\[
\sigma_x^2 = b^{-2} \left[ \sigma_{a'}^2 + \left( \frac{a'}{b} \right)^2 \sigma_b^2 \right]
\]  

(A5.6)

The errors in the parameters \( a' \) and \( b \) are given by

\[
\sigma_{a'}^2 = (\sum w_i)^{-1} \quad \text{and} \quad \sigma_b^2 = \left[ \sum \left( w_i x_i' \right)^2 \right]^{-1}
\]  

(A5.7)

We elaborate (A5.6) for the case of a constant fractional error in \( y \), so we have \( \sigma_i = \sigma_0 \cdot y_i \). Combination of (A5.6) and (A5.7) leads to
Expression of the error $\sigma_x$ in terms of $a$, $b$, and $x$ of (A5.1) yields

$$\sigma_x = \frac{\sigma_0}{b} \sqrt{\frac{1}{\sum y_i^{-2} + \frac{a^2}{b^2 \sum \left( \frac{x_i}{y_i} \right)^2}}} \tag{A5.8}$$

An estimate for the value of $\sigma_0$ can be made as follows. On the vertical axes of Fig. 5.3 and Fig. 5.4 the value is plotted of $S_{\nu \nu DS}/I_D^2$ raised to the power 1/3 and -1/3, respectively. Hence with the principle of error propagation we find that the fractional error of $\left( S_{\nu \nu DS}/I_D^2 \right)^{1/3}$ is 1/3 of the fractional error of $S_{\nu \nu DS}/I_D^2$.

The low-frequency noise is measured and the power spectral density is plotted versus the frequency on a double logarithmic plot. Then a $1/f$ slope is fitted to the data at low-frequency. The error of a reading of the $1/f$ noise from a double logarithmic plot is estimated at ±0.5 dB, which is a fractional error of 12%. So a reasonable estimate of the value of $\sigma_0$ is 0.04, i.e. 1/3-12%.

References


Chapter 6

LOW-FREQUENCY NOISE IN GATE-ALL-AROUND MOSFETS

6.1 INTRODUCTION

Dual-gate Silicon-on-Insulator (SOI) MOSFETs provide an increase in the transconductance of at least a factor two compared to standard single gate SOI transistors at equal effective gate voltage [1]-[4]. Other features include a nearly ideal subthreshold slope [2], reduced short channel effect [1], and absence of the kink effect in n-channel devices. From Gate-All-Around (GAA) structures the low-frequency noise is reported to be low compared to single gate SOI transistors [5]. The low-frequency noise in p-channel GAA devices is the subject of this chapter.

In Fig. 6.1 a schematic representation is given of the structure of the GAA MOSFET. The shaded gate is all around the channel.

![Fig. 6.1 Schematic representation of a GAA MOSFET](image)

We studied the DC characteristics and the low-frequency noise of two devices made on the same wafer. The devices are made by IMEC (Louvain Belgium). Both devices have a gate width $W$ of 4 µm. The gate length is 3 µm for transistor T1 and 5 µm for transistor T2. The thickness of the channel silicon film $t_{si}$ is 100 nm. The channel is doped with donors at a concentration of $N_D = 5 \cdot 10^{16}$ cm$^{-3}$. The gate oxide thickness $t_{ox}$ is 50 nm.

All measurements are carried out at room temperature.

6.2 DC CHARACTERISTICS

The drain current at low drain-source bias (ohmic region) is given by

$$I_D = \frac{2C_{ox}\mu_{eff}W|V_{GS} - V_T|V_{ds}}{L}$$ (6.1)
where $V_{ds}$ is the voltage across the channel which is equal to the applied drain-source voltage $V_{DS}$ minus the voltage drop across the series resistance, $V_{GS}$ is the applied gate-source voltage, $V_t$ is the threshold voltage, $C_{ox}$ is the oxide capacitance per unit area, and $\mu_{eff}$ the effective mobility in the channel.

The effective mobility in (6.1) is given by

$$\mu_{eff} = \frac{\mu_0}{1 + \theta |V_{GS} - V_t|}$$

(6.2)

where $\mu_0$ is the mobility for $V_{GS} = V_t$, and $\theta$ is the mobility degradation factor.

In the appendix the following expression is derived for the drain current as a function of the applied drain-source voltage for the transistor in strong inversion

$$I_D = \frac{2\beta_0 |V_{GS} - V_t| V_{DS}}{1 + (\theta + 2\beta_0 R_s) |V_{GS} - V_t|} \text{ with } \beta_0 = \mu_0 C_{ox} W/L$$

(6.3)

where $R_s$ is the sum of the source and drain series resistance. In the calculation it is assumed that the series resistances at the source and drain side are equal.

In Fig. 6.2 a plot is presented of the drain-source conductance $G_{DS}$ measured in the ohmic region versus the applied gate-source bias $V_{GS}$. We observe that the ratio between the conductance of T1 and T2 is approximately equal to the ratio of the gate lengths 5/3.

![Fig. 6.2](image)

Fig. 6.2 Plot of drain-source conductance $G_{DS}$ in the ohmic region versus the applied gate-source bias $V_{GS}$ for transistor T1 and T2.

The threshold voltage is determined with the so-called double derivative extraction method [7]. The second derivative of the channel current $I_D$ to $V_{GS}$ is calculated after the $I_D$ versus $V_{GS}$ curve was smoothed with the help of a moving average method. The result is plotted in Fig. 6.3. We observe that the extreme of the derivative of the transconductance is obtained at the same gate-source bias for both transistors. The threshold voltage $V_t$ is found to be -1.4 V.
One of the features of the Gate-All-Around structure is a nearly ideal sub-threshold curve. In Fig. 6.4 a plot $I_{DS}$ versus $V_{GS}$ at constant $V_{DS}$ of the sub-threshold region is made. We obtain $I_{DS} \propto \exp(qV_{GS}/\eta kT)$ with $\eta = 1.20$ for T1 and $\eta = 1.15$ for T2, so that the slope is $1.2 \cdot kT/q = 70 \text{ mV/decade}$ for T1 and $1.15 \cdot kT/q = 67 \text{ mV/decade}$ for T2.
With the help of (6.3) we obtain for the resistance between drain and source

\[ R_{DS} = \frac{V_{DS}}{I_D} = \frac{1}{2 \beta_0 |V_{GS} - V_t|} + R_s + \frac{\theta}{2 \beta_0} \]  

(6.4)

In Fig. 6.5 a plot is made of \( R_{DS} \) versus the reciprocal effective gate voltage \( 1/|V_{GS} - V_t| \).

This plot is linear and from the intersection \( R_{DS0} \) with the vertical axis \( (V_{GS} = V_t) \) we determine the value of

\[ R_{DS0} = R_s + \frac{\theta}{2 \beta_0} \]  

(6.5)

The values for \( R_s \), \( \theta \), and \( \beta_0 \) are determined as follows. From the slope of the plot we determine the value of \( (2 \beta_0)^{-1} \). This value can be substituted in (6.5).

Since our devices are made on the same wafer we assume that the mobility degradation factor \( \theta \) is equal for both devices. Both devices have equal gate width \( W \) so that we expect the series resistance of both devices to be equal.

With the two values for the intersection \( R_{DS0} \) in Fig. 6.5 we have two equations in the two variables \( R_s \) and \( \theta \). Solution yields \( R_s = 2 \text{ k}\Omega \) and \( \theta = 0.13 \text{ V}^{-1} \). This value found for \( \theta \) is comparable to values reported in literature [8].

### 6.3 LOW-FREQUENCY NOISE

The low-frequency drain-source voltage noise measurements were carried out on the devices biased in the ohmic region. The spectral density was measured in the frequency range from 3 Hz to 20 kHz. In Fig. 6.6 a typical plot is presented of the spectral density of the drain-source voltage fluctuations versus the frequency. The solid lines represent de decomposition of the spectrum in a \( 1/f \) component and two generation-recombination (g-r) noise components. The white noise \( 4kT R = 3.7 \cdot 10^{-16} \)
Low-frequency noise

$V^2/\text{Hz}$ is not shown in Fig. 6.6 because the value is below the lowest $g$-$r$ noise. In the ohmic region the two $g$-$r$ noise time constants $\tau$ were found to be independent of $V_{DS}$ and $V_{GS}$. The $1/f$ noise intensity and the plateau levels of both Lorentzians are proportional to $V_{DS}^2$, showing that we are dealing with resistance noise. At some biasing conditions the spectra did not show an exact $1/f$ slope at low frequencies. In these cases a Lorentzian-like component was observed. However the shape of this bulge was not clear enough to identify it as a third $g$-$r$ noise component. For this reason the accuracy of the extracted values for the $1/f$ component is not always very high. The Lorentzian with the lower time constant could not be determined very accurately either because its cut-off frequency is close to the maximum frequency of our measurements.

![Figure 6.6](image)

**Fig. 6.6** A typical low-frequency noise spectrum of T1, $V_{GS} = -2.9 \text{ V}$, $V_{DS} = -59 \text{ mV}$, and $I_D = 2.6 \mu\text{A}$.

A. 1/f Noise

For the determination of the location of the dominant noise generator we can use the method presented in paragraph 5.3. We have

$$
\frac{S_{V_{DS}}}{I_D^2} = S_{R_s} + S_{R_{ch}}
$$

(6.6)

where $S_{R_s}$ is the $1/f$ noise in the series resistance and $S_{R_{ch}}$ is the $1/f$ noise in the channel. With the help the relation of Hooge [9] we find

$$
S_{R_{ch}} = \frac{\alpha_{ch} R_{ch}^2}{f N_{ch}} = \frac{\alpha_{ch} q \mu_{\text{eff}} R_{ch}^3}{f L^2}
$$

(6.7)

Here we used the following expression for the number of carriers in the channel $N_{ch}$.
\[ N_{ch} = \frac{L^2}{q\mu_{eff} R_{ch}} \]  

(6.8)

where \( L \) is the channel length. The effective mobility \( \mu_{eff} \) depends on the effective gate voltage.

It should be mentioned that the Hooge relation applied in (6.7) is valid for homogeneous samples only. In the channel of the MOSFET the mobility and presumably the \( \alpha \)-value are position dependent. So in (6.7) we have an effective \( \alpha_{ch} \)-value.

\( S_{R_{ch}} \) is proportional \( R_{ch}^3 \). The \( 1/f \) noise \( S_{Rs} \) is independent of the applied gate-source bias and hence independent of the channel resistance \( R_{ch} \).

In Fig. 6.7 a plot is made of \( S_{V_{DS}}/I_D^2 \) versus the channel resistance \( R_{ch} \).

![Fig. 6.7 Plot of the 1/f noise \( S_{V_{DS}}/I_D^2 \) versus the channel resistance \( R_{ch} \).](image)

We do not observe a part where \( S_{V_{DS}}/I_D^2 \) is independent of \( R_{ch} \), so we conclude that the \( 1/f \) noise stems from the channel. The solid lines in Fig. 6.7 have a slope 3. The values of \( S_{V_{DS}}/I_D^2 \) are very close to these lines, so that with the help of (6.7) we conclude that the product \( \alpha_{ch}\mu_{eff} \) is only a weak function of the gate-source bias and thus of the channel resistance.

The value of \( \mu_{eff} \) as a function of the effective gate-source voltage is obtained from

\[ \mu_{eff} = \frac{L}{2C_{ox} W \left| V_{GS} - V_t \right|} \]

(6.9)

In Fig. 6.8 the effective mobility is plotted versus \( |V_{GS} - V_t| \) for transistor T2. The plot for T1 is similar. For the calculation of \( C_{ox} = \varepsilon_{ox}/t_{ox} \), where \( t_{ox} \) is the oxide thickness, we took \( \varepsilon_{ox} = 3.5 \times 10^{-13} \) F/cm.
With the help of (6.7) and the results in Fig. 6.8 the Hooge parameter $\alpha_{ch}$ can be determined. In Fig. 6.9 the noise parameter $\alpha_{ch}$ is plotted versus the effective gate voltage. We observe that $\alpha_{ch}$ is almost independent of the effective gate voltage. This experimental fact is in agreement with results for p-MOSTs in literature [10]. The extracted $\alpha_{ch}$-values $9 \cdot 10^6$ and $1.7 \cdot 10^5$ are not too far apart, so $\alpha_{ch}$ could be considered as a material constant. Also the values of $\alpha_{ch}$ are comparable to values reported in literature that are in the range of $10^{-6}$-$10^{-4}$ in [11].

Fig. 6.8 Plot of calculated values of $\mu_{eff}$ versus the effective gate-source voltage of transistor T2.

Fig. 6.9 A plot of the extracted 1/f noise parameter $\alpha_{ch}$ versus the effective gate-source voltage.
B. G-R Noise

We have found two Lorentzians in the noise spectra for both T1 and T2. Hence the g-r spectra can be described by the relation

\[ S_{VDS} = \sum_{i=1}^{2} \frac{P_i}{1 + \omega^2 \tau_i^2} \]  \hspace{1cm} (6.10)

where \( P_i \) is the plateau level of component \( i \), and \( \tau_i \) its time-constant. The levels \( P_1 \) and \( P_2 \) are found to be proportional to \( I_D^2 \). The frequency is given by \( \omega = 2\pi f \). The time constants are \( \tau_1 = 1.4 \times 10^{-4} \) s and \( \tau_2 = 5 \times 10^{-6} \) s for transistor T1. For T2 we found \( \tau_1 = 1.2 \times 10^{-4} \) s and \( \tau_2 = 1 \times 10^{-5} \) s.

In order to find the location of the g-r noise sources we follow a similar procedure as for the 1/f noise (6.6). In Fig. 6.10 the plateau \( S_{VDSS0} / I_D^2 = P_i / I_D^2 \) of the g-r noise components is plotted versus the effective gate-source voltage.

![Figure 6.10](image)

Fig. 6.10 Plot of the plateau \( S_{VDSS0} / I_D^2 \) versus the effective gate-source bias.

If the g-r noise is generated in the series resistance we expect that the plateau \( S_{VDSS0} / I_D^2 \) is independent of the effective gate-source bias because the carrier concentration and the effective trap density are independent of the effective gate-source voltage in the series resistance. In Fig. 6.10 no gate-source voltage independent part is observed so the g-r noise stems from the channel.

In order to interpret the g-r results we consider the band diagram of the channel perpendicular to the current flow, that is given in Fig. 6.11. The channel thickness is given by \( t \), \( E_c \) is the conduction band, \( E_D \) is the donor energy level, \( E_F \) is the Fermi-level, \( E_v \) is the valence band, and \( E_t \) is a possibly present trap energy level.

The number of holes in the channel \( N_{ch} \) is given by
Low-frequency noise

\[ N_{ch} = WL \int_0^t p(x)dx = \frac{I^2}{q\mu_{eff}R_{ch}} \]  

(6.11)

where \( p(x) \) is the hole concentration at position \( x \). The fluctuations in the number of holes due to trapping and de-trapping are given by

\[ \Delta N_{ch} = WL \int_0^t \Delta p(x)dx \]  

(6.12)

Fig. 6.11 Band diagram of the channel perpendicular to the current flow.

For number fluctuations we have at constant current \( V_{ds} \propto R_{ch} \propto 1/N_{ch} \) and thus

\[ \frac{\Delta V_{ds}}{V_{ds}} = \frac{\Delta V_{DS}}{V_{ds}} = \frac{\Delta N_{ch}}{N_{ch}} \]  

(6.13)

The spectral density of the voltage noise is given by

\[ S_{VD_{S}} = \left( \frac{V_{ds}}{N_{ch}} \right)^2 S_{N_{ch}} \]  

(6.14)

Using (6.13) we obtain for the variance

\[ \left\langle \Delta N_{ch}^2 \right\rangle = \int_0^{\infty} S_{N_{ch}}(f)df = \left( \frac{N_{ch}}{V_{ds}} \right)^2 \int_0^{\infty} S_{V_{DS}}(f)df \]  

(6.15)

For a spectrum with two Lorentzians we obtain with (6.10)

\[ \int_0^{\infty} S_{V_{DS}}(f)df = \left\langle \Delta V_{DS}^2 \right\rangle = \sum_{i=1}^{2} \frac{P_i}{4\tau_i} \]  

(6.16)

To analyze the g-r results we consider the variance. The magnitude \( \left\langle \Delta N_{ch}^2 \right\rangle \) can be at most equal to \( N_{ch} \). With the help of the Eqs. (6.15) and (6.16) we find the variance \( \left\langle \Delta N_{ch}^2 \right\rangle \) to be of the order of magnitude of \( 10^2 \) for the spectrum in Fig. 6.6.
With the help of (6.11) we find \( N_{ch} \equiv 10^5 \) for T1 at the biasing conditions given in Fig. 6.6. So \( \langle \Delta N_{ch}^2 \rangle \ll N_{ch} \). For all studied biasing conditions we find \( \langle \Delta N_{ch}^2 \rangle \ll N_{ch} \) for both transistors.

From (6.15) and (6.16) we deduce

\[
\frac{\langle \Delta N_{ch}^2 \rangle}{N_{ch}^2} = \frac{2}{N_{ch}^2} \frac{\sum_i P_i / 4 \tau_i}{V_{ds}^2} = \frac{\langle \Delta V_{DS}^2 \rangle}{V_{ds}^2}
\]

(6.17)

In general we have for the variance in g-r processes

\[
\langle \Delta N_{ch}^2 \rangle \propto N_{ch}^k \quad \text{with} \quad 0 \leq k \leq 1
\]

(6.18)

Combination of (6.17) and (6.18) yields

\[
\frac{\langle \Delta V_{DS}^2 \rangle}{V_{ds}^2} \propto N_{ch}^{k-2} \propto |V_{GS} - V_t|^{k-2}
\]

(6.19)

In Fig. 6.12 a plot is made of \( \frac{\langle \Delta V_{DS}^2 \rangle}{V_{ds}^2} \) versus the effective gate-source voltage.

![Plot](image.png)

**Fig. 6.12** Plot of the relative variance \( \frac{\langle \Delta V_{DS}^2 \rangle}{V_{ds}^2} \) versus \( |V_{GS} - V_t| \).

The solid lines have a slope of -2. We observe that the decrease in the relative variance is somewhat stronger than inversely proportional to the effective gate-source voltage squared: i.e. \( \frac{\langle \Delta V_{DS}^2 \rangle}{V_{ds}^2} \propto |V_{GS} - V_t|^{-2.5} \), and thus \( k \equiv -0.5 \).

For a possible explanation for \( k \) being smaller than zero we have to consider the regions of the main conductance and of the main g-r noise sources in the channel. The conductance is mainly concentrated in the edges at the oxide interface \( 0 \leq x \leq \lambda \),
and \( t - \lambda \leq x \leq t \) (see Fig. 6.11). The g-r noise is generated in the same edges. We have two possibilities.

i) The g-r noise is generated in the area very close to the oxide interface, i.e. \( x = 0 \) and \( x = t \). Here we have transitions of holes between the valence band and traps located in the oxide or at the oxide interface. Possibly we might have a trap distribution.

ii) The g-r noise is generated in the area around \( x = \lambda \) and \( x = t - \lambda \) where the trap level is close to the Fermi-level: we have transition of holes between the valence band and traps in the silicon. This might lead to a distribution of relaxation times [12].

In the first case i) we have [13]

\[ S_{N_{ch}} = \frac{4 \langle \Delta N_{ch}^2 \rangle \tau_{ox}}{1 + \omega^2 \tau_{ox}^2} \text{ with } \langle \Delta N_{ch}^2 \rangle = 2WLn_{t_{ox}}f_t(1-f_t) << N_{ch} \]

where \( n_{t_{ox}} \) is the oxide trap density which can be a function of the trap energy level, \( \tau_{ox} \) is the oxide trap relaxation time, and \( f_t \) is given by

\[ f_t^{-1} = 1 + \exp[(E_F - E_t)/kT] \]

where \( E_F \) is the Fermi-level and \( E_t \) the trap energy level.

If we suppose that the oxide trap density is constant with respect to the trap energy level we can calculate \( n_{t_{ox}} \) from the variance.

\[ \langle \Delta N_{ch}^2 \rangle = WLn_{t_{ox}} \int_{-\infty}^{\infty} f_t(1-f_t) d(E_F - E_t) = 2WLkTn_{t_{ox}} \]

We find using the data in Fig. 6.6 that \( n_{t_{ox}} \) is of the order of magnitude of \( 10^{10} \text{ cm}^{-2}\text{eV}^{-1} \), which is reasonable, compared to values reported in literature in the range of \( 8 \cdot 10^8 - 8 \cdot 10^9 \text{ cm}^{-2}\text{eV}^{-1} \) in [11].

In the second case ii) we have [12]

\[ S_{N_{ch}} = \frac{4 \langle \Delta N_{ch}^2 \rangle \tau_{si}}{1 + \omega^2 \tau_{si}^2} \text{ with } \tau_{si}^{-1} = \nu_{th}\sigma_tN_V \exp(E_t/kT) \]

where \( \tau_{si} \) is the trap relaxation time, \( \nu_{th} \) the thermal velocity, \( \sigma_t \) the capture cross-section, and \( N_V \) the density of states in the valence band.

The noise is generated in an area of the order of magnitude of the Debye length \( L_D \) around \( x = \lambda \) and \( x = t - \lambda \), where the Fermi-level intersects with the trap energy level. The length \( L_D \) around \( x = \lambda \) is roughly

\[ L_D = \frac{kT\varepsilon_{si}}{q^2[N_D + p(\lambda)]} \]

where \( \varepsilon_{si} \) is the dielectric constant of silicon. If we assume that around \( x = \lambda \) and \( x = t - \lambda \) the free hole concentration \( p(x) \) is smaller than the donor concentration we
obtain $L_D = 18$ nm. The concentration $p(\lambda)$ is smaller than the donor concentration if the trap energy level $E_t - E_v$ is larger than 0.13 eV.

An upper limit for the variance is then
\[
\frac{\langle \Delta N_{ch}^2 \rangle}{N_{ch}^2} \leq \frac{2p(\lambda)L_DWL}{\int_0^t p(x)dx} \ll 1
\]

(6.25)

In both cases i) and ii) the variance $\langle \Delta N_{ch}^2 \rangle$ is independent of the effective gate-source voltage. Hence $\langle \Delta V_{DS}^2 \rangle/V_{ds}^2 = \langle \Delta N_{ch}^2 \rangle/N_{ch}^2 \propto (V_{GS} - V_t)^{-2}$.

Possible explanations for the deviation from this relation in Fig. 6.12 can be in case i): the trap density in the oxide $n_{tox}$ is not homogeneously distributed with respect to the trap energy level. In case ii) we can have a spatially inhomogeneous trap distribution.

Furthermore if volume inversion occurs the relation $N_{ch} \propto V_{GS} - V_t$ may no longer be valid.

A few remarks should be made

i) Here the g-r processes with the two types of traps are considered to be independent of each other. If both g-r bulges are generated at the same position $x$ by two types of traps with different energy levels this is not generally allowed [14]. It is permissible as long as the free hole concentration is much larger than the trap concentration of the individual traps. In strong inversion this condition is easily fulfilled near the oxide interface.

ii) The g-r noise generated in the channel may have a broadened Lorentzian shape due to the distributed relaxation times. This distribution of relaxation times originates from the fact that the trap energy level with respect to the Fermi-level is position dependent leading to a position dependent relaxation time. The resulting g-r noise spectrum has a broadened lorentzian shape [12]. From our experimental results we can not accurately determine the exact shape of the g-r spectra due to the complexity of the spectra, so we can not check whether the g-r bulges are pure Lorentzians or broadened Lorentzians.

### 6.4 CONCLUSIONS

The $I$-$V$ characteristics and the low-frequency noise are studied of two p-channel Gate-All-Around SOI MOSFETs at low drain-source bias.

The low-frequency noise spectra are decomposed in a $1/f$ noise and two g-r noise components. The $1/f$ noise stems from the channel. No $1/f$ noise from the series resistance is observed. The $1/f$ noise from the channel can be described by the Hooge relation. The Hooge $1/f$ noise parameter $\alpha$ was found to be nearly independent of the gate-source bias. The extracted typical values for $\alpha$ for the two devices are $9 \cdot 10^{-6}$ and $1.7 \cdot 10^{-5}$. 

The g-r noise stems from the channel. The relaxation times of the g-r spectra are independent of the gate-source bias. For all biasing conditions it is found that the variance in the number of carriers is much smaller than the number of carriers in the channel.

The g-r noise can be generated by i) traps located in the oxide or at the oxide interface and ii) by traps in the silicon film at a position close to the intersection of the Fermi-level and the trap level. In both cases i) and ii) the variance is determined by the effective number of traps. If this effective number of traps is constant we expect the relative variance to be inversely proportional to the total number of carriers in the channel squared and hence inversely proportional to the effective gate-source voltage squared. Experimentally we observed a decrease of the relative variance somewhat stronger than inversely proportional to the effective gate-source bias squared. Possible explanations can be an inhomogeneous distribution of the effective trap density in the oxide with respect to the trap energy level in the oxide or an inhomogeneous distribution of traps in the channel with respect to the position in the channel. Furthermore at the onset of volume inversion the number of carriers in the channel is no longer proportional to the effective gate-source voltage leading to an underestimate of the number of carriers in the channel.

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Appendix

**DERIVATION OF THE DRAIN CURRENT VERSUS GATE-SOURCE VOLTAGE IN THE LINEAR REGION**

We assume that the series resistance at the drain and source side are equal and given by \( R_{ss} \). Inclusion of the influence of the series resistance in the expression for the drain current (6.1) yields

\[
I_D = 2\beta_0 \frac{|V_{GS} - I_D R_{ss} - V_t| (V_{DS} - 2I_D R_{ss})}{1 + \theta|V_{GS} - I_D R_{ss} - V_t|} \quad \text{with} \quad \beta_0 = \frac{\mu_0 C_{ox} W}{L} \quad (A6.1)
\]

For a p-MOST we have \( V_{GS} - V_t < I_D R_{ss} \) so that (A6.1) can be replaced by

\[
I_D = 2\beta_0 \frac{(I_D R_{ss} - V_{GS} + V_t) (V_{DS} - 2I_D R_{ss})}{1 + \theta (I_D R_{ss} - V_{GS} + V_t)} \quad (A6.2)
\]

Solving (A6.2) for \( I_D \) yields a square-law relation with solution

\[
I_D = \frac{b - \sqrt{b^2 - 4ac}}{2a} \quad (A6.3)
\]
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with

\[ a = \theta R_{sS} + 2\beta_0 R_{sS}^2 \]
\[ b = 1 - (\theta + 4\beta_0 R_{sS})(V_{GS} - V_t) - 2\beta_0 R_{sS} V_{DS} \]  
(A6.4)
\[ c = 2\beta_0 (V_{GS} - V_t)V_{DS} \]

In the linear region where \( V_{DS} \) is small compared to \( V_{GS} - V_t \) the last term in the expression for \( b \) in (A6.4) can be neglected.

In practice we have the ratio \( a/cb^2 \ll 1 \) so that the square-root in (A6.3) can be expanded. Taking the first two terms of the expansion we have

\[ I_D = -2\beta_0 \frac{(V_{GS} - V_t)V_{DS}}{1 - (\theta + 4\beta_0 R_{sS})(V_{GS} - V_t)} \]  
(A6.5)

Since for p-MOSTs \( V_{GS} - V_t < 0 \) Eq. (A6.5) can be replaced by

\[ I_D = 2\beta_0 \frac{|V_{GS} - V_t|V_{DS}}{1 + (\theta + 4\beta_0 R_{sS})(V_{GS} - V_t)} \]  
(A6.6)

With \( R_s = 2R_{sS} \) we get (6.3).

References

**SUMMARY AND CONCLUSIONS**

In this dissertation the $I$-$V$ characteristics and the low-frequency noise are studied of silicon bipolar transistors both with conventional emitters and with polysilicon-emitters, of GaInP/GaAs heterojunction bipolar transistors, of modulation doped field effect transistors (MODFETs), and of Gate-All-Around Silicon-On-Insulator (GAA SOI) MOSFETs.

In the silicon bipolar transistors with conventional emitter the main $1/f$ noise generator is found to be the $1/f$ noise in the base current $S_{Ib}$. At a constant base-emitter voltage both the base current density, and the $1/f$ noise turned out to be dependent on the emitter geometry. The emitter geometry dependence of the base current density can be explained in terms of a position-dependent minority carrier lifetime in the emitter. Assuming mobility fluctuations to be the source of the $1/f$ noise, a distributed minority carrier lifetime can also explain the observed emitter geometry dependence of the $1/f$ noise. A model was made that divides the emitter in two parts: a central part and an edge part around the emitter with a shorter minority carrier lifetime than the central part. This model is in fair agreement with the experimental results for large emitter areas. Better agreement with the experimental results can be obtained by assuming that the minority carrier lifetime is the shortest in the four corners areas of the emitter. With this refinement the model can also explain the anomalous current dependence of $S_{Ib}$ when emitter current crowding occurs.

The $1/f$ noise of the polysilicon-emitter bipolar transistors stems from noise in the base current $S_{Ib}$ and from noise in the emitter series resistance $S_{r_e}$. Considering the $1/f$ noise in $S_{Ib}$ as a function of the emitter geometry, we found that the $1/f$ noise sources are homogeneously distributed over the emitter area. The $1/f$ noise in $S_{Ib}$ and in $S_{r_e}$ increases with the thickness of the oxide layer present at the monosilicon-polysilicon interface. Grown oxide layers show less noise in both $S_{Ib}$ and $S_{r_e}$ than native oxide layers. The $1/f$ noise in $S_{Ib}$ can be explained in terms of fluctuations of the tunneling probability or transparency, due to barrier height fluctuations of the oxide layer barrier at the polysilicon-monosilicon interface. These transparency fluctuations also cause the $1/f$ noise in the emitter series resistance. Strong support for our model can be found in the fact that both $S_{Ib}$ and $S_{r_e}$ have the same dependence on the oxide layer properties. Our model also predicts that the fluctuations in the base current and the emitter series resistance are fully correlated. The correlation factor between the $1/f$ noise in the base current and the $1/f$ noise in the emitter series resistance was measured. Experimentally, the correlation factor was found to be in the range 0.3-0.5. The fact that the correlation factor is smaller than one can be ascribed to local inhomogeneities in the oxide layer.
Due to the low transparency of the oxide layer, the base current is almost independent of the diffusivity of minority carriers in the emitter. Thus the contribution of diffusivity (mobility) fluctuations to $S_{I_b}$ in the monosilicon region and the polysilicon region is reduced.

The $I$-$V$ characteristics and the $1/f$ noise have been studied of two series of Ga$_{0.5}$In$_{0.5}$P/GaAs heterojunction bipolar power transistors made with basically the same production process. However, the second series has an improved insulation of the metal connecting the emitter to the bonding pad. The $I$-$V$ curve of the base current versus the base-emitter voltage shows a high ideality factor at low currents and a lower ideality factor at high currents. We obtain reasonably accurate results with a description in terms of two base current contributions, one non-ideal with an ideality factor in the range of 1.5-2.8, and an ideal one with ideality factor 1.

The $1/f$ noise in the base current $S_{I_b}$ is found to be the dominant noise generator for all devices. At low currents, where the ideality factor is high, we find $S_{I_b}$ to be proportional to $I_B^2$. At high currents, where the ideality factor decreases, there is a roll-off. Our interpretation of the roll-off is that $S_{I_b}$ is associated with the non-ideal base current. We find that $S_{I_b}$ is proportional to the non-ideal base current squared over the whole studied current range, without a roll-off.

There is a large spread in the $1/f$ noise magnitude for different transistors of the first series. Due to this spread it is difficult to be conclusive about the emitter geometry dependence of the $1/f$ noise. However, from devices with a large number of emitters, having less spread in the noise magnitude, we found the $1/f$ noise magnitude to be independent of the emitter finger length. Based on this experimental fact we suppose that the dominant $1/f$ noise generators are located at the emitter finger tips.

For the devices with the improved insulation (series 2) we found a huge reduction in the $1/f$ noise. Using the relative $1/f$ noise in the non-ideal base current for comparison between devices of comparable emitter geometry, we find a reduction of a factor $10^4$ in the noise for the devices of series 2 compared to those of series 1.

A comparison is made between experimental results obtained from our devices and results presented in literature from AlGaAs/GaAs and from GaInP/GaAs devices. It is found that AlGaAs/GaAs devices have less $1/f$ noise than GaInP/GaAs devices.

We have investigated the $I$-$V$ characteristics and low-frequency noise of modulation doped field effect transistors (MODFETs) made with different gate etching processes and different semiconductor materials. The lowest values for the Hooge $1/f$ noise parameter $\alpha$ in the channel are approximately equal to $10^{-4}$. These values are obtained for both GaAs channels and InGaAs channels and are in agreement with values reported in literature.

We have presented a method to determine whether the dominant $1/f$ noise generator is located in the 2DEG channel or in the series resistance. We have demonstrated that measuring the $1/f$ noise makes it possible to extract the values of
Summary and conclusions

the threshold voltage and of the channel series resistance, provided that the $1/f$ noise stems from the channel and not from the series resistance.

We interpreted the $1/f$ noise in the gate current in terms of transparency fluctuations of electrons tunneling through the interfacial oxide between the metal contact and the semiconductor layer underneath. These transparency fluctuations are caused by the Nyquist noise in the oxide layer. The transparency fluctuations have a $1/f$ spectral density if the loss tangent of the oxide is frequency independent over a wide range of frequencies. The loss tangent values we calculate are high compared to the values reported for bulk oxide materials, but the values are comparable with data of thin films. Furthermore the values for the loss tangent are comparable to the values we calculated for polysilicon-emitter bipolar transistors in chapter 3 of this dissertation. Another interpretation giving reasonable results is the two-step tunneling model where carriers tunnel through the oxide layer via traps. In order to have a $1/f$ spectral density specific requirements have to be fulfilled for the distribution of traps within the oxide.

Due to the fact that the presumably present oxide layers are native and hence may have a different structure from device to device, it is difficult to be conclusive about a possible impact of the gate etching process or semiconductor material choice on the $1/f$ noise in the gate current.

The $I$-$V$ characteristics and the low-frequency noise are studied of two p-channel Gate-All-Around SOI MOSFETs at low drain-source bias.

The low-frequency noise spectra are decomposed in a $1/f$ noise and two g-r noise components. The $1/f$ noise stems from the channel. No $1/f$ noise from the series resistance is observed. The Hooge $1/f$ noise parameter $\alpha$ was found to be nearly independent of the gate-source bias. The extracted typical values of $\alpha$ for the two devices are $9 \times 10^{-6}$ and $1.7 \times 10^{-5}$.

The g-r noise stems from the channel. The observed relaxation times of the g-r spectra are independent of the gate-source bias. For all biasing conditions it is found that the variance in the number of carriers is much smaller than the number of carriers in the channel.

The g-r noise is assumed to be generated by i) traps located in the oxide or at the oxide interface and/or ii) by traps in the silicon film at a position close to the intersection of the Fermi-level and the trap level. In both cases i) and ii) the variance is determined by the effective number of traps. If this effective number of traps is constant we expect the variance to be independent of the gate-source voltage. Experimentally we observed a weak decrease of the variance with increasing gate-source bias. Possible explanations can be an inhomogeneous distribution of the effective trap density in the oxide with respect to the trap energy level in the oxide or an inhomogeneous distribution of traps in the channel with respect to the position in the channel.
SANENVATTING

In dit proefschrift zijn deresultaten gepresenteerd van een onderzoek naar de stroom-spanning (I-V) karakteristieken en de laagfrequentruis van silicium bipolaire transistoren zowel met conventionele emitters als met polysilicium-emitters, van GaInP/GaAs heterojunctie bipolaire transistoren, van MODFETs (modulation doped field effect transistors), en van GAA-SOI-MOSFETs (gate-all-around silicon-on-insulator metal-oxide-semiconductor field-effect transistors).

We hebben gevonden dat de 1/f ruis in de basisstroom $S_{I_b}$ de dominante 1/f ruis generator is in de silicium bipolaire transistoren met conventionele emitters. Zowel de basisstroomdichtheid als de grootte van de 1/f ruis blijken afhankelijk te zijn van de geometrie van de emitter. We hebben de relatie tussen de basisstroomdichtheid, gemeten bij constante basis-emitter-spanning, en de geometrie van de emitter verklaard met behulp van een positie afhankelijke levensduur van de minderheidsladingstragers in de emitter. Als we aannemen dat fluctuaties in de beweeglijkheid van de ladingstragers de bron van 1/f ruis is, dan kunnen we ook de relatie tussen de grootte van de 1/f ruis en de geometrie van de emitter verklaren met een verdeelde levensduur van de minderheidsladingstragers in de emitter.

We hebben een model opgesteld waarin de emitter wordt opgedeeld in twee gebieden: een centraal gebied en een randgebied met een lagere effectieve levensduur van de minderheidsladingstragers dan in het centrale gebied. Dit model is slechts matig in overeenstemming met de experimentele resultaten voor grote emitter oppervlakken. Betere overeenstemming kan worden verkregen door aan te nemen dat de levensduur van de minderheidsladingstragers het kortst is in de vier hoekpunten van de emitter. Met deze verfijning van het model kunnen we ook de stroomafhankelijkheid van de ruis in de basisstroom $S_{I_b}$ verklaren als "emitter current crowding" optreedt.

De 1/f ruis in de polysilicium emitter bipolaire transistoren is afkomstig van de ruis in de basisstroom $S_{I_b}$ en de ruis in de emitter-serieweerstand $S_{r_e}$. Uit de relatie tussen $S_{I_b}$ en de geometrie van de emitter concluderen we dat de ruisbronnen homogeen over het emitter oppervlak zijn verdeeld.

De 1/f ruis dichtheden $S_{I_b}$ en $S_{r_e}$ nemen toe met toenemende dikte van de oxydelaag, die zich bevindt op het grensvlak tussen het polykristallijne en het monokristallijne silicium van de emitter. Thermisch gegroeide oxydelagen leiden tot een lagere 1/f ruis dan de van nature aanwezige oxydelagen. De 1/f ruis kan worden toegeschreven aan fluctuaties in de tunnelkans door het oxyde als gevolg van fluctuaties in de barrièrehoogte van het oxyde. Deze fluctuaties in de tunnelkans leiden tot fluctuaties in de basisstroom en de emitter-serieweerstand. Een sterk argument voor ons model is het feit dat $S_{I_b}$ en $S_{r_e}$ dezelfde afhankelijkheid hebben van de eigenschappen van de oxydelaag. Ons model voorspelt ook dat $S_{I_b}$ en $S_{r_e}$ volledig gecorreleerd zijn. Experimenteel vinden we een correlatiefactor tussen 0.3 en 0.5. Het feit dat we geen volledige correlatie vinden kan worden toegeschreven aan lokale inhomogeniteiten in de oxydelaag.
Ten gevolge van de lage tunnelkans voor ladingsdragers door de oxydelaag is de basisstroom slechts zwak afhankelijk van de beweeglijkheid van de ladingsdragers in de emitter. Hierdoor wordt de bijdrage van fluctuaties in de beweeglijkheid tot $S_{1b}$ sterk gereduceerd.

De $I-V$ karakteristieken en de $1/f$ ruis zijn gemeten aan twee series Ga0.5In0.5P/GaAs heterojunctie bipolaire vermogenstransistoren. Beide series zijn gemaakt met hetzelfde produktieproces. Alleen heeft serie 2 een verbeterde isolatie van de metaallaag die de emitter verbindt met het "bonding pad". De $I-V$ curve van de basisstroom heeft een hoge idealiteitsfactor bij lage stromen en een lagere idealiteitsfactor bij hogere stromen. We kunnen de basisstroom redelijk nauwkeurig beschrijven met twee stroomcomponenten, een niet ideale component met een hoge idealiteitsfactor (tussen de 1.5 en 2.8) en een ideale component met een idealiteitsfactor van 1.

We hebben gevonden dat de $1/f$ ruis in de basisstroom $S_{1b}$ domineert in alle transistoren. Bij lage stromen, waar de idealiteitsfactor hoog is, is $S_{1b}$ evenredig met $I_B^2$. Bij hoge stromen, waar de idealiteitsfactor afneemt, neemt $S_{1b}$ minder toe dan evenredig met $I_B^2$. Onze interpretatie van dit laatste is dat $S_{1b}$ geassocieerd is met de niet ideale basisstroom. We vinden dat $S_{1b}$ evenredig is met het kwadraat van de niet ideale basisstroom over het gehele stromebereik van onze metingen.

Er is een grote spreiding in de intensiteit van de $1/f$ ruis voor de verschillende transistoren van serie 1. Door deze spreiding is het niet mogelijk eenduidige conclusies te trekken wat betreft de relatie tussen de grootte van de $1/f$ ruis in de basisstroom en de geometrie van de emitter. Echter, transistoren met een groot aantal emittervingers hebben minder spreiding in de grootte van de ruis. Hier vinden we dat de grootte van de $1/f$ ruis onafhankelijk is van de lengte van de emittervingers. Op grond van dit experimentele gegeven vermoedden we dat de $1/f$ ruisbronnen zich bevinden in de uiteinden van de emittervingers.

Bij de transistoren van serie 2 hebben we een grote reductie van de $1/f$ ruis gevonden. De relative $1/f$ ruis in de niet ideale basisstroom blijkt een factor $10^4$ lager te zijn in de transistoren van serie 2 vergeleken met die van serie 1.

We hebben een vergelijking gemaakt tussen de experimentele resultaten verkregen van onze transistoren en resultaten beschreven in de vakliteratuur over AlGaAs/GaAs transistoren en GaInP/GaAs transistoren. De AlGaAs/GaAs transistoren blijken minder $1/f$ ruis te hebben dan de GaInP/GaAs transistoren.

We hebben de $I-V$ karakteristieken en de laagfrequentruis bestudeerd van MODFETs die gemaakt zijn met verschillende etstechnieken voor de gate en met verschillende halfgeleidermaterialen. De laagste waarden voor Hooge's $1/f$ ruisparameter $\alpha$ in het kanaal zijn ongeveer gelijk aan $10^{-4}$. Deze waarden zijn verkregen van zowel GaAs kanalen als InGaAs kanalen en komen overeen met waarden die in de vakliteratuur gerapporteerd zijn. We hebben een methode gedemonstreerd om te bepalen of de $1/f$ ruis gegenereerd wordt door het twee-dimensionale electronegas (2DEG) in het kanaal of door de serieweestand. Met behulp van $1/f$ ruismetingen is het mogelijk de waarde van de
threshold spanning en de serieweerstand te bepalen, onder de voorwaarde dat de ruis afkomstig is van het kanaal en niet van de serieweerstand.

De 1/f ruis in de gate-stroom hebben we toegeschreven aan fluctuaties in de tunnelkans voor elektronen, die tunnelen door de oxydelaag tussen de metaallaag en het onderliggende halfgeleidermateriaal. Deze fluctuaties in de tunnelkans worden veroorzaakt door de Nyquistruis van de oxydelaag. De Nyquistruis wordt bepaald door de verliesweerstand en dus door de verlieshoek van het oxyde. De fluctuaties in de tunnelkans hebben een 1/f spectrale dichtheid als de verlieshoek onafhankelijk is van de frequentie in het beschouwde frequentiegebied. De waarden die we berekenden voor de verlieshoek zijn hoog vergeleken met de bulkwaarden van het oxydemateriaal, gerapporteerd in de vakliteratuur, maar vergelijkbaar met waarden gerapporteerd voor dunne lagen. Bovendien komen de waarden voor de verlieshoek overeen met waarden gevonden voor onze polysillicium-emitter transistoren in hoofdstuk 3 van dit proefschrift. Een andere interpretatie, die ook redelijke resultaten geeft, is het zogenaamde "two-step tunneling model", waar ladingstragers door het oxyde tunnelen via traps. Om dan een 1/f spectrum te krijgen moet aan stringente voorwaarden voldaan worden wat betreft de verdeling van traps in het oxyde.

Doordat de vrijwel zeker aanwezige oxydelaag spontaan ontstaan is (d.w.z. niet via een gecontroleerd proces) en dus een sterk wisselende structuur kan hebben voor verschillende transistoren, is het moeilijk conclusies te trekken met betrekking tot de invloed van het etsproces van de gate en de invloed van het halfgeleidermateriaal op de 1/f ruis in de gate-stroom.

We hebben de I-V karakteristieken en de laagfrequente ruisspectra in twee p-kanaals GAA-SOI-MOSFETs bij lage drain-source spanning bestudeerd. De laagfrequente ruisspectra zijn gesplitst in een 1/f ruiscomponent en twee generatie-recombinatie (g-r) ruiscomponenten. De 1/f ruis is afkomstig van het kanaal. We hebben geen 1/f ruisbijdrage van de serieweerstand waargenomen. We hebben gevonden dat de Hooge 1/f ruisparameter \( \alpha \) praktisch onafhankelijk is van de gate-source spanning. De waarden van \( \alpha \) voor de twee transistoren zijn \( 9 \times 10^{-6} \) en \( 1.7 \times 10^{-5} \).

De g-r ruis is afkomstig van het kanaal. De relaxatietijden van de g-r spectra zijn onafhankelijk van de gate-source spanning. Voor alle polarisatiecondities hebben we gevonden dat de variantie in het aantal ladingsdragers veel kleiner is dan het aantal ladingsdragers in het kanaal.

De g-r ruis wordt veroorzaakt door "trapping-detrapping" processen. Er zijn twee mogelijkheden: i) via traps in het oxyde of aan het grensvlak tussen oxyde en halfgeleider, en ii) via traps in de halfgeleider in een gebied rondom het snijpunt van het Fermi-niveau en het trap-niveau. In beide gevallen i) en ii) wordt de variantie bepaald door het effectieve aantal traps. Als dit effectieve aantal traps constant is verwachten we dat de variantie onafhankelijk is van de gate-source spanning. Experimenteel zien we een zwakke afname van de variantie met toenemende gate-source spanning. Mogelijke verklaringen kunnen zijn: een inhomogene verdeling van traps met betrekking tot de energieniveaus in het oxyde of een ruimtelijk inhomogene verdeling van traps in het kanaal.
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STELLINGEN

behorende bij het proefschrift getiteld

Low-frequency noise in modern semiconductor transistors

Hans Markus

1. In polysilicon-emitter bipolaire transistoren met een (min of meer) gesloten oxydelaag tussen het poly- en monokristallijne silicium kan de bijdrage van de 1/f ruis afkomstig van de serieweerstand van de emitter zeer belangrijk zijn.
   - 
   - Hoofdstuk 3 van dit proefschrift

2. Voor het zover mogelijk reduceren van de 1/f ruis in halfgeleiderrkomponenten, waarin de elektrische stroom door een oxydelaag moet tunnelen, is het van belang om aandacht te besteden aan het proces van de vorming van het oxyde. De 1/f ruis wordt geminimaliseerd door een zo dun mogelijke oxydelaag via thermische oxydatie te maken.
   - Hoofdstuk 3 en 5 van dit proefschrift

3. In de vakliteratuur wordt vaak gesteld dat, als de stroomspannings-karakteristieken worden bepaald door de intrinsieke bipolaire transistor, dit ook geldt voor de 1/f ruis. Deze bewering is onjuist.

4. Circuitontwerpers gebruiken vaak een ruisbeschrijving van een bipolaire transistor met een equivalente ingangsruisbron. In de praktijk wordt daartoe de ruis aan de uitgang van de transistor in een gemeenschappelijke-emitterschakeling gemeten en teruggerekend naar de ingang. Deze beschrijving is niet gegarandeerd volledig en heeft daarom dan ook geen voorspellende waarde voor het ruisgedrag van de transistor in andere dan de gemeenschappelijke-emitterschakeling. In de vakliteratuur wordt dit niet altijd onderkend.

5. Algemeen veronderstelt men in de telecommunicatiewereld dat de thermische ruis in frequentie wordt begrensd door de "quantum cut-off," omdat deze begrenzing onafhankelijk is van materiaal eigenschappen. In werkelijkheid wordt de thermische ruis echter begrensd door de reciroke botsingstijd van elektronen in het materiaal.
6. In veel tekstboeken over de bipolaire transistor wordt de afvoersnelheid van minderheidsladingdragers in de basis aan de collectorzijde oneindig verondersteld. Deze benadering leidt bij moderne transistoren tot een grote discrepantie tussen model en werkelijkheid.

7. Aan de opmaak van de tekst voor de proceedings van wetenschappelijke conferenties worden vergaande eisen gesteld door de organisatie van de conferentie. Hetzelfde zou ook moeten gelden voor de verzorging van de presentaties.

8. Dat de maatschappij zicht eist op wat de wetenschap doet is terecht. Dat de politiek zich nu echter in detail met de wetenschap wil gaan bemoeien is een slechte zaak, daar de wetenschap dan gemakkelijk ten prooi kan vallen aan het vrij algemeen gangbare korte termijndenken in de politiek.

9. Ministers en staatssecretarissen gebruiken graag het regeerakkoord als argument om zich te onttrekken aan vaak noodzakelijke bijstellingen van beleid. Deze weinig flexibele interpretatie van het regeerakkoord wringt het regeringsbeleid in een strak keurslijf voor een wel erg lange periode.

10. De Europese politiek zou gebaat zijn bij het afschaffen van het vetorecht van de individuele lidstaten.

11. In Nederland wordt het belang van goede restauratieve voorzieningen in bedrijven en instellingen vaak onderschat.

12. Werkervaring is een dualistisch begrip: bij recrutering van jonge werknemers is het meestal een vereiste, voor het behoud van een baan voor oudere werknemers blijkt het vaak van ondergeschikt belang.

13. Oversteken bij rood licht is relatief veilig want het biedt de zekerheid dat aanstormend verkeer niet stopt.