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A Background Calibration Technique Based on Limit Cycles for Reconfigurable Sigma Delta Modulators

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\textbf{Abstract}—Reconfigurable ADCs bring a lot of functionality, high added value while sharing the development time and cost for each targeted application. Sigma Delta Modulators (SDMs) are very popular for their suitability for a wide range of applications. While individual SDMs can be tailored towards specific applications, a reconfigurable SDM addresses several of them at the same time. Due to their complexity (introduced by the programmability) and the limitations imposed by PVT variations, calibration is essential. To this effect, we introduce a new background calibration technique based on the limit cycle model of SDMs. We show how a simple counting and categorization of output bit-patterns can be used for measurement and correction/adjustment of the loop filter in the presence of multiple inaccuracies or changing operation conditions. The calibration scheme is demonstrated with measurement results from a test chip. The chip implements a 3rd order reconfigurable SDM for ultra-low bio-sensor current measurements. The reconfigurability, coupled with the calibration scheme, allows a widely programmable bandwidth and dynamic range, making it useful for a variety of applications.

I. INTRODUCTION

Continuous time sigma delta modulators (CT-SDMs) have successfully met the industry demands for high resolution using relatively simple circuits. However, an upper bound on that resolution is imposed by various non-idealities that CT-SDMs suffer from. Some non-idealities which can be addressed on the system level are loop filter inaccuracy i.e. inaccurate placement of poles and zeroes, excess loop delay (ELD) resulting from a slow comparator or a switched-capacitor DAC and non-linear delay resulting from hysteresis in a comparator. Finite op-amp parameters, comparator metastability, charge injection, etc. are circuit level non-idealities. Most circuit level non-idealities have some system level effect. Many calibration techniques have been proposed which address these non-idealities on an individual basis \cite{1} \cite{2} \cite{3} \cite{4}.

Our calibration technique is targeted primarily for reconfigurable SDMs. Sigma Delta Modulators (SDMs) are typically favored as reconfigurable ADCs. There are multiple reasons for this choice. SDMs are capable of achieving very low power consumption levels while providing an inherent trade-off between power, speed and accuracy \cite{5}. While changing the sampling frequency is the most common way of reconfiguring the SDM \cite{6}–\cite{9}; flexible order loop-filters \cite{10}, \cite{11}, multi-bit quantizers and multi-stage \cite{12}–\cite{14} structures are also being used to achieve the most optimum power-accuracy trade-off and to extend/adapt the operation region of the SDM. Continuous-time Sigma Delta Modulators (CT-SDMs) also exhibit inherent anti-aliasing filtering, noise shaping of sampling non-linearity \cite{5}. Design centering for reconfigurable SDMs becomes very complex and unmanageable as the reconfigurability scales up. As a result, calibration mechanisms are necessary to ensure that reconfigurable SDMs operate optimally in every mode.

In this paper, we propose a new calibration technique which does not require any test signals, out-of-band interferers or replica circuits. The technique is a background calibration method which does not interfere with the normal operation of the SDM and requires no extra hardware in the loop, except for the redundancy required to design a tunable SDM. The output bit-stream is observed during normal operation to estimate a distribution of the operating limit cycles \cite{15}. Each non-ideality affects the distributions in a specific way. We use this knowledge to identify the non-ideality and compensate/calibrate it in a step-by-step method. This method can be used to calibrate the loop-filter coefficients, the excess loop delay and the quantizer hysteresis.

In section II we explore the most popular applications where reconfigurable SDMs are employed. In section III we elaborate on the need for calibration in reconfigurable SDMs, followed by existing techniques for calibration. In section IV we introduce the limit cycle model of SDMs and (in section V) use it to derive a very simple background calibration technique for compensation of loop-filter co-efficient variations, excess loop delay in response to sampling clock variation and quantizer hysteresis. In section VI the effect of input signal on limit cycle distributions is discussed. In section VII we demonstrate the calibration technique using a MATLAB testbench. In section VIII we demonstrate the calibration technique with a case study. A reconfigurable current mode SDM was fabricated and was used a test vehicle to demonstrate the calibration technique. The conclusions are discussed in section IX.

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II. APPLICATIONS OF RECONFIGURABLE SIGMA DELTA MODULATORS

Reconfigurable SDMs find multiple applications, among which, the most common ones are: multi-mode radios where different standards impose different specifications on the SDM and multi-signal bio-medical interfaces where the signal bandwidths and dynamic ranges vary widely. More recently advances in amperometry and related bio-sensors for the study of various natural phenomena also require reconfigurable current mode SDMs which can convert signals with very large dynamic ranges.

A. Multi-Mode Radios

An important commercial aspect of mobile communication systems is the efficient usage of the available spectrum by cognitive radio techniques [16]. The key for this view of cognitive radio is a reconfigurable RF frontend providing the required flexibility. This also becomes a key issue in 4G telecom systems where receivers not only have to handle multiple standards and specifications, but also have to adapt to the environment such as the presence of received blockers or status of battery power levels. One of the most challenging parts of such a multi-standard radio system is the analog to digital converter. Although an RF to digital converter would make the above mentioned Software Defined Radio (SDR) paradigm possible, the specifications required imply that this would lead to a very unfeasible and power-hungry solution. Towards this goal, many reconfigurable ADCs have been proposed in the past, of which a reconfigurable SDM is the most practical to implement due to its inherent power-accuracy and power-bandwidth trade-off. SDMs offer multiple options to realize this trade-off in the form of filter order, quantizer bits and oversampling ratio. The structure of the SDM and its coefficients can be so chosen as to implement a narrowband STF which is useful for signal selectivity and blocker suppression. If the coefficients are made programmable, the signal band can also be varied according to the requirements. A widely programmable lowpass/bandpass SDM has been reported in [17]. Using a combination of programmable LC and RC filters, the centre frequency can be varied over a large set of values. A ‘leap-frog’ topology has also be reported [6] which aims to split the notch for more flexible placement. Programmability in the quantizer bits is introduced to compensate for the drop in OSR at higher bandwidth requirements such as WLAN. [8] reports a programmable loop filter which optimally reconfigures the NTF in response to a change in the number of quantizer bits. MASH SDMs, both continuous time and discrete time, have been reported for use in multi-mode radios [12], [13]. MASH topologies can achieve higher orders while enjoying the stability of lower order SDMs. Individual stages can also be power gated to save power in certain modes. [18] provides an excellent overview of various SDM topologies used in multi-mode radios.

B. Bio-Potential Signal Sensing

Bio-potential signals are characterized by very low amplitudes, large dynamic range and widely varying bandwidths. There is an increasing demand for universal analog frontends which can sense a large subset of various bio-potential signals. Having a power efficient analog to digital converter forms the basis for the implementation of a power efficient frontend. A number of Nyquist ADCs with state-of-the-art figures of merit (FOM) have been proposed in the past. However, these were limited to resolutions below 12-bits. [9] proposes a reconfigurable DT-SDM with a state-of-the-art FOM, achieving up to 16-bits of resolution. The SDM can be reconfigured for 3 modes trading off resolution with bandwidth at a nearly constant FOM. The power scaling was achieved by power gating the OTAs and switching to a different sampling capacitance between the different modes.

III. CALIBRATION IN RECONFIGURABLE SDMS

Verifying this programmability of highly reconfigurable SDMs during design time by simulating Process, Voltage and Temperature (PVT) corners and Monte-Carlo simulations, becomes very impractical and time consuming. With fabrication technology moving to lower process nodes, the variation between design and implementation is bound to increase. Furthermore, the sample-to-sample variations also increase. As a result, calibration is necessary to ensure that reconfigurable systems perform as expected at each configurable state. As we saw in the previous section, SDMs are reconfigured by changing the sampling frequency, the filter order, number of bits in the quantizer and the number of stages (in case of MASH topologies). For CT-SDMs, the loop-filter parameters have to be changed for each configurable state. Varying the sampling frequency also changes the impact of excess loop delay (ELD) on the performance. Thus the ELD correction mechanism also has to adapt to the sampling frequency. All the most SDM topologies, the signal swing at the output of the integrators is minimized in order to save power. Comparator hysteresis and offset become dominant for very low signal swings, and must also be calibrated.

Several calibration techniques have been proposed in the past to correct various non-idealities such as RC time constant error [1], inaccuracy in analog voltage references [2], excess loop delay [3], feedback DAC non-linearity [19], etc. Techniques have been suggested to estimate these non-idealities before calibration [20]. Common techniques to calibrate the loop filter involve calibrating the NTF using a well defined test signal or a signal with a known amplitude distribution [21]. This is a form of offline/foreground calibration. However, disconnecting the input to apply the test signal is inconvenient. Therefore online/background calibration techniques were derived where a broadband signal is applied either at the input or at the quantizer [22]. Correlation techniques are then used to compensate the inaccuracy. Another technique involves estimating the inaccuracy from a replica circuit (e.g. an integrator) and then applying a correction to the actual circuit [1]. While all the above mentioned techniques are effective against isolated non-idealities, they fail against multiple non-idealities occurring together, as in most practical situations. A certain calibration technique may not work as effectively in presence of another non-ideality as their effects may be
difficult to distinguish. Furthermore, the need to use special test signals is an added inconvenience, especially when dedicated hardware is required to generate them.

We propose a new background calibration technique based on the limit cycle model of SDMs. Our technique does not require any test signals, out-of-band interferers or replica circuits. It requires no extra hardware in the loop, except for the redundancy required to design a tunable SDM. For reconfigurable SDMs, the redundancy is already built-in. The calibration technique primarily targets system level non-idealities such as loop-filter zero position inaccuracy, excess loop delay and comparator hysteresis compensation. Other non-idealities such as the ones mentioned in this section also adversely affect SDMs. Preliminary simulation results of the proposed calibration technique towards correcting these other non-idealities have produced promising results. However, they require further verification and will be the subject of another paper.

IV. LIMIT CYCLE MODEL OF SDMS

The limit cycle model takes a non-linear approach towards the analysis and synthesis of sigma delta modulators (SDMs) [23]. Traditionally, the term “limit-cycles” is associated with the undesired tonal behavior observed in SDMs. We distinguish between this generally recognized term from the mechanism that essentially governs the operation of SDMs. In the following analysis we describe limit-cycles as an integral part of SDM operation. Limit cycles are regular patterns that are observed in the output bit-stream. “..10101010..” is one such pattern which is the $\frac{f_s}{4}$ limit cycle. “..11001100..” is the $\frac{f_s}{8}$ limit cycle, etc. The SDM is treated as a non-linear closed loop (NLCL) system in which the linear and non-linear parts are separated as shown in Fig 1. The linear part $L(j\omega)$, which we term as the loop filter incorporates contributions from the forward path as well as contributions from the feedback path. The non-linear part, which is the quantizer, is replaced by its describing function $N(A, \phi_s)$ [24]. Since it is a feedback system, it is capable of oscillating (limit cycling) under the right conditions, namely if $1 + L(j\omega)N(A, \phi_s) = 0$. The system will oscillate if the loop gain is unity and the phase shift is either $0$ or $2\pi n, n \in \mathbb{Z}$ radian. This is most conveniently visualized in a phase-magnitude plot as shown in figure 2(a).

The describing function of a binary 2-level quantizer is given by $N(A) = \frac{4A}{1+4A^2}$, where ‘A’ is the amplitude of the signal before the quantizer. By virtue of its non-linearity, it also ensures that the gain in the loop is unity. The loop filter (solid curve in figure 2(a)) contributes a frequency dependent magnitude and phase shift as defined by its transfer function. The quantizer clock adds a signal-dependent phase shift. Although the exact phase shift cannot be predicted, the range of phase shifts at the limit cycle frequencies can be predicted and is shown by the dashed lines in figure 2(a) [24]. The frequencies at which the limit cycling conditions are met are called limit cycle modes (LCM). Figure 2(a) shows that the system can oscillate at limit cycle frequencies $LCM1 = \frac{f_s}{2}$ and $LCM2 = \frac{f_s}{4}$, although not at the same time. The line for $LCM4 = \frac{f_s}{8}$ does not

Fig. 1. Model of a SDM separated into linear and non-linear blocks

Fig. 2. Example of a Limit Cycle Plot. (a) Phase-magnitude plot. (b) Transient loop filter output

Fig. 3. Loop filter output showing the tonal pattern in limit cycle switching
cross the 180 degree line. Thus the system cannot oscillate at LCM4 or, in other words, LCM4 is not supported. Any signal applied to the input gradually renders the operating limit cycle unstable as the clock added phase shift steadily increases (or decreases) to a point where oscillations cannot be sustained. At this point, the system switches to another supported limit cycle. The amount of phase accumulation required to render a limit cycle unstable is dependent on the phase boundary (the amount by which the dashed lines cross the 180 degree line). Fig 2(b) demonstrates this process by plotting the output of the loop filter for a small DC input signal. From this figure, two limit cycle modes can clearly be recognized and it is shown that the SDM switches between those two modes. The limit cycles themselves do not hold any information. The applied signal is encoded by the switching between the limit cycles that are supported by the SDM.

Tonal behavior in SDMs is attributed to a repeating pattern in the switching between the supported limit cycles. It is observed primarily in first order SDMs or when the stabilizing zeroes of the loop filter of higher order SDMs are positioned at very low frequencies. Figure 3 shows the output of the loop filter of a second order SDM with a stabilizing zero at a very low frequency. A repeating pattern in the limit cycle switching can be observed. 3 bits belong to LCM1 and 2 bits belong to LCM2. If each bit is labeled as belonging to a particular limit cycle, the following pattern emerges: ...111221122111.... This leads to correlated quantization noise and spurs in the output spectrum. Higher order modulators with optimally positioned loop filter zeros are able to de-correlate quantization noise by randomizing the limit cycle switching pattern.

V. NON-IDEALITIES AND LIMIT CYCLE DISTRIBUTIONS

In section V we saw that limit cycle switching can be viewed as an integral part of SDM operation. Depending on the loop configuration, the SDM operates at some limit cycles more than others. This means, that in a given set of output bits, more bits belong to a particular supported limit cycle than the rest of the bits, which belong to another supported limit cycle. Such a limit cycle can be termed as a dominant limit cycle. A dominant limit cycle has a greater distribution in the number of observed output bits. This is dependent on the phase boundary of each limit cycle. The phase boundary is the amount of excess phase shift by which the dashed lines cross the 180 degree line (fig 2(a)). The performance and stability of the SDM is also governed by limit cycle distributions. A configuration which results in a dominant LCM1 operation is the most stable configuration but it also has the lowest performing mode in terms of signal to quantization noise ratio (SQNR). A first order SDM or a second order SDM with a low frequency zero is an example of this configuration. A balanced configuration where LCM1 and LCM2 are equally occurring exhibits higher SQNR but slightly lower maximum stable amplitude (MSA) than the dominant LCM1 case. A third configuration allows lower limit cycles (LCM3, LCM4, etc). This results in a high overall SQNR but lower limit cycles have a large signal swing which can result in clipping. This configuration is less preferred as it is more prone to instability triggered by layout errors or process mismatch errors. Figure 4 shows the different modes and their impact on the SNR.

The output bit-stream contains information about the supported limit cycles and their switching activity. A limit cycle of a given frequency appears as a particular pattern in the bit-stream. E.g. LCM1 appears as a .1010.. pattern, LCM2 appears as a .11001100.. pattern, LCM3 appears as a .111000111001.. pattern and so forth. Any bit-stream can be decomposed into its constituent limit cycle patterns as shown in Fig 5. It must be noted that while decomposing the bit-stream we start with the lowest frequency limit cycle. The lowest frequency limit cycle can be found out by measuring the length of the longest set of consecutive 0s or 1s in the bit-stream. The limit cycle distribution can then be constructed by counting the total number of bits belonging to a particular limit cycle. Abnormalities in limit cycle distributions can point towards specific non-idealities in the modulator loop. Most non-idealities affect a certain portion of the phase-magnitude plot. As a result, the limit cycle distributions also change in a unique way. Additionally, some loop parameters affect limit cycle distributions only in the presence of a certain non-ideality. This information can be used to identify the non-ideality and take steps towards compensating it.
A. Inaccuracies in Loop Filter Zero Position

The poles of the loop filter define the order of the modulator and the zeros control the performance and stability. A Loop-filter zero placed at a high frequency can result in instability, while at low frequency it degrades the performance of the modulator to a lower order. An optimally positioned zero results in high SNR and is of importance for calibration. Figure 6(a) shows the effect of changing the zero frequency on a phase-magnitude plot and the limit cycle distributions. The loop filter zero predominantly affects the part of the loop filter curve which is relatively horizontal. Limit cycles belonging to the vertical portion (parallel to the 180 degree line) are not affected as much since the phase boundaries of those limit cycles do not change significantly. Figure 6(b) plots the limit cycle distributions as computed at various zero frequencies. A $2^{nd}$ order SDM with a sampling frequency of 500 kHz was used as the simulation vehicle in MATLAB. A uniformly distributed random signal was applied as the input to the SDM and the limit cycle distributions were computed from the output bit-stream using the method described in figure 5. A low frequency zero is characterized by a dominant $\frac{1}{N}$ limit cycle or limit cycle mode 1 (LCM1). As the zero moves to higher frequencies, LCM1 starts becoming less dominant, LCM2 starts becoming more frequent and lower limit cycles (LCM3, LCM4, etc) start making an appearance (figure 6(b)). Eventually, with the introduction of many low frequency LCMs the system becomes unstable. The distribution of LCM1 relative to other LCMs provides an estimate regarding the position of the zeros. The trend shows that it is not possible to further reduce or completely eliminate the operation of LCM1 simply by positioning the zeroes at higher frequencies.

B. Excess Loop Delay

The effect of excess loop delay (ELD) can be understood intuitively using the limit cycle model. Slow comparators and multi-phase switched capacitor feedback DACs are known to cause excess loop delay. Larger delays can result in instability. ELD can be interpreted as an infinite number of parasitic poles at higher frequencies. Figure 7(a) shows the effect of ELD on a phase-magnitude plot. The bend in the loop filter curve at higher frequencies is caused by the parasitic poles introduced by ELD. The nature of ELD is such that it is dominant at higher frequencies. As a result, it affects higher frequency limit cycle modes such as LCM1, LCM2, etc (in decreasing order of effect). This is visible from the trend in the limit cycle distributions for individual limit cycles as illustrated in figure 7(b). As the amount of delay is increased, the occurrence of LCM1 reduces and eventually disappears. This is different compared to the case of high frequency zeroes because the SDM is still stable, albeit, working at a lower SNR. This signifies that it is possible to completely eliminate higher frequency limit cycle modes (LCM1 in this case) while keeping the loop operational and stable.

C. Hysteresis

Hysteresis is a non-linear amplitude dependent delay resulting from comparator non-idealities. Its describing function can be written as $N_{BOM}(A, \phi) = \frac{4D}{\pi} e^{-j\sin^{-1}(\frac{\phi}{A})}, A > h$ where $A$ is the amplitude of the signal before the quantizer, $\phi$ is the phase shift, $D$ is the amplitude of the signal after the quantizer, $h$ is the normalized hysteresis relative to $D$ [24]. Figure 8(a) shows the effect of hysteresis on a phase-magnitude plot. It shows a bend in the line corresponding to the describing function of the quantizer $\frac{1}{N_{CM}}$. The bend signifies the increasing amplitude dependent phase shift. The bend is sharper at lower amplitudes and hence affects higher frequency limit cycles such as LCM1. Hysteresis essentially has a similar effect on limit cycle distributions as ELD (figure 8(b)) i.e. it makes higher frequency limit cycles such as LCM1 progressively less dominant. In order to compensate this non-ideality, it is important to distinguish hysteresis from ELD. Since hysteresis is an amplitude dependent delay, it is affected by loop gain. Varying the loop gain effectively shifts the whole loop filter curve up (or down) within the phase-magnitude plot. This modifies the phase boundaries by modifying the crossing points of limit cycles with the quantizer curve. This is a useful
loop parameter to undo the effects of hysteresis. Furthermore, loop gain does not affect the limit cycle distributions in the absence of hysteresis, regardless of other non-idealities present.

While calibration of loop filter zero positions, hysteresis and delay are important for reconfigurable SDMs, there are other non-idealities which also adversely affect the performance of the SDM. Notable among these are circuit noise and non-linearity. Larger non-linearities require special analysis by treating it as a separate non-linearity in the limit cycle model. A preliminary treatment of multiple non-linearities in a non-linear closed loop is given in [24]. Its treatment in the context of limit cycle based calibration, however, is out of the scope of this paper. Circuit noise does not affect the recording of limit cycle distributions. However, it limits the peak achievable performance, as limit cycle calibration primarily targets quantization noise. This is demonstrated in the following section.

VI. EFFECT OF INPUT SIGNAL ON LC DISTRIBUTIONS

Limit cycle switching is governed by phase accumulation which in-turn is dependent on the specific input applied to the SDM [23]. As such, the limit cycle distributions are weakly dependent on the applied signal amplitude unless it overloads the SDM. For DC inputs, the phase accumulation (or subtraction) is monotonic. Phase accumulation or subtraction is based on the polarity of the DC signal applied. The rate at which the phase accumulates is dependent on the magnitude of the DC signal applied. The duration of operation of each limit cycle is dependent on system configuration and is a weak function of the applied DC signal amplitude. Figure 9(a) plots the limit cycle distribution as a function of the applied DC signal amplitude for a given loop-filter configuration (2nd order, $F_s = 500$ kHz). In case of a sinusoidal input the phase accumulation too is sinusoidal instead of being monotonous. Equal phase accumulation and subtraction occurs in the loop over 1 period of the sine wave. For sufficiently large input amplitudes, the loop can jump between supported limit cycles.
several times within 1 period. The frequency of the applied sinusoidal input can also affect the switching pattern since it influences the instantaneous amplitude. Figure 9(b) plots the limit cycle distribution as a function of the input sine wave amplitude. The weak dependence on amplitude is demonstrated here as well. Figure 9(c) plots the limit cycle distribution for a uniformly distributed random signal.

VII. TEST-BENCH AND SIMULATION RESULTS

Figure 10 shows a 2nd order feedforward SDM used as an example to demonstrate the calibration algorithm. The low frequency zero is controlled using the feedforward coefficient ‘c’. The high frequency zero resulting from the extra loop can be controlled using the coefficient ‘k’. The hysteresis can be controlled using the ‘Bias’ control. The test-bench outputs a bit-stream which is used to calculate the limit cycle distributions. The algorithm is implemented separately as a MATLAB script which uses the limit cycle distributions and generates the necessary control signals to the test-bench.

In the following discussion we will consider a test case; a situation where a 1-bit 2nd order SDM with real poles and zeroes (F_s = 500 kHz, OSR = 50) is corrupted by hysteresis, ELD and an inaccurately placed low frequency loop-filter zero, at the same time. The input to the SDM is a uniformly distributed (within the linear dynamic range) random signal, as would be expected in a real-world application (the method works well for sine-wave and DC inputs). The eventual goal of the algorithm is to compensate delay, hysteresis and to calibrate the position of the loop-filter zero to obtain high SNR, allowing limit cycles up to LCM4 while maintaining stability. The algorithm can be tailored towards different goals.

Since LCM1 is the highest frequency limit cycle, it is also the most sensitive towards hysteresis and delay. In our approach, we vary a certain loop parameter and observe its effect on the distribution of LCM1. In each calibration step, a loop parameter is varied in a way so as to achieve the pre-determined calibration goal. Figure 11(a) shows that at start-up LCM2 is dominant, followed by LCM1 and LCM3. This is indicative of a large amount of delay and/or hysteresis. The algorithm starts by correcting hysteresis. The loop gain is increased till the LCM1 distribution nearly saturates and is no longer affected by variations in the loop gain. This is verified since the distributions begin to equalize and LCM3 is eliminated. The high frequency delay compensating zero is calibrated similarly until the LCM1 distribution begins to saturate. At this point the limit cycle distributions reflect the inaccuracy solely due to the frequency position of the loop-filter zero (lower frequency). This zero is then calibrated till the required distribution is obtained (figure 11(b)). Figure 12 demonstrates the calibration process applied to a 3rd order SDM with real poles and zeros (F_s = 500 kHz, OSR = 50). The non-idealities are introduced in different proportions compared to the 2nd order case in order to demonstrate the robustness of the calibration scheme.

Circuit noise is an important non-ideality that limits the maximum achievable performance using limit cycle based calibration. The power of circuit noise is much lower than

Fig. 9. Limit cycle distributions with various applied inputs (a) DC (b) Sinusoidal (c) Uniformly distributed random signal.
the power of limit cycles. As a result, the presence of noise at
the input of the SDM does not adversely affect the recording
of limit cycle distributions. Within the bandwidth of interest,
however, circuit noise may dominate. This will limit the
maximum achievable performance. We demonstrate this with
a 6th order SDM (Fs = 500 kHz, OSR = 50, -20 dBFS
sinewave input) with a uniformly distributed noise coupled
to its input. As in the previous test-benches, non-idealities
in the zero position, delay and hysteresis are also introduced.
Figure 13(a) shows the almost overlapping LCM1 distributions
for different noise variances. Figure 13(b) shows the SNR
trend when the noise variance is increased. When circuit noise
begins to dominate, the SNR gain from limit cycle calibration
becomes negligible.

In another test case we consider a 4th order SDM (Fs =
500 kHz, OSR = 50, -20 dBFS sinewave input). The order of
the SDM is successively scaled to lower orders by switching
off the integrators (as it might be required for power-saving
reasons). As the order scales, the coefficients also have to be
scaled. Without relying on pre-determined coefficient values
(which may not be ideal in the presence of various errors),
the filter coefficients can be effectively scaled using limit cycle
distributions as described the previous section. Figure 14(a)
plots the limit cycle distributions. A step in the distributions
is observed whenever the order (L) is scaled. The calibration
algorithm scales the coefficients to obtain equal distributions for
LCM1 and LCM2; a calibration goal set for this testbench.
Figure 14(b) plots and compares the signal to noise ratios
obtained with and without limit cycle calibration.

VIII. CASE STUDY: RECONFIGURABLE SDM FOR
AMPEROMETRIC BIO-SENSOR SIGNAL ACQUISITION

Amperometry is typically performed with a charge amplifier
front-end which integrates the sensor generated current into
a voltage. This voltage is then processed and converted by
an analog to digital converter. However, the current trend is
towards miniaturizing and array integration of nano-biosensors.
In such a scenario, it is essential to avoid noise due to the
stray capacitance of long interconnect lines. This requires A/D
correction to be performed as close to the sensor substrate
as possible. Furthermore, multiplexing a digital output is far
easier and more reliable than multiplexing analog voltages. A
pixel level A/D converter achieves the above goal. A pixel level

![Fig. 10. An example 2nd order feed-forward sigma delta modulator](image-url)

![Fig. 11. Simulation results demonstrating step-wise compensation of various
non-idealities for a 2nd order SDM. (a) Limit cycle distributions at each
 calibration step. (b) Signal to Noise Ratio (SNR) at each calibration step. (c)
Output Spectrum before/after calibration](image-url)
ADC needs to be compact and the circuit overhead resulting from frontend circuitry needs to be minimized.

Given the low bandwidth and high resolution requirement, a current-mode incremental sigma delta ADC presents itself as the most optimum choice for A/D conversion in this example application. [25], [26] describe Sigma Delta ADC based current acquisition platforms with excellent low frequency noise performance. However, these systems have a low dynamic range and can handle only a limited range of currents. We describe an incremental continuous time sigma delta ADC intended to be used as a direct interface current acquisition platform for individual sensors. In contrast to existing systems, our system is highly reconfigurable with four current ranges: 25nA, 250nA, 25µA and 250µA. Along with scalable dynamic range, the sampling clock is also scalable for achieving different conversion times. The ADC incorporates programmability in its loop filter which can calibrate itself to an optimum operating point in response to the scaled clock.

Fig. 13. Simulation results demonstrating step-wise compensation of various non-idealities for a 6th order SDM in the presence of circuit noise. (a) LCM1 distribution at each calibration step. (b) Signal to Noise Ratio (SNR) at each calibration step

Fig. 12. Simulation results demonstrating step-wise compensation of various non-idealities for a 3rd order SDM. (a) Limit cycle distributions at each calibration step. (b) Signal to Noise Ratio (SNR) at each calibration step. (c) Output Spectrum before/after calibration
A. System Design and Circuits

The system acquires an input current and converts it into a bit-stream, whose weighted average corresponds to the input current. It consists of an on-chip continuous time current input sigma delta ADC and an off-chip $Sinc^3$ filter. The sigma delta modulator is implemented using a $3^{rd}$ order low pass loop filter by cascading 3 filter stages as shown in Figure 15. The charge amplifier is utilized effectively by making it a part of the sigma delta modulator loop as the first stage of the loop filter. It adds a single pole at the origin. The second and third stages are implemented using active RC filters, each contributing a pole at the origin and an adjustable zero. A fourth filter stage can be introduced into the signal path to add an extra zero, which is used for excess loop delay compensation. This cascade of filters topology is very useful for reconfigurability as it allows independent control of various loop parameters unlike feed-forward or feedback topologies where co-efficients and integrator gains are interdependent. We chose to implement the loop filter gain control in the charge amplifier by controlling the integrating capacitance. The stabilizing zeros are determined by the RC product in each filter stage and are controlled by varying the feedback capacitance in each stage. The extra zero introduced by the fourth filter stage can also be independently controlled by varying the feedback capacitance in this stage. In our implementation we use banks of capacitors in combination with CMOS transmission gates to program the RC products in individual filter stages. While this approach is area expensive (especially at low frequencies when RC products become large), it allows freedom and flexibility for tuning individual loop parameters. Parasitics introduced by the tuning circuitry, that result in inaccurate coefficients are automatically calibrated by the limit cycle calibration algorithm.

The charge amplifier in the first stage is implemented using a two-stage fully differential Miller op-amp (Figure 16(a)). The charge amplifier is one of the most critical components; its noise performance dominates the noise performance of the system. Thermal noise is minimized by appropriately choosing the bias currents. Flicker noise, being the dominant contributor, is reduced to an acceptable level by increasing the size of the input transistors. Figure 16(b) shows the continuous time noise model for the charge amplifier. The voltage and current noise components (Figure 17(a)) are obtained by performing an AC noise simulation on the parasitics-extracted layout of the charge amplifier to account for noise due parasitic capacitances of the interconnects in addition to that of the amplifier. The combined input referred current noise is shown in Figure 17(b). The simulated RMS noise in a bandwidth of 100 Hz is found to be approximately 300fA. The discrete time noise generated due to the noise sampling operation in the reset switch (which happens at the start of each conversion) is neglected since it only generates a small offset which the loop corrects over time when an input current is applied.

The loop filter is followed by a single-bit quantizer. This preserves the linearity of the loop while conserving power and area which would be required for dynamic element matching or data weighted averaging schemes. The quantizer is implemented using a dynamic comparator described in [27].

The charge transferred by the DAC is made programmable by means of a capacitor bank. This allows a programmable dynamic range over a wide current interval. The DAC is fully differential and implemented using a switched-capacitator network (Figure 18(a)). The parasitics associated with the capacitor bank are minimized by careful layout and matching techniques. DAC switches are implemented using transmission gates which reduce charge injection and clock feedthrough errors. The fully differential topology further minimizes offsets resulting from charge injection and clock feedthrough. The switches are clocked with low duty cycle phase clocks. In contrast to traditional clocking techniques, using a low duty cycle phase clock significantly reduces delay resulting from the charge-discharge cycle of a switched capacitor DAC, by reducing the delay between the two phases. The low duty cycle phase clocks are generated from a digital ring counter. The feedback DAC also contributes to the total noise at the input terminals of the charge amplifier. Figure 18(b) shows the
results of a periodic noise (P-Noise) simulation performed on the parasitics-extracted layout of the DAC. The RMS noise current integrated over a 100 Hz bandwidth is found to be approximately 16.4fA.

B. Experimental Results

The prototype chip was implemented in a 0.18μm CMOS process and occupies an active area of 0.49 mm². The chip micrograph is shown in Figure 20. In this measurement setup, the bit-stream generated by the SDM is imported directly into MATLAB for processing. A LabVIEW module acts as an intermediate interface which forwards the bit-stream to MATLAB and also generates the necessary control signals for reconfiguring the SDM. The calibration algorithm targets a limit cycle distribution based on application requirements. It may, for example, be desirable to eliminate a high frequency limit cycle such as LCM1. The maximum operating frequency of the loop will reduce to LCM2 frequency. This will relax the bandwidth requirement of the op-amps, allowing bias currents to be scaled, thereby saving power. Thus the calibration algorithm will focus on eliminating LCM1.

To demonstrate the programmability in the dynamic range, Figure 19 plots the transfer curves for 4 dynamic ranges namely 25nA, 250nA, 25μA and 250μA. The microampere mode is used by switching ON the input current divider. While a linear transfer is observed in the nanoampere region, the linearity in the microampere region is limited by the linearity of the current divider. This can be post-corrected by using an appropriate fitting function. Figures 21(a),21(b) plot the output spectrum for a zero input and full-scale 250nA and 250μA inputs respectively. The spectrum shows a 1st order rise in the PSD up to a frequency of 10 kHz signifying that circuit noise is the dominant noise source. This matches with the noise simulation results from the previous sub-section where we calculated the input referred current noise. 10 kHz onwards the slope shows a 3rd order rise in PSD signifying that quantization noise becomes dominant. Given the sensitive nature of the input terminals, external disturbances such as noise, leakage currents, power-line interference and other measurement artifacts easily couple to the input. In order to characterize the ADC alone, we isolate the input terminals and measure the integrated noise from the output spectrum. The full scale input is applied from an external

Fig. 15. A 3rd order SDM with charge amplifier and cascaded filters

Fig. 16. Noise analysis. (a) A two-stage miller op-amp as the core in the charge amplifier (b) Opamp Noise model

Fig. 17. Noise simulations. (a) Simulated input referred voltage and current noise components (b) Total input referred noise

Fig. 18. (a) A fully differential switched capacitor DAC with phase clock generation (b) RMS output noise current of the DAC obtained from a periodic noise simulation

Fig. 19. Plots the transfer curves for 4 dynamic ranges namely 25nA, 250nA, 25μA and 250μA.
In successive calibration steps, LCM1 is made less dominant effect of calibrating the loop-filter by monitoring the limit cycle distributions, in the absence of any calibration. At 250 kHz, the noise shaping becomes less aggressive with LCM3 operation dropping and finally being eliminated at 1 MHz. Figure 23(a) shows the effect of scaling the sampling clock on the limit cycle distributions, in response to the scaled sampling clock. Figure23(c) shows this effect. This results in an oversampling ratio (OSR) = 16. Figure 22(b) shows the effect on the in-band RMS noise current. The calibration routine has little effect when bandwidth is limited to 100 Hz due to the dominant circuit noise. The effects of the calibration routine become visible in the frequency band where quantization noise is dominant.

1) Calibrating the loop filter: Figure 22(a) demonstrates the effect of calibrating the loop-filter by monitoring the limit cycle distributions. Initially, LCM3 operation is negligible. In successive calibration steps, LCM1 is made less dominant and the operation of LCM3 is increased for more aggressive noise shaping. A frequency band of 15 kHz is selected to demonstrate this effect. This results in an oversampling ratio (OSR) = 16. Figure 22(b) shows the effect on the in-band RMS noise current. The calibration routine has little effect when bandwidth is limited to 100 Hz due to the dominant circuit noise. The effects of the calibration routine become visible in the frequency band where quantization noise is dominant.

2) Calibrating the loop filter in response to scaled clock: It is common practice to scale the sampling clock frequency in order to trade-off power consumption for faster conversion times and vice versa. Our SDM uses a continuous time loop-filter which needs to adapt its coefficients when the sampling clock frequency is scaled. We do not scale the coefficients according to a fixed look-up table. The coefficients are scaled by monitoring the limit cycle distributions. Figure 23(a) shows the effect of scaling the sampling clock on the limit cycle distributions, in the absence of any calibration. At 250 kHz sampling clock, the loop-filter is configured for aggressive noise shaping. At 500 kHz, the noise shaping becomes less aggressive with LCM3 operation dropping and finally being eliminated at 1 MHz. Figure 23(b) shows how the calibration algorithm tries to maintain the initial limit cycle distributions in response to the scaled sampling clock. Figure23(c) shows evolution of the in-band noise over the calibration steps. The in-band noise is calculated over a bandwidth of 5 kHz, 10 kHz.*

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**Fig. 19.** Measured Input-Output current transfer curve. (a) 25nA mode (b) 250nA mode (c) 25 µA mode (d) 250 µA mode

**Fig. 20.** Micrograph of the fabricated chip

**Fig. 21.** Output PSD measured from the bit-stream for a zero input and full scale input respectively (a) 250nA mode (b) 250µA mode

**Fig. 22.** Experimental results demonstrating the effect of loop-filter calibration (a) Limit cycle distributions at each calibration step (b) In-band RMS noise current at each calibration step

**TABLE I.** RMS Noise Currents obtained by integrating the Output PSD over various bandwidths

<table>
<thead>
<tr>
<th>Bandwidth</th>
<th>10 kHz</th>
<th>5 kHz</th>
<th>1 kHz</th>
<th>100 Hz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integrated RMS Noise Current</td>
<td>0.72nA</td>
<td>94.7pA</td>
<td>6.87pA</td>
<td>314fA</td>
</tr>
</tbody>
</table>
and 20 kHz for sampling frequencies of 250 kHz, 500 kHz and 1 MHz respectively, to maintain a constant OSR of 25.

As the number of quantizer bits increase, more aggressive noise shaping is made possible. Similarly, when the number of quantizer bits are lowered, the loop filter transfer function must be adapted to prevent instability. Limit cycle calibration can also be demonstrated for variable quantizer bits. However, that functionality was not implemented on this chip. The limit cycle based calibration technique is very robust, as demonstrated from the experimental results. The technique works even in the presence of significant noise, non-linearity and other non-ideal effects that could not be compensated with our technique.

The chip draws a current of 685\(\mu\)A from a 2.5V supply resulting in an average power consumption of 1.7mW. The measured RMS noise current in a 100 Hz bandwidth is 314fA which, for a full scale input of \(\pm 250\)nA, translates to 116 dB SNR or 19.2-bit resolution. The calculated figure of merit [28] is 160.6 dB.

**IX. CONCLUSION**

Reconfigurable SDMs address several application domains. While their design complexity is high, there are significant savings in terms of area and power compared to a fixed configuration SDM or several SDMs addressing each application. While seamlessly integrating with digital circuitry, they successfully address the industry’s demand for multi-mode and multi-application ADCs. With each added application (and specification), the design of reconfigurable SDMs becomes increasingly complex. In addition to the design challenge there is now a verification challenge. Predicting the SDM’s behavior in each mode becomes very difficult. This creates the need for calibration. To address this challenge, we proposed a new background calibration technique based on the limit cycle model of SDMs. The technique is based on the simple counting of the output bit-stream and categorizing bit-patterns. The calibration technique was first demonstrated using a MATLAB model with 2\(^{nd}\) order and 3\(^{rd}\) order SDMs as test vehicles. Later we also demonstrated the loop filter calibration with a test chip. A 3\(^{rd}\) order reconfigurable SDM was used in the measurement setup. The effectiveness of our limit cycle calibration technique was successfully demonstrated using this chip. The calibration technique does not require any specially generated test signals and the subsequent processing of the bit-stream is also very simple (counting bits). Due to the simplicity of the calibration technique, it can be implemented as a completely autonomous self-calibration scheme, preventing the need for any external intervention.

By virtue of its reconfigurability, coupled with the limit cycle based calibration technique, our ADC achieves a very large dynamic range (extending from hundreds of femtoamperes to 250\(\mu\)A) with an excellent current resolution of 314fA along with a widely scalable bandwidth (extending from DC to 15 kHz). The reconfigurability also allows it to operate as an incremental SDM at lower bandwidths. We report a SNR of 116 dB/19.2-bit resolution in a 100 Hz bandwidth with a FOM of 160.6 dB. Using a combination of simulation and experimental results, we have successfully demonstrated that

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Fig. 23. Experimental results demonstrating the effect of clock scaling on limit cycle distributions (a) LC distributions without calibration (b) LC distributions with calibration (c) In-band RMS noise current with a constant OSR.
it is possible to design a highly reconfigurable SDM and have it operate optimally in different modes using limit cycle based calibration.

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REFERENCES


