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Regular Brief Paper

A High-Performance SI Memory Cell

D. M. W. Leenaerts, A. J. Leeuwenburgh, and G. G. Persoon

Abstract—In this paper, we present a new type of switched current memory cell with a three phase clock cycle. The design technique is based on differential error matching, which leads to a high accuracy cell with measured errors less than 200 ppm for input currents between 50 and 85 μA . The conversion period is 700 ns, which is significantly lower, compared to other results presented in the literature, taking into account the error. Still higher speeds can be obtained by using shorter channel-length technologies.

I. INTRODUCTION

THE switched current (SI) technique is a sampled-data signal processing technique that represents analog signals by currents [1]. The technique was introduced at the end of the eighties by J. Hughes. One of the main basic building blocks in this design technique is the memory cell. Although the usefulness of the concept was demonstrated already in many applications, matching and clock feedthrough problems appeared to pose serious limitations in SI systems. To overcome these problems, several options have been proposed in the literature. Known techniques are the usage of a replica circuit [2], [3], the adjustment of transistor sizes [4], or the usage of dummy transistors. However, the first technique cancels only signal-dependent clock feedthrough currents, the second reduces the maximum operating frequency, and the last depends on the controllability of the phases of the employed clock. Another problem was the influence of the channel length modulation, resulting in a sensitivity of the output current for variations in the output voltage. This effect can be made negligible by the “regulated cascode” memory cell [5].

In this paper, we will treat a new type of memory cell, based on the regulated cascode memory cell, with improved performances. This is achieved by a new cancellation technique, described in Section II, followed by a detailed analysis and the design in Section III. In Section IV, we will present the measurements and then some conclusions in Section V.

II. THEORY

To describe the behavior of clock feedthrough more precisely, consider an NMOS SI regulated memory cell as depicted in Fig. 1. We will use an NMOS sampling switch S_1 and will refer to this cell as cell 1. In phase ϕ_1 the switch S_1 is closed and the input current i_{in} will flow through switch S_1

Fig. 1. SI-memory cell 1.

into the cell. In the next clock phase the switch S_1 is opened and S_{in} and S_{out} is closed; the current i_{out} is available at the output node. This results in a two clock phase cycle. Define $V_{g,on}$ as the on-voltage, $V_{g,off}$ as the off-voltage of the switch S_1 respectively, C_{ch} as the gate-oxide capacitance and C_{ov} as the overlap capacitance; then the total amount of error $I_{cf,1}$ in cell 1 can be expressed as:

$$I_{cf,1} = g_{m1,1} \left\{ \frac{C_{ov}}{C_1} (V_{g,off} - V_{g,on}) + \frac{1}{2} \frac{C_{ch}}{C_1} \times (V_{to,1} + (1 + n_{o,1})V_{g,1} - V_{g,on}) \right\} \quad (1)$$

with n_o the linearized body factor of the NMOS switch [6]. Subscripts 1 in g_m, n_o denote the dependency with cell 1. This equation is the same as in [1, pp. 108–110]. Consider now the situation of a memory cell designed with all PMOS transistors, except for the switch, which still remains an NMOS transistor. The error $I_{cf,2}$ for this cell 2 can be derived in a similar way as expression (1) and results in

$$I_{cf,2} = g_{m1,2} \left\{ \frac{C_{ov}}{C_2} (V_{g,off} - V_{g,on}) + \frac{1}{2} \frac{C_{ch}}{C_2} \times (V_{to,2} + (1 + n_{o,2})V_{g,2} - V_{g,on}) \right\}. \quad (2)$$

With memory transistor M_1 of both cells operating in its linear region, the error in these cells will satisfy

$$I_{cf} = \Delta I_{m1} = g_{m1} \Delta V_{gs1} = g_{m1} V_{cf} \quad (3)$$

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Fig. 2. The double memory cell.

where the sign is determined by the sign of the gate voltage and thus depends on whether a PMOS or NMOS transistor M_1 is used in combination with that particular switch S_1 . Because both errors have opposite sign cancellation occurrences and the addition of both will result in a much smaller error than the original error, under the restriction that transconductance of transistor M_1 in both cells is equal and $C_1 = C_2 = C$,

$$I_{cf,tot} = g_m \left\{ \frac{1}{2} \frac{C_{ch}}{C} [(1 + n_{o,1})V_{g,1} - (1 + n_{o,2})V_{g,2}] \right\}. \quad (4)$$

The assumption is made that $V_{to,1} = V_{to,2}$, which is valid for the process we use; otherwise a small term must be summed up in (4).

This idea can be realized by the circuit given in Fig. 2. Here we have a memory cell, consisting of two regulated cascode cells, cell 1 and cell 2. We will refer to this circuit as the double memory cell. In clock phase 1, the input current is stored in cell 1. In the next phase, it is transferred and stored into cell 2, and in clock phase 3, the current is transferred to the output node. Switches S_4 and S_3 are necessary to prevent the current from flowing during phase 1 into cell 2 and during phase 3 into cell 1, respectively.

III. DETAILED ANALYSIS AND DESIGN

To present a better description of the circuit behavior, the total error $I_{cf,tot}$ at the output has to be described in terms of currents through the memory cells instead of the gate voltages. The motivation to do this lies in the fact that the current first stored in the NMOS cell 1 differs from the current stored in the PMOS cell 2, on account of the (intermediate) error introduced

TABLE I
TRANSISTOR DIMENSIONS

($V_{dd}=5V$, $V_{b1}=3.51V$, $V_{b2}=1.38V$, $V_{b3}=2.5V$)

transistor	dimension W/L ($\mu m/\mu m$)
M1	4.8/2.4
M2,M3,M13,M14,M15,M16,M17	2.4/24
M4	4.8/4.8
M5,M11	3.6/2.4
M6,M12	7.2/2.4
M7	12/2.4
M8,M9	60/2.4
M10	2.4/2.4

in cell 1. The gate voltages in (4) have to be replaced by

$$\begin{aligned} V_{g1,1} &= V_o + \frac{i_{in}}{g_m} \\ V_{g1,2} &= V_{dd} - V_o + \frac{i_{in} + I_{cf1}}{g_m} \end{aligned} \quad (5)$$

to express the total clock feedthrough error as a function of the signal current, together with the error generated in memory cell 1. V_o represents the minimum voltage to keep M_1 in its linear region. This yields

$$\begin{aligned} I_{cf,tot} &= g_m \frac{1}{2} \frac{C_{ch}}{C} \left[(2 + n_{o,1} + n_{o,2})V_o - (1 + n_{o,2})V_{dd} \right. \\ &\quad \left. + (2 + n_{o,1} + n_{o,2})\frac{i_{in}}{g_m} + (1 + n_{o,2})\frac{I_{cf1}}{g_m} \right]. \end{aligned} \quad (6)$$

A better insight is given when the (linearized) body factors are neglected, resulting in:

$$I_{cf,tot} = g_m \frac{1}{2} \frac{C_{ch}}{C} \left[2V_o - V_{dd} + 2\frac{i_{in}}{g_m} + \frac{I_{cf1}}{g_m} \right]. \quad (7)$$

Comparing (7) with (1) shows that a large part of the error is cancelled by the proposed method. However the clock feedthrough still depends on the signal current. This may cause a problem: an increasing signal current will result in an increasing gate voltage in the NMOS cell, while the gate voltage in the PMOS cell will decrease. The signal dependency of the current in the double cell will be two times higher, as compared with the single SI memory cell. This means that the proposed method is only useful for a certain range of input currents.

The double cell of Fig. 2 was designed such that input currents from 60 μA up to 100 μA could be memorized with a small error at a high conversion rate, resulting in a circuit as depicted in Fig. 3. The circuit was designed to achieve a conversion rate of 1 MHz with an error of less than 200 ppm. These results were predicted by SPICE simulations for a design in a 2.4- μm N -well CMOS process. In Table I, the dimensions of the transistors are given together with the power supply voltages. To assure stability, transistor M_{17} is used, which connects the output node of cell 2 at half the power supply voltage during clock phase 1. In Fig. 4, the clock cycle is given. In practice, the clock edges are nonoverlapping.

Fig. 3. The designed double cell.

Fig. 4. The clock cycle.

IV. MEASUREMENTS

Fig. 5 shows a photograph of the chip with a die area of $100 \times 50 \mu\text{m}^2$. The clock control logic was not implemented on the chip for test purposes. For testing, we used a 16-b DA converter to generate the input current. Using a virtual ground-point, the output current was measured by a 16-b AD converter. The timing of the clock control logic as well as the AD- and DA-converters were controlled by a microprocessor. In Fig. 6, the error in ppm is depicted, measured at a conversion rate of 700 ns. For a 1-KHz tone having a $22.5\text{-}\mu\text{A}$ amplitude ($67.5\text{-}\mu\text{A}$ bias current), the measured THD is 0.11%. Despite the fact that the measured error also includes a small contribution

Fig. 5. Die photograph of the circuit.

Fig. 6. The measured error.

of settling errors, this result is significantly better than results obtained in the literature so far. The accuracy is similar to the cell presented in [7] which has a conversion rate of 1 ms. In [8] the clock rate is about 100 ns but the precision is less. In [9] an S^2I cell is proposed with a simulated error of 700 ppm at 15 ns (designed in $0.8 \mu\text{m}$ CMOS). To the authors' knowledge, the double cell seems to have the best combination of accuracy and speed. We reasonably may expect that much higher speeds can be achieved if submicron technology will be used.

V. CONCLUSION

A new SI memory cell is proposed, based on differential error matching. The conversion rate can be up to several megahertz with an acceptable error. Certainly compared to the already proposed circuits in the literature, the double cell is better suited for applications in high-performance and high-quality SI circuits.

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