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Noise in DMOS Transistors
in a BICMOS-Technology

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Abstract—An experimental and theoretical study of the 1/f noise and the thermal noise in double-diffused MOS (DMOS) transistors in a BICMOS-technology has been carried out. By using an analytical model that consists of an enhancement MOS transistor in series with a depletion MOS transistor and a resistance, and by attributing noise sources to each device, the noise in DMOS devices is simulated accurately. Three distinct regions of operation are defined: enhancement transistor control, depletion transistor control and the linear region. In the first region, the noise is strictly determined by the enhancement transistor. It was found that the 1/f noise in this region is caused by mobility fluctuations and is very low. In the depletion transistor control region both transistors influence the total noise. Here the 1/f noise is dominated by the depletion transistor. The series resistance is only of importance in the linear region.

I. INTRODUCTION

At present, many applications require the integration of high-voltage devices in Integrated Circuits. This demands the use of a technology that combines bipolar (BJT), CMOS and DMOS transistors on a single chip. DMOS transistors have a high breakdown voltage, which allows them to be used in specific applications. Formerly, DMOS devices were principally used in high-power switches, but with the integration of these transistors in BICMOS-technology, other applications, such as high-voltage digital cells, high-voltage current sources and operational amplifiers, have come within reach.

The use of DMOS transistors in high-power switches did not really require low-noise performance, but with the introduction of the above-mentioned applications the noise behavior of DMOS transistors has become important. In order to reduce the output noise of an operational amplifier, for example, it is essential to have a better understanding of the noise mechanisms in DMOS transistors.

Considering the above, it does not seem strange that few articles have been written on noise in DMOS transistors up to now [1]–[3]. On top of this, no model was available to explain the results. In this paper a model for DMOS transistors is introduced, which describes both the 1/f noise and the thermal noise.
Fig. 2. (a) Macromodel for the n-type DMOS transistor. The depletion and enhancement MOS transistors have the same width, but different length, threshold voltage and gain parameter denoted by $L_D, L_E; V_{TD}, V_{TE};$ and $\beta_D, \beta_E$, respectively. (b) DMOS equivalent circuit with added noise sources.

The gain parameter $\beta$ and the body factor $\delta_E$ of the enhancement transistor are defined by

$$I_D = \beta_E (V_G - V_{T_E}) V_X - \frac{1}{2} (1 + \delta_E) V_X^2$$

$$\delta_E = \frac{\gamma_E}{2\sqrt{2}\phi_{FE}}$$

where $\gamma_E$ denotes the body effect coefficient of the enhancement transistor (in $V^{1/2}$), $\phi_{FE}$ denotes the Fermi level of the enhancement transistor relatively expressed in units of $kT/q$, and $n_i$ represents the intrinsic electron concentration of silicon (in electrons/cm$^3$), and $N_E$ stands for the doping concentration in the p-Base (in atoms/cm$^3$).

In contrast to [7], we take the body effect into account in the equations. The channel in the p-Base is not doped uniformly due to lateral diffusion. This means that the doping concentration varies along the channel. In order to model this channel with one enhancement transistor only, an effective channel length $L_E$ and an effective doping concentration $N_E$ have to be introduced [7]. The effective channel length differs from the physical channel length, and the effective doping concentration $N_E$ is smaller than the maximum doping concentration in the channel.

Furthermore it should be noted that the depletion transistor is in an accumulation layer. This implies that no depletion layer is formed under the gate in the n-Tub and thus no body effect has to be taken into account.

The DMOS device pinches off whenever the channel of either transistors pinches off. The external drain-to-source voltage for which the enhancement transistor pinches off is $V_{DSE}$, and the external drain-to-source voltage for which the depletion transistor pinches off is $V_{DSD}$. The two drain saturation voltages can be solved from (1) and (2). The physical solutions read as follows:

$$V_{DSE} = V_G - V_{TD}$$

$$V_{DSD} = V_G - V_{TE} + \sqrt{A + I_D R_D}$$

where $\gamma_E = \frac{\gamma}{2\sqrt{2}\phi_{FE}}$, $\phi_{FE}$ is the Fermi level of the enhancement transistor relatively expressed in units of $kT/q$, $n_i$ is the intrinsic electron concentration of silicon (in electrons/cm$^3$), and $N_E$ is the doping concentration in the p-Base (in atoms/cm$^3$).
From (7) and (8), we find
\[ V_{DSE} = V_{DSD} - \sqrt{A}. \] (9)

This implies that \( V_{DSE} \leq V_{DSD} \), unless the term \( A \) is negative and, therefore, \( V_{DSE} \) is nonexistent. Both transistors are on the brink of saturation if \( V_{DSE} = V_{DSD} \), i.e., if the term \( A = 0 \). Physically, this occurs with
\[ V'_G = V'_{GT} = \frac{(1 + \delta_E)\Delta V_T}{\sqrt{\beta(1 + \delta_E) - \delta_E}}. \] (10)

Assuming that \( \beta' > \delta_E/(1 + \delta_E) \), which is normally the case for values of effective doping concentration \( N_E \) that are not too high, the effective transition gate voltage \( V'_{GT} \) has a positive value. Now analogous to [7], three different regions of operation can be defined for the DMOS-transistor:

**Region 1—Enhancement Transistor Control:** For \( V_{DS} \geq V_{DSE} \) and \( 0 \leq V'_G \leq V'_{GT} \), the term \( A \) is positive and hence \( V_{DSE} \) is nonexistent. The enhancement transistor is in the linear region and the depletion transistor is in saturation. Although the depletion transistor may operate in its saturation region or its linear region, the drain current is only determined by the enhancement transistor in this region
\[ I_D = \frac{\beta_E}{2(1 + \delta_E)} V_G^2. \] (11)

The transconductance \( g_m \) is
\[ g_m = \frac{\partial I_D}{\partial V_{GS}} \bigg|_{V_{DS}} = \frac{\beta_E}{(1 + \delta_E)} V_G'. \] (12)

The DMOS device acts as a single MOS transistor.

**Region 2—Depletion Transistor Control:** For \( V_{DS} \geq V_{DSE} \) and \( V'_G > V'_{GT} \), the enhancement transistor is in the linear region and the depletion transistor is in saturation. In this region, the drain current is determined by the depletion transistor.

**Region 3—Linear Region:** For \( V_{DS} < V_{DSE} \) and \( 0 \leq V'_G \leq V'_{GT} \) or \( V_{DS} < V_{DSE} \) and \( V'_G > V'_{GT} \), both the enhancement transistor and the depletion transistor are in the linear region. In this case the influence of the series resistance on the drain current equation becomes very important.

In Fig. 3, the drain current \( I_D \) (a) and the transconductance \( g_m \) (b) of a typical p-type DMOS transistor are depicted as a function of the effective gate voltage \( V_G' \) for \( V_{DS} = -10 \) V, ignoring possible mobility reduction. At low effective gate voltages the DMOS transistor operates in Region 1, and the transconductance increases linearly with \( V'_G \) in agreement with (12). For \( V'_G = V'_{GT} \) the transconductance reaches a maximum. With effective gate voltages \( |V'_G| \) just above \( |V_{GT}| \) as the DMOS transistor passes into Region 2, the transconductance decreases momentarily. After that, it starts to increase linearly with effective gate voltage. At very high effective gate voltages the DMOS transistor is no longer in saturation, and it operates in Region 3.

**III. DMOS NOISE MODEL**

In order to calculate the noise model, a noise source is attributed to each device of the equivalent circuit in Fig. 2(a), in the same way as was done for MOS tetrodes in [9]. The resulting circuit is shown in Fig. 2(b).

The two MOS transistors (i.e., the inversion or accumulation layer they stand for) exhibit both thermal noise and flicker noise. The thermal noise in MOS transistors has been extensively studied and is well understood [9], [10]. For a single MOS transistor the thermal noise part of the drain current spectral density \( S_I \) was calculated in [11]. Here, we calculate the thermal noise introducing the body effect: \( 0 \leq \eta \leq 1 \)
\[ S_I = 4kT\beta(V_{GS} - V_T)\left(1 - \eta + \frac{1}{2}\eta^2\right) \left[1 - \frac{1 - \eta}{1 - \frac{1}{2}\eta}\right], \] (13)
where
\[ \eta = \frac{(1 + \delta) V_{DS}}{(V_{GS} - V_T)}. \]

In the saturation region, where \( \eta = 1 \), this gives
\[ S_I = \frac{8}{3}kT\mu C_O L (V_{GS} - V_T). \] (14)
Although many papers have been written on the origin of $1/f$ noise in MOS transistors, a generally accepted model explaining the $1/f$ noise in all n- and p-channel MOS transistors is still lacking. Most models concerning the $1/f$ noise can be roughly divided into two schools of thought: the $\Delta\eta$ model and the $\Delta\mu$ model as origins of conductance fluctuations. According to [12] and [13], the flicker noise in n-channel MOS transistors often seems due to carrier-density fluctuations, while the flicker noise in p-channel MOS-transistor is easier to interpret in terms of mobility fluctuations.

Without making a distinction between the $\Delta\eta$ model and $\Delta\mu$ model, the flicker noise in MOS transistors can be written as [14], again introducing the body effect

$$S_I = \frac{\mu IV_{DS} \alpha}{L^2 f} = \frac{\mu^2 C_{OX} W}{L^3} \left( V_{GS} - V_T - \frac{1}{2}(1+\delta)V_{DS} \right)^2 \frac{\alpha}{f}. \quad (15)$$

In saturation the current becomes

$$I_{SAT} = \mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T \right)^2 \quad (16)$$

and the noise becomes

$$S_I = \frac{2qI_{SAT}^2 \alpha}{C_{OX} (V_{GS} - V_T) W L f} = \frac{\mu^2 C_{OX} W}{2(1+\delta)^2 L^3} \left( V_{GS} - V_T \right)^2 \frac{\alpha}{f} \quad (17)$$

The $1/f$ noise parameter $\alpha$ is used as a figure of merit and its value is geometry independent in both models. Under certain circumstances [13], the $\Delta\mu$ model predicts a gate-voltage-independent $\alpha$ value. $\alpha$ values have been measured in the range of $10^{-3}$ to $10^{-7}$. The $\Delta\eta$ model, on the other hand, predicts an $\alpha$ value that is proportional to the oxide thickness $t_{OX}$ and inversely proportional to the effective gate voltage $V_{GS}$ [11]: $\alpha \propto \frac{t_{OX}}{V_{GS} - V_T}$.

In order to calculate the total drain-current noise spectral density of the DMOS transistor, all terminals of the DMOS device are assumed to be short-circuited to ground. In this case the equivalent circuit of the DMOS transistor in Fig. 2(b) leads to the small-signal circuit in Fig. 4, where the ac-signal $V_{GS} = 0$.

In Fig. 4, the symbols in (18)–(20), shown at the bottom of the page, are used. Elaborating the Kirchhoff equations related to Fig. 4, the following formula for $i_T$ is obtained

$$i_T = \frac{(g_{m_D} + g_{d_D}) i_E + g_{d_E} i_D + g_{d_D} g_{d_E} R_D i_R}{g_{d_D} + g_{d_E} + g_{m_D} + g_{d_D} g_{d_E} R_D} \quad (21)$$

and (22), shown at the bottom of the page. The transconductance $g_{m_E}$ of the enhancement MOS transistor is given by

$$g_{m_E} = \begin{cases} \beta_E V_X, & \text{for } V_X < \frac{V'_{GS}}{\beta_E}, \\ \frac{g_{d_E}}{1+\delta_E}, & \text{for } V_X \geq \frac{V'_{GS}}{\beta_E}. \end{cases} \quad (23)$$

Using a small-signal circuit where the ac-signal $V_{GS} \neq 0$, we find the following for the transconductance $g_m$ of the DMOS transistor

$$g_m = g_{m_D} g_{d_E} + g_{m_D} g_{m_D} + g_{d_D} g_{m_E}, \quad (24)$$

Combining (22) and (24), the equivalent input voltage noise is given by (25), shown at the bottom of the next page. Now for the different operating regions as mentioned in Section 2, the equivalent input voltage noise can be simplified to:

**Region 1—Enhancement Transistor Control:** The enhancement transistor is in saturation, which indicates that $g_{d_D} = 0$. Using (14), (17), (23) and (25) we find

$$S_{V_{eq}}(f) = \frac{S_{Ie}(f)}{g_{m_E}^2} = \frac{8kT(1+\delta_E)^2}{3\beta_E V'_G} + \frac{qV'_{G}}{2C_{OX} W L E} \frac{\alpha_E}{f} \quad (26)$$

$$g_{d_D} = \begin{cases} \beta_E (V'_G - (1+\delta_E) V_X), & \text{for } V_X < \frac{V'_{GS}}{1+\delta_E}, \\ 0, & \text{for } V_X \geq \frac{V'_{GS}}{1+\delta_E}. \end{cases} \quad (18)$$

$$g_{m_D} = \begin{cases} \beta_D (V_X - V'_G), & \text{for } V_D < V'_G \Delta V_T + I_D R_D, \\ \beta_D (V'_G + \Delta V_T - V_X), & \text{for } V_D \geq V'_G + \Delta V_T + I_D R_D. \end{cases} \quad (19)$$

$$g_{d_D} = \begin{cases} \beta_D (V'_G + \Delta V_T - V'_G), & \text{for } V_D < V'_G \Delta V_T + I_D R_D, \\ 0, & \text{for } V_D \geq V'_G + \Delta V_T + I_D R_D. \end{cases} \quad (20)$$

$$S_{Ie}(f) = \frac{(g_{m_D} + g_{d_D})^2 \cdot S_{Ie}(f) + g_{d_D}^2 \cdot S_{Ie}(f) + (g_{d_D} g_{d_D} R_D)^2 \cdot S_{Ie}(f)}{(g_{d_D} + g_{d_D} + g_{m_D} + g_{d_D} g_{d_D} R_D)^2} \quad (22)$$
As was to be expected, the total noise in this region is strictly determined by the enhancement transistor.

Region 2—Depletion Transistor Control: The depletion transistor is in saturation and the enhancement transistor is in the linear region. This implies that \( g_{dD} = 0 \) and \( g_{de} \neq 0 \), so again using (25), we find

\[
S_{V_{th}}(f) = \frac{S_{I_{th}}(f)}{(g_{de} + g_{me})^2} + \left( \frac{g_{de}}{g_{me}} \right)^2 \frac{S_{I_{d}}(f)}{(g_{de} + g_{me})^2}. \quad (27)
\]

If thermal noise only is considered, using (13), (14), (18), (19), and (23), we find that (27) becomes

\[
S_{V_{th}}(f) = \frac{4kT V_G}{\beta_E (V_G' - \delta_E V_X)^2} \left( \frac{V_X'}{V_G' - \delta_E V_X} \right)^2 \left( 3 \frac{8kT}{\beta_E (V_G' + \Delta V_T - V_X)} \right). \quad (28)
\]

Considering the flicker noise, using (15), (17)–(19), and (23), we find that (27) gives

\[
S_{V_{th}}(f) = \frac{q}{C_{ox}} \left( \frac{V_G'}{V_G' - \delta_E V_X} \right)^2 \left( \frac{\alpha_E}{f} \right) \quad (29)
\]

In this region both the enhancement and the depletion transistor determine the total noise.

Region 3—Linear Region: If \( V_{DS} \ll V_G \), using (18), (19), (20) and (23), (25) can be approximated by (30), shown at the bottom of the page. For large \( R_D \) the noise contributed by the series resistance becomes dominant. The noise in this region was not subject to any further experimental study.

As regards p-type DMOS devices, all voltages and currents in formulae (1) to (30) have to be multiplied by \(-1\).

IV. EXPERIMENTAL RESULTS

Noise measurements were only performed on p-type DMOS transistors, because these devices are often used in operational amplifiers, which makes noise an important feature.

The channel lengths of the DMOS transistors under examination are fixed \((L_E = 4 \mu m, L_D = 12 \mu m)\), and different channel widths \( W (= W_E = W_D) \) were used \((W = 7 \mu m, 50 \mu m \) and \(100 \mu m)\).

All of the noise experiments were done in saturation (i.e., Regions 1 and 2).

First of all, the dc-characteristics were studied and parameters were extracted, so that the dc-characteristics could be properly simulated for a large range of channel widths and for low gate voltages. Thus, the occurrence of a negative dynamic resistance is avoided.

For simulations to be accurate, the mobility reduction due to the transverse gate field has to be taken into account too. Here only the reduction of the surface mobility \( \mu_E \) of the enhancement transistor is taken into account. It is expressed by the empirical SPICE relation

\[
\mu_E = \begin{cases} 
\mu_0, & V_G' \leq \frac{U_{CRIT}}{C_{ox} V_G'} \\
\mu_0 \left( \frac{U_{CRIT}}{C_{ox} V_G'} \right)^{U_{EXP}}, & V_G' > \frac{U_{CRIT}}{C_{ox} V_G'}
\end{cases} \quad (31)
\]

where \( U_{CRIT} \) stands for the critical field for mobility degradation (in V/m), above which mobility reduction sets in. \( U_{EXP} \) stands for the critical field exponent, which determines the dependency of the mobility on the gate voltage, and \( \mu_0 \) is the surface mobility in the inversion layer at low gate voltages. Both the parameters \( U_{CRIT} \) and \( U_{EXP} \) were fitted for the dc-characteristics.

The transconductance of the device under test was measured in order to determine the equivalent input voltage noise. Next, the drain-current spectral density \( S_{I_{th}} \) was measured in the frequency range 10 Hz to 100 kHz, and converted to the equivalent input noise voltage \( S_{V_{th}} \) using (25).

1/f Noise: In Fig. 5, the measured \( S_{V_{th}} \) and transconductance \( g_m \) are plotted as a function of \( V_G' \) for a DMOS transistor with \( W = 100 \mu m \). No acute change in transconductance \( g_m \) can be observed at \( \frac{1}{V_{ATI}} \), i.e., Region 1, the equivalent input voltage noise \( S_{V_{th}} \) increases proportionally to \( \frac{1}{V_{ATI}} \). For \( \frac{1}{V_{ATI}} > \frac{1}{V_k T} \), i.e., Region 2, the equivalent input voltage noise \( S_{V_{th}} \) starts to increase more rapidly as the noise contribution of the depletion transistor comes into play and becomes dominant.

Equation (26) is adjusted for mobility reduction in the enhancement transistor for high bias voltages, using (31). The adjusted equation is used to determine parameter \( \alpha_E \).
from the experimental results for $|V'_G| < |V'_{GD}|$, $\alpha_E$ as a function of $|V'_G|$ is shown in Fig. 6. As can be seen here, $\alpha_E$ is gate-voltage-independent. This implies that the $1/f$ noise in the enhancement transistor is caused by mobility fluctuations. It has been shown before that the flicker noise in $p$-channel transistors is often due to mobility fluctuations [12], [13], presumably because these transistors often have a buried channel at a large distance from the oxide interface.

Assuming that $\alpha_E$ remains constant for $|V'_G| > |V'_{CE}|$ and adjusting (29) for mobility reduction, using (31), the parameter $\alpha_D$ was calculated and is depicted as a function of $|V'_G|$ in Fig. 6. Note that $\alpha_D$ is gate-voltage-dependent, which may indicate that the noise in the depletion transistor is caused by number fluctuations. The $\Delta n$ model predicts that, for this case, $\alpha_D$ should be inversely proportional to $|V_G - V_{TD} - V_X|$. Therefore, $\alpha_D$ is plotted as a function of $|V_G - V_{TD} - V_X|$ for DMOS transistors with different channel widths $W$ in Fig. 7. The figure shows that the flicker noise induced by the accumulation layer in the $p$-epitaxial layer, modeled by the depletion transistor, is due to number fluctuations. The accumulation layer is formed close to the Si-SiO₂ interface, which may explain why the fluctuations caused by the tunnelling of free-charge carriers into oxide traps are dominant here.

For $W = 50 \, \mu m$ and $W = 100 \, \mu m$, parameter $\alpha_D$ is in the same order of magnitude, whereas for $W = 7 \, \mu m$, $\alpha_D$ is somewhat higher. The latter may be due to narrow channel effects. Narrow channel devices suffer more from parasitic channels at the edges, resulting in increased $1/f$ noise.

The parameter $\alpha_E$ was also determined for several transistors with different channel widths (the results are shown in Fig. 8). Again with $W = 50 \, \mu m$ and $W = 100 \, \mu m$, parameter $\alpha_E$ is roughly the same, whereas with $W = 7 \, \mu m$, $\alpha_E$ is somewhat higher due to parasitic narrow channel effects.

The nonuniformly doped channel in the $n$-well results in the use of an effective channel length $L_E$ for the enhancement transistor. This effective channel length differs from the physical channel length. The effective channel length was used to determine $\alpha_E$. If the physical channel length had been used instead, $\alpha_E$ would have been about 30% higher. Despite this fact, the parameter $\alpha_E$ is about $1 \times 10^{-7}$ for this BICMOS-technology.

As in the case of the $\Delta \mu$ model, $\alpha$ is geometry and voltage-independent. It can easily be used as a figure of merit to compare the noise behavior of ($p$-type) transistors from different technologies, as was done in [13]. The results of [13], in which a comparison is made between twelve different CMOS manufacturers from the United States, Japan and Europe, shows $\alpha$ values between $1 \times 10^{-6}$ and $8 \times 10^{-6}$. This means that the noise parameter $\alpha$, for the technology under examination, has one of the lowest values ever measured.

The flicker noise was simulated for a transistor with $W = 100 \, \mu m$ using a constant parameter $\alpha_E$ and a gate-voltage-dependent parameter $\alpha_D$. The simulated and the measured $1/f$ noise are shown in Fig. 9, where we see that the simulated values correspond rather well to the measured values.

**Thermal Noise:** The thermal noise of the DMOS transistors was measured at $f = 100 \, kHz$, where the flicker noise is
A novel model for the noise in lateral DMOS transistors in BICMOS-technology has been demonstrated. The model is based on a series circuit of an enhancement MOS transistor, a depletion MOS transistor and a series resistance, where a noise source is attributed to each separate device. In the saturation region, the DMOS device noise is exclusively caused by the noise in the two transistors. The proposed noise model was experimentally verified for p-type DMOS transistors in saturation; the theoretical results correspond well to the measured results.

For gate voltages below a certain value $V_{GT}$ and under conditions of saturation, the drain current and its noise are strictly determined by the enhancement transistor (i.e., the diffused portion of the DMOST channel). In this region the $1/f$ noise and the thermal noise behave the same way as they would in a single (enhancement) MOS transistor. The $1/f$ noise in the enhancement transistor is caused by mobility fluctuations, and the noise parameter $\alpha_E$ is about $1 \times 10^{-7}$, which is one of the lowest values ever measured for $\alpha$.

For gate voltages above $V_{GT}$ and under conditions of saturation, both transistors influence the noise behavior of the DMOS device. At the onset of this region, the $1/f$ noise increases sharply. The flicker noise in the depletion transistor (i.e., the uniform portion of the DMOST channel) can be ascribed to carrier number fluctuations. As a result, it is much higher than the flicker noise contributed by the enhancement transistor. Therefore, the total $1/f$ noise in this region is principally controlled by the noise in the depletion transistor. In fact, the abrupt transition in the $1/f$ noise at $V_G = V_{GT}$ is basically caused by a sharp difference in spatial noise sources that become dominant at the device terminals. As the thermal noise in the enhancement transistor and the thermal noise in the depletion transistor are due to the same physical mechanism and are in the same order of magnitude, no sharp transition can be seen around $V_G = V_{GT}$ for the thermal noise of the DMOS device.

In the linear region, the total noise is not determined by the two transistors only, but also by the series resistance. The latter plays an important role in the noise behavior of DMOS devices in this region, depending on its value and its noise contribution. The noise in the linear region still requires more extensive study.

V. CONCLUSION

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Ronald van Langevelde (S'95) was born in Terneuzen, The Netherlands, on May 18, 1971. He received the Master's degree in electrical engineering from the Eindhoven University of Technology, The Netherlands, in 1994. This present paper is part of his Master's thesis, with the work performed at Alcatel Mietec, Brussels, Belgium. He is currently working toward the Ph.D. degree in electrical engineering at the Eindhoven University of Technology.

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L. K. J. Vandamme was born in De Panne, Belgium, on October 22, 1943. He received the Master's degree of electrical engineering (cum laude) from Delft University of Technology, The Netherlands, in 1971, and the Doctorate degree from the Eindhoven University of Technology, The Netherlands, in 1976. He has done research on $1/f$ noise in electrical contacts, thick-film resistors, and Bi Films. His current areas of research are $1/f$ Noise in MOSFET's and optoelectronic devices. He has authored or co-authored more than 90 publications. During 1981–1982, 1986–1987, and 1992, he held a visiting Professorship at the University of Science and Technology, Montpellier, France.