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Thermal Stress Reduction of Power MOSFET in Electric Drive Application with Dynamic Gate Driving Strategy

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Abstract—While operating an electric drive under different load conditions, power semiconductor devices experience thermal stress which compromises lifetime. In this paper, a model based gate voltage control is proposed to reduce the thermal stress by shaping the profile of conduction losses. Thermal stability criteria are introduced, which confine the gate voltage range to prevent current focalization and local heat up. This method is verified by using a custom proof-of-concept gate driver that supplies an adjustable three-level gate voltage. A three-phase electric drive is prototyped, on which power cycling tests are conducted and the results confirm the thermal control method.

Index Terms—Gate driver, Power MOSFET, Modelling, Lifetime, Electric drive

I. INTRODUCTION

In electric motor drives, multiple power switches are incorporated to meet fault-tolerant, high efficiency and high precision requirements [1], [2]. Therefore, the lifetime of the power switches significantly influences the reliability of the power converters.

Thermal cycling of the power switches causes package related wear-out, such as bond-wire degradation, reconstruction of chip metallization and solder fatigue [3]. These are caused by the mechanical stress between contact materials with different thermal expansion coefficients and thermal gradient. Countermeasures of thermal stress have been investigated in [4] to enhance the lifetime of power switches by reducing the junction temperature swing ΔT_J .

Active thermal management through the gate drive unit is found to be a promising solution due to its flexible implementation. For instance, a two-step gate driver is proposed in [5] to regulate the switching transient by adjusting the dv/dt , and therefore controlling the switching losses. Also gate drivers with switchable gate resistor arrays are proposed to manipulate the switching losses [6], where resistors with a different value are selected according to the estimated feedback junction temperature. In [7], the power MOSFET is operated in the saturation region to dissipate additional losses for further reducing ΔT_J . Gate voltage as a control variable is applied in [8], which smooths the temperature profile by adjusting the conduction losses. However, associated local heat

up and current focalization problems are observed in [9], while operating with low gate voltage.

The objective of this paper is to develop a dynamic gate voltage control method for thermal stress reduction of silicon-carbide power MOSFETs. The paper is structured as follows. Section II begins by introducing a McNutt Hefner model to describe characteristics of the power MOSFET. After that, a power losses model is developed, and, based on which a dynamic gate voltage expression is derived to reshape the power losses and smooth the junction temperature. To ensure a safety operation, thermal stability criteria are investigated to confine the gate voltage range, such that current focalization and the associated local heat-up are avoided. In section III, an electro-thermal equivalent circuit model is built up to extract both the power losses and the corresponding junction temperature. The system operation principle is developed to incorporate the dynamic gate voltage control method into an electric drive system to reduce the thermal stress caused by the output load steps. Simulations are conducted in section IV based on an electric drive system for validation. The results suggest reduced temperature swing ΔT_J by hardly compromising any system efficiency. Lifetime estimation is conducted in section V, and the results indicate an improvement of 53.0%. Section VI focuses on experimental verification, where a proof-of-concept three-level gate driver and an electric motor drive prototype are realized, on which thermal cycling tests are carried out. The junction temperature is measured, and the results confirm the capability of the proposed thermal control method. At last, conclusions are presented.

II. DYNAMIC GATE VOLTAGE DERIVATION

To shape the temperature profile of a power MOSFET, the power losses have to be controlled. During the conduction stage, the power losses P_{con} depend on the drain current I_d and drain-source voltage V_{ds} by $P_{con}(t) = I_d(t) \cdot V_{ds}(t)$. Varying $V_{ds}(t)$ can be realized with a proper gate voltage $V_{gs}(t)$, which therefore can stabilize the fluctuation of P_{con} , caused by a varying load profile. In this section, an analytical power MOSFET model and an associated parameter extraction method are introduced at first to describe the MOSFET

behaviors. After that, an expression of the conduction losses is derived and evaluated. Based on this expression, a dynamic gate voltage control method is proposed to shape the power losses profile. Furthermore, to avoid the thermal runaway problem that occurs at low gate voltage levels, thermally stable operation criterions are developed to set a boundary of the gate voltage operation range.

A. Power MOSFET Modelling

To analyze the MOSFETs static and dynamic behavior, analytical models that describe the relationship between the gate-source voltage V_{gs} , drain-source voltage V_{ds} and drain current I_d have been developed. The Hefner model in [10] [11] [12] is developed to account for the linear behavior of the transfer curve at high current and gate voltage levels, whereas the electron mobility is reduced as a result of a high transverse electric field. In addition, separate linear and saturation transconductance with different values are used to incorporate the effects of carrier diffusion due to the nonuniform channel dopant density. Moreover, temperature dependent parameters are included to model and explain the temperature-related characteristic drift behavior.

By taking the model accuracy and complexity into account, the following McNutt Hefner model [10] is adopted for gate voltage derivation:

$$I_d = \begin{cases} \frac{K_{lin} \left[(V_{gs} - V_{th})V_{ds} - \frac{K_{lin}V_{ds}^2}{2K_{sat}} \right]}{[1 + \theta \cdot (V_{gs} - V_{th})]}, & \text{if } V_{ds} \leq V_{pin}; \\ \frac{K_{sat}(V_{gs} - V_{th})^2}{2[1 + \theta \cdot (V_{gs} - V_{th})]}, & \text{if } V_{ds} > V_{pin}, \end{cases}$$

with the pinch-off voltage $V_{pin} = (V_{gs} - V_{th}) \frac{K_{sat}}{K_{lin}}$,

$$K_{lin}(T) = K_{lin}(T_0) \left(\frac{T_0}{T} \right)^{K_t}, \quad K_{sat}(T) = K_{sat}(T_0) \left(\frac{T_0}{T} \right)^{K_t}$$

and $V_{th}(T) = V_{th}(T_0) + V_k(T - T_0)$.

(1)

In the above model, K_{sat} and K_{lin} are the saturation and linear region transconductance respectively, and θ is the transverse electric field parameter [11]. Different parameter extraction sequences are proposed in [12] [13], and the Levenberg-Marquardt curve-fitting method which shows the least relative variation is implemented here. This method is carried out based on the measurement data of the iv -characteristic curve at both 25 °C and 150 °C as taken from the data sheets. After applying to the model (1), the extracted parameter values are listed in Table I.

The fitted model and the data obtained from the data sheet are then illustrated in Fig. 1 (a) and (b), which indicate a good modelling accuracy.

It is worth noting that the extracted parameter values in Table I might be physically inviable, for instance, the gate

TABLE I: Parameter values of the Hefner model in (1).

Parameter Name	Symbol	25 °C	150 °C
Linear region transconductance (A/V ²)	K_{lin}	1.03	0.52
Saturation region transconductance (A/V ²)	K_p	1.08	0.55
Transverse electric field parameter (V ⁻¹)	θ	0.05	0.05
MOSFET gate threshold voltage(V)	V_{th}	6.83	0.50
channel-length modulation parameter (V ⁻¹)	γ	0.01	0.01

threshold voltage V_{th} is too large at 25 °C and close to zero at 150 °C. In spite of this, the gate voltage $V_{gs}(t)$ can be derived based on this model, since discrepancies are small, which shows its capability of providing a precise analytical description.

B. Power Losses Modelling

Electric machines employed in the electric vehicles are generally operated at high speed conditions. The output current frequency typically ranges from a few hundreds to thousand Hertz. The power losses and the corresponding junction temperature T_J of power switch devices are then determined by the load profile I_L , or equivalently, the RMS value of the drain current.

By applying a sinusoidal load current $I_{load}(t, \tau)$ at a frequency of $\omega_e = 2\pi/T_L$, with the duty cycle $d(\tau)$ that is modulated with index D and D₃ for the 1st the 3rd order harmonic respectively. The cycle-to-cycle RMS current in an electrical period T_L can be derived as

$$I_{d,rms,cc}(t) = \sqrt{\frac{1}{T_L} \int_{-\pi/2\omega_e}^{3\pi/2\omega_e} I_{load}(t, \tau)^2 \cdot d(\tau) d\tau} = \frac{I_L(t)}{2},$$

whereas $I_{load}(t, \tau) = I_L(t) \cdot \cos(\omega_e \tau)$, $\tau \in [-\pi/2\omega_e, 3\pi/2\omega_e]$,

and the duty cycle

$$d(\tau) = \frac{D}{2} \cos(\omega_e \tau + \phi_{load}) + \frac{D_3}{2} \cos(3\omega_e \tau + 3\phi_{load}) + \frac{1}{2},$$

with load angle ϕ_{load} .

(2)

Next, the conduction loss produced in each electrical period T_L is set to a constant by

$$\langle P_{con, T_L} \rangle(t) = \frac{1}{T_L} \int_{-\pi/2\omega_e}^{3\pi/2\omega_e} V_{ds}(t, \tau) \cdot I_d(t, \tau) d\tau$$

$$\cong V_{ds,rms,cc}(t) \cdot I_{d,rms,cc}(t) = P_{const},$$

with $P_{const} = \text{Max}[\langle P_{con, T_L} \rangle(t)]$. The maximum power losses P_{const} can be obtained by calculating the average power losses within the period where the amplitude of load profile $I_L(t)$ equals to its maximum value. The voltage term $V_{ds,rms,cc}(t)$ corresponds to an equivalent drain source voltage drop at the dc current level $I_{d,rms,cc}(t)$ for any applied gate voltage.

Fig. 1: Simulated Hefner model in (1) and the iv -characteristic curve extracted from data sheets for 1200 V SiC MOSFET at (a) 25 °C and (b) 150 °C; and moreover, the operation points for achieving constant power losses are indicated by the blue dots.

C. Power Losses Modelling Accuracy

In worth mentioning that, the equivalence or approximate equivalence symbol “ $\approx$ ” is used in (3) because the equivalence becomes valid only if the drain current I_d has a linear relationship with the drain-source voltage V_{ds} . However, this condition does not hold when the operation point approaches to the saturation region.

In addition to that, the body diode shares part of the drain current when the power MOSFET is reverse conducted. As a result, the body diode and MOSFET channel are in parallel, which reduces the effective source-drain voltage V_{sd} . Moreover, this effect is strengthened when the gate voltage turns to a smaller value. Therefore, the approximation error of (3) that defined by

$$\text{error} = \frac{V_{ds,rms,cc}(t) \cdot I_{d,rms,cc}(t) - \langle P_{con,T_L} \rangle(t)}{\langle P_{con,T_L} \rangle(t)} \cdot 100\% \quad (4)$$

shall be evaluated.

Due to the parallel connected MOSFET channel and body diode, the effective source-drain voltage drop V_{sd} at a negative current I_1 can be calculated with

$$V_{sd}(I_1) = \frac{V_F(I_1) \cdot V_{ch}(I_1)}{V_F(I_1) + V_{ch}(I_1)}. \quad (5)$$

The voltage drop due to the MOSFET channel $V_{ch}(I_1)$ is shown in Figure. 2, and can be obtained by finding the inverse function of (1). The forward voltage drop V_F is a function of the diode current and can be described by a 2D look-up table. Therefore, during one load period T_L , the operation points are illustrated in Fig. 2, and in details, following the trajectory $A \rightarrow 0, 0 \rightarrow B, B \rightarrow 0, 0 \rightarrow A$.

By incorporating the body diode, the average power losses $\langle P_{con,T_L} \rangle(t)$ during a full electric period T_L is achieved with

$$\begin{aligned} \langle P_{con,T_L} \rangle(t) &= \frac{1}{T_L} \int_{-\pi/2\omega_e}^{\pi/2\omega_e} V_{ds}(t, \tau) \cdot I_d(t, \tau) d\tau \\ &+ \frac{1}{T_L} \int_{\pi/2\omega_e}^{3\pi/2\omega_e} V_{sd}(t, \tau) \cdot I_d(t, \tau) d\tau. \end{aligned} \quad (6)$$

Fig. 2: Graph illustration of the power MOSFET operation point while conducting a sinusoidal current.

However, no explicit analytical expression can be derived from (6), due to a lost of the symmetry between the 1st and 3rd quadrant of the iv -characteristic curves. Therefore, only the numerical value of the approximation error (i.e., “error” in (4)) can be obtained.

As a result of the body-diode effects, the power losses and the corresponding approximation error are modulation index D , gate voltage V_{gs} , drain current I_d and load angle ϕ_{load} dependent. These dependencies are calculated by using (4), (5) and (6), and the results are illustrated in Fig. 3.

At high speed operation conditions, a small load angle ϕ_{load} and a large modulation index D are expected due to a large back-EMF. It can be observed from Fig. 3 (a), (d), (g) that, the approximation errors (“error” in %) are generally very small at all used gate voltage levels which indicates a high approximation accuracy of (3).

D. Gate Voltage Derivation

By setting the power losses in each load period T_L to a constant value P_{const} , the gate voltage $V_{gs,T_L}(t)$ is then derived by finding the solution of the simultaneous equations consisting of (1) and (3), which is indicated by the intersections in Fig. 1,

Fig. 3: The approximation error (“error” in %) of (3), where the 1st, 2nd and 3rd rows refer to the value of (4) at $V_{gs} = 14V$, $V_{gs} = 16V$, and $V_{gs} = 18V$ respectively; and the 1st, 2nd and 3rd columns refer to the value of (4) at $\phi_{load} = 0$, $\phi_{load} = \pi/4$ and $\phi_{load} = \pi/2$ respectively.

and is found to be

$$V_{gs, T_L}(I_L(t)) =$$

$$\left(\frac{K_{lin}}{K_{sat}} \frac{P_{const}}{I_L(t)} + \frac{I_L(t)^2}{4K_{lin}P_{const}} \right) / \left(1 - \frac{\theta \cdot I_L(t)^2}{4K_{lin}P_{const}} \right) + V_{th},$$

$$\text{while } \frac{I_L(t)}{2} > I_{min}(t), \text{ and } I_{min}(t) = \left[\frac{(K_{lin}P_{const})^2}{2K_{sat}} \right]^{\frac{1}{3}}. \quad (7)$$

It worth mentioning that, an *error* that less than zero indicates underestimated power losses. As a consequence, the gate voltage derived in (7) will actually drive more power

losses than it requires. In order to further enhance the control accuracy, countermeasures such as online junction temperature measurement and feedback control are recommended.

E. Thermal Stability Criteria

By observing Fig. 1, a relatively high drain-source voltage V_{ds} is required while the drain current I_d is low to achieve constant conduction losses. However, operating with low gate voltage can trigger secondary breakdown and thermal runaway, because of the negative temperature coefficient (NTC) property that tends to focalize current and cause local hot spots [14] [15] [16]. Therefore, the gate voltage range should be confined to operate in the positive temperature coefficient (PTC) area, which is illustrated in Fig. 4.

Fig. 4: NTC and PTC operation areas of the 1200 V SiC MOSFET illustrated by the iv -characteristic curve at (a) gate voltage of 12 V and 14 V and (b) gate voltage of 16 V.

The temperature compensation point (TCP) that separates the NTC and PTC area is defined as the thermally stable boundary condition. Gate voltage $V_{gs,TCP}$ at the TCP is derived by setting $dI_d/dT = 0$, which gives

$$\frac{K_{lin}}{2K_{sat}} V_{ds} = (V_{gs,TCP} - V_{th}) - \left[n + \frac{\theta}{1 + \theta \cdot (V_{gs,TCP} - V_{th})} \right]^{-1}, \quad (8)$$

or equivalently

$$V_{gs,TCP}(I_d) = \left(\frac{nI_d}{2K_{sat}} + \frac{1}{n} \right) / \left(1 - \frac{\theta n I_d}{2K_{sat}} \right) + V_{th}, \quad (9)$$

$$\text{with } n = \frac{1}{K_{lin}} \cdot \left| \frac{dK_{lin}}{dT} \right| \cdot \left| \frac{dV_{th}}{dT} \right|^{-1}.$$

To operate in the PTC area, the gate voltage $V_{gs}(t)$ has to be larger than (9), and therefore by combining with (7), it can be synthesized as:

$$V_{gs}(t) = \begin{cases} \text{Max}[V_{gs,T_L}, V_{gs,TCP}], & \text{if } I_L(t) > 2I_{min}(t), \\ V_{gs,TCP}, & \text{if } I_L(t) \leq 2I_{min}(t), \end{cases} \quad (10)$$

III. ELECTRIC DRIVE APPLICATION

This section focus on a validation method by numerical simulations of the dynamic gate voltage control method by first introducing on an equivalent electro-thermal model (ETM) of the power MOSFET. From the ETM, power losses and the corresponding temperature responses are extracted. The validation is carried out in simulation on an electric motor drive system. By applying a series of load current steps, the power losses varies and the corresponding junction temperature T_J changes accordingly at every load step. At last, the obtained results indicate reduced junction temperature swing ΔT_J when implementing the proposed dynamic gate voltage control method.

A. Electro-thermal equivalent circuit model

To verify the proposed gate voltage control method, an electro-thermal model (ETM) of the power MOSFET is built up and illustrated in Fig. 5.

Fig. 5: Equivalent electro-thermal model based on an 1200 V SiC power MOSFET with TO-247 package.

The power switch contains three parasitic nonlinear capacitors C_{gd} , C_{gs} and C_{ds} respectively, which depend on the drain-source voltage V_{ds} due to a change of the corresponding depletion layer boundaries. These dependencies are described by look-up tables. Based on this model, the switching losses and conduction losses are obtained. A third order thermal model is applied for junction temperature estimation, where parameters are obtained from data sheets.

B. System Operation Principle

It can be observed from (7) and (10) that after acquiring $I_L(t)$, the gate voltage control scheme can be easily applied to all power MOSFETs installed in an electric motor drive. The gate voltages for all power switches share the same value due to the same load current profile $I_L(t)$. As a result, the value of the gate voltage only need to be calculated once when load step occurs, which largely simplifies the controller design and alleviates the corresponding computation efforts. The gate voltage control method in an electric motor drive system is then developed, and illustrated in Fig. 6.

Instead of a conventional two-level pulse, this gate driver generates a three-level gate signal as shown in Fig. 6, which starts with a high voltage stage V_h (18 V in this case) for fast switching, thus avoiding extra voltage harmonic distortions on the load side. The voltage V_h is selected to have a reasonably large amplitude depending on the MOSFET type,

Fig. 6: Operation principle of the gate voltage control method in the electric motor drive application.

which enables fast switching within the safe operating area of the device. To accommodate different switching frequencies, the width of the V_h stage can be adjusted and its duration t_h ($1.2 \mu s$ in this case) should be at least longer than the minimum required switching-on time. After the power transistor is fully switched on, the gate voltage level is adjusted according to $V_{gs}(t)$ during the on-state to control the conduction losses.

The operation principle indicates an independent control of each switch by supplying a gate voltage depending on the load current profile $I_L(t)$. Furthermore, its implementation can be readily realized by merely integrating three dynamic gate drivers employed in Fig. 6. Other aspects, such as the power converter topology, the modulation method, and the control scheme (i.e. field-oriented-control in this case) of the electric drive will not be affected.

IV. SIMULATION RESULTS

To obtain the drain-source voltage response to the three-level gate signal, the electro-thermal model (ETM) that presented in Fig. 5 is built up in Matlab Simulink using the Plexim PLECS blockset. It can be observed from Fig. 7 (a) that, with a 10 A output current, V_{ds} is increased from 1.5 V to 2.4 V, when the three-level gate signal changes from 18 V to 13.5 V.

After that, simulations are conducted to evaluate the performance of the proposed gate voltage control method in the electric drive system that shown in Fig. 6. The simulated electric drive system employs a PMSM machine of 10 pole-pairs, a DC-link supply voltage of 400 V, and a switching frequency of 10 kHz.

The load profile employs a 200 Hz three-phase current with its peak amplitude $I_L(t)$ changes in every 0.5 s to emulate the load steps. By observation of Fig. 7 (b), the dynamic gate voltage $V_{gs}(t)$ of switch Cu, as obtained from (10), follows the envelope of the load current $I_{loadC}(t)$ and is always higher than the required level $V_{gs,TCPI}(I_{loadC}(t))$ to operate the switch Cu in the PTC area. After that, the corresponding power losses are extracted from the equivalent circuit model in Fig. 5, which consisting both switching losses and conduction losses. The junction temperature response of switch Cu is then obtained from the connected thermal equivalent circuit.

Simulations with a conventional two-level gate signal under the same load condition are conducted to obtain the junction temperature for reference. Temperature swings ΔT_J at different load transitions are depicted in Fig. 7 (c), and the values are listed in Table II. The results show a reduced

temperature swing by applying the proposed gate voltage control method. Moreover, the compensation effects are load current dependent since sufficient amount of current is required to produce a defined power losses P_{const} . In addition to that, the power losses are slightly increased as expected due to reduced gate voltage, however, the overall system efficiency is merely affected while operating with a high speed operation and thus a high output power (i.e., 4262 W in this case).

V. LIFETIME ESTIMATION

In [17], the LESIT lifetime testing project that covers a standard power module from different suppliers are carried out. The tests were conducted at different average junction temperatures T_{avg} and temperature swings ΔT_J , and the results in [18] indicate a linear relationship between the number of cycles to failure N_f and ΔT_J in the log-log scale. To describe this relationship, an empirical lifetime model is developed as follows:

$$N_f = A_c \cdot \Delta T_J^\alpha \cdot \exp(E_a/k_B T_{J,avg});$$

where

$$\begin{aligned} \text{Activation energy } E_a &= 9.89 \cdot 10^{-20} \text{ J}, \\ \text{Boltzmann-constant } k_B &= 1.38 \cdot 10^{-23} \text{ J} \cdot \text{K}^{-1}, \\ A_c &= 650790, \text{ and } \alpha = -4.67. \end{aligned} \quad (11)$$

The lifetime models presented above are developed based on repetitive identical power cycles. However, in real applications, the thermal stress profile generally consists irregular cycles featuring different T_{avg} and ΔT_J . In order to estimate the lifetime of power semiconductors under such a condition, the linear damage accumulation (LDA) principle shall be applied [19]. If the same failure mechanism is shared within a full thermal stress profile, all stress levels can be added up to calculate the total accumulated damage (AD) as:

$$AD = \sum_{i=1}^k \frac{n_i}{N_{fi}} = \frac{n_1}{N_{f1}} + \frac{n_2}{N_{f2}} + \frac{n_3}{N_{f3}} \cdots + \frac{n_k}{N_{fk}}. \quad (12)$$

Where N_{fi} represents the number of cycles to failure at a specific stress ΔT_{Ji} , and n_i is the number of cycles accumulated at this stress level. The end of life (ED) can be expected when the inverse of AD reaches one. The inverse of AD is the expected repetition rate N_r of the considered thermal stress profile, which is expressed as $N_r = 1/AD$.

It can be deduced that, the lifetime is fully consumed by a single run of this stress profile when AD equals to one. For a AD larger than 1, the repetition rate N_r becomes less than 1, and the power semiconductor will thereby not last for a single

Fig. 7: (a) Response of V_{ds} to the three-level gate signal, (b) Gate voltage profile and three-phase load current, and (c) Junction temperature response.

TABLE II: Performance evaluation at a high speed operation with 10kHz switching frequency.

	ΔT_{J1} J_{avg1} (K) 30→20 (A)	ΔT_{J2} J_{avg2} (K) 30→15 (A)	ΔT_{J3} J_{avg3} (K) 30→10 (A)	P_{losses} /Switch(W)	P_{out} (W)	η (%)	N_r
$V_{gs}(t) = 18V$	34.9, 337.4	45.4, 332.2	51.4, 329.2	24.4	4262	98.3	$9.67 \cdot 10^6$
$V_{gs}(t)$ in (10)	21.4, 344.2	37.4, 336.2	49.2, 330.3	27.4	4262	98.1	$1.48 \cdot 10^7$

run. When AD is less than 1, this stress profile can be repeated for N_r times. Based on this method, the repetition rate N_r is calculated according to the data in Table II, where the result suggests a lifetime improvement of 53.0%.

VI. EXPERIMENTAL VERIFICATION

For experimental verification, a proof-of-concept for a three-level gate driver is shown in Fig. 8 (a). It is operated by first activating the turn-on FET to produce a high voltage stage (18V for 1.2μs in this case) to maintain a fast switching transient. After that, the power op-amp is enabled to adjust the gate voltage according to $V_{gs}(t)$ to achieve constant conduction losses. The turn-off FET is triggered at last for switching the power transistor off.

A saturation detection scheme is developed, which monitors the on-state drain-source voltage drop to ensure a safe operation of the power MOSFET. The associated protection circuit compares the drain-source voltage with two different voltage levels. When V_{ds} is higher than the low level, the gate voltage will be switched back to +18V to avoid saturation, such that no hard stops would occur during the power cycling test. However, when short circuit occurs, the power MOSFET will be switched off by Soff immediately.

To conduct the power cycling test, a 3kW electric drive in Fig. 8 (b) is built up. As can be seen from Fig. 8(c), the drain-source voltage V_{ds} increases by reducing the gate voltage from 18V to 13V. As a temperature sensitive electric parameter, a look-up table of the on-state resistance R_{on} measured under 18V gate voltage is used for the junction temperature estimation. In order to acquire this R_{on} , a periodical two-level 18V gate trigger signal that illustrated in Fig. 8(c) is produced for every 1ms to measure the on-state voltage $V_{ds,on}$ by a clamping circuit. After that, the electric motor drive is loaded with a 50Hz three-phase current with a load profile as

depicted in Fig. 8(e) for power cycling. Junction temperatures are estimated, which shows reduction of the temperature swing by applying the proposed method.

CONCLUSION

In this paper, a model based dynamic gate voltage control method is proposed to reduce the thermal stress of power MOSFET. After that, thermal stability criterions are introduced to prevent current focalization and local heat up. This method is verified by a dynamic gate driver that supplies an adjustable gate voltage. At last, thermal cycling tests are conducted on a three-phase electric motor drive and the results show reduction of the junction temperature swing, which confirms the thermal control method.

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Fig. 8: (a) Three-level dynamic gate driver schematics, (b) Three-phase electric motor drive setup, (c) The V_{ds} response of the 10kHz three-level gate signal, (d) Look-up table for junction temperature T_j estimation, and (e) Temperature profile during power cycling test.

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