Design & Real-Time Field Implementation of Micro-Inverter for Rural Applications

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Design & Real-Time Field Implementation of Micro-Inverter for Rural Applications

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Abstract— Need for comprehensive development of photovoltaic (PV) based micro-inverter interface for various rural applications is observed. This paper demonstrates the design, development, and real-time field experimentation of an energy-efficient, PV based single-phase micro-inverter for rural/remote applications. The proposed dual-stage single-phase inverter takes the advantage of interleaved DC/DC boost converter for cancellation of 180° phase-shifted harmonics and application of voltage doubler circuit results in a reduction of the transformer turns ratio with low flux leakage and thus endeavoring for better conversion efficiency at a reduced size of magnetics. Further, high-frequency switching at the first leg and low switching frequency at another leg of the full-bridge converter ensures lower switching losses at light load conditions. Experimental results are carried out at field location (latitude: 26.431°, longitude: 74.707°) in Rajasthan, India. The interleaved boost DC/DC converter efficiency is found approximately 91.73% at full load and 77.74% at 10% load. Micro-inverter overall efficiency is observed in between 57.34% to 91.6%.

Keywords— *Interleaved DC-DC converter, Photovoltaic (PV), micro-inverter, rural electrification.*

I. INTRODUCTION

Rural electrification along with the need of supplying continuous, clean, and quality electricity supply is still a major concern of developing Nations. Approximately, 940 million people across the World do not have any access to electricity [1]. Further, it is difficult to quantify the availability of electricity in rural areas based on hours per day. The photovoltaic (PV) market has emerged as a promising option for rural electrification [2], [3]. Micro-inverters have received the attention of researchers, industrialists, and users due to their several techno-economical benefits [4] such as able to extract maximum power even under mismatching conditions, increased reliability, ease of use and maintenance, plug and play approach [5]. Various types of single-phase micro-inverter configurations can be referred to in [6] - [10].

Single-phase micro-inverters with high frequency (HF) ac-link architectures may be divided into two subcategories. First are the micro-inverters with phase-modulated dc-dc converter topologies presented in [11]. The series resonant dc-ac dual active bridge converter represents the second category [12], [13]. It uses HF resonant inverter to obtain HF current waveform with its amplitude modulated at line frequency. Further, as the next stage, a full-bridge or half-bridge converter is then utilized to obtain the desired line frequency output. A single-stage, isolated, PV micro-inverter with single-phase DC/AC topology is presented in [14]. The proposed configuration in [14] works on the dual-active-bridge principle and have two full-bridge cells with floating DC bus capacitors. Further, an interleaved flyback converter-

based PV micro-inverter suitable for remote areas is discussed in [15]. It consists of a flyback transformer for isolation purpose and uses a full-bridge inverter to supply power at the desired frequency and AC voltage. Single-phase micro-inverters suffer from the issue of pulsations on the DC bus and therefore need a large capacitor across the DC bus [16]. Authors in [17], proposed a pulse-width modulation based single-phase micro-inverter to mitigate the need for large, bulky electrolytic capacitors at the DC bus.

This work presents a low cost, dual-stage, isolated, PV based single-phase micro-inverter with interleaved DC/DC boost topology, suitable for low power applications in rural/remote regions. The design aims to develop compact size, low cost, energy-efficient PV based single-phase inverter. The proposed dual-stage single-phase inverter takes the advantage of interleaved DC/DC boost converter for cancellation of 180° phase-shifted harmonics and application of doubling voltage circuits results in a reduction of the transformer turns ratio with low flux leakage and thus endeavoring for better conversion efficiency at a reduced size of magnetics. Further, HF switching at the first leg and low switching frequency at another leg of the full-bridge converter ensure that switching losses are minimized at light load.

This paper is structured as follows: description of the proposed PV micro-inverter is presented in section II. Design and calculation are included in section III. Section IV presents real-time experimental results. Summary of the carried work along with future work direction is shared in section V.

II. PROPOSED MICRO-INVERTER DESCRIPTION

The schematic of the proposed single-phase micro-inverter for rural application is presented in Fig. 1. The micro-inverter configuration has three main stages: (i) interleaved boost DC/DC converter with doubler circuit; (ii) HF transformer; (iii) high switching frequency and low switching frequency leg- power converter. It relates two-phase interleaved HF switching with 180° phase shift for reduced harmonics with isolation transformer for boosting the voltage from DC bus voltage to approximately 290-356V through rectifying diode and capacitor bridge-based voltage doublers topology as pre-stage input DC bus for micro-inverter. To reduce switching noise, the power bridge using one HF leg (15-20 kHz) with blocking diodes and the second leg at normal supply frequency (50 Hz) are planned. The specifications of the micro-inverter are given in Table I.

III. DESIGN OF SINGLE-PHASE MICRO-INVERTER

For a micro-inverter working at 230V AC 50 Hz, an initial DC boost stage with maximum power point tracking (MPPT); accommodating fast varying PV voltage along with

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A. Design of Interleaved Boost DC-DC Converter as a Boost Stage of Micro-Inverter

The main specifications for design and calculations are projected in Table II; both DC bus as well as PV panels are of the same rating except that nominal working voltages are 24 and 30 V for both cases respectively. It is therefore considered as PV based or DC bus based micro-inverter system further.

Table II DC-DC boost converter stage specifications for micro-inverter (230V 1- ϕ AC 50 Hz)

Parameter	Projected design (DC bus)	Projected design (PV)
Power (W)	250	250
Input voltage rating (V)	24	30
Input voltage range (V)	(18-30)	18-36
Output voltage (V)	324	324
Output DC voltage range (V)	290-356	290-356
Projected efficiency	>97%	>97%
Switching frequency	30 kHz	30 kHz

Interleaving topology makes use of multiple leg combinations with switching at a phase difference of 360°/n and helps in canceling harmonic ripples and breaking a large inductor into small size inductors; thus, helping in size and weight reduction. The second advantage is almost equal sharing of load current at the primary stage. A minor unequal magnitude difference could be absorbed by MOSFET safe operational area. Referring to Fig. 2, considering all variables with smaller values, the output voltage in continuous conduction mode (CCM) is expressed in (1):

$$V_o = \frac{(V_{in} - I_{ind} \times R_{ind})}{(1-D)} - V_d - V_{ds} \times \frac{D}{1-D} \quad (1)$$

As a voltage doubler diode capacitor bridge is planned to reduce the transformer ratio for reducing flux leakage. The duty cycle may be defined as:

$$V_o = 2 * V_{in} \frac{1}{(1-D)} \quad (2)$$

Ascertaining duty cycle more than 50%, knowing the values of specified input and output voltages the duty cycle value D is chosen as 0.65-0.7.

The transformer ratio is calculated as:

$$N = \frac{V_o(1-D)}{2 * V_{in}} = 2.36 \quad (3)$$

The transformer may be chosen as 2.5 for a wide duty cycle.

The input power based on projected efficiency as (4):

$$P_{in} = \frac{P_{out}}{\eta} = \frac{250}{0.97} = 257.7 \text{ W} \quad (4)$$

For supplying full load power, the input maximum current can be found as per (5):

$$I_{ind_max} = \frac{P_{in}}{V_{in_max}} = \frac{257.7}{18} = 14.32 \text{ A} \quad (5)$$

$$I_{ind_rms_max} = \sqrt{\frac{2-D}{2}} I_{in_max} = \sqrt{\frac{2-0.65}{2}} * 14.32 = 6.01 \text{ A} \quad (6)$$

The average current of a switching cycle in the inductor may be written as in (7):

$$I_{ind_average} * \frac{T_{off}}{T_s} = I_{ind_average} * (1-D) = I_o \quad (7)$$

The maximum output current may be calculated as (8):

$$I_{o_max} = \frac{P}{V_{min}} = \frac{250}{290} = 0.86 \text{ A} \quad (8)$$

For ensuring CCM mode, the minimum load limit is taken as 10% and therefore minimum power transfer is given by (9) and limiting load current that should be governed by (10).

$$P_{limit} = 10\% * P = 0.1 * 250 = 25 \text{ W} \quad (9)$$

$$I_{limit} = \frac{1}{2} * \frac{P_{limit}}{V_{in_max}} = \frac{1}{2} * \frac{25}{30} = 0.41 \text{ A} \quad (10)$$

The inductor ripple should be limited to I_{limit} for CCM mode operation, therefore:

$$\Delta I_{ind} = I_{limit} = 0.41 \text{ A} \quad (11)$$

Therefore, inductor value can be calculated as (12):

$$L = \frac{V_{in_min} * D}{\Delta I_{ind} * f_{min}} = \frac{18 * 0.65}{0.41 * 30000} = 951 \mu\text{H} \quad (12)$$

The diode current equivalent to I_{rms} value is given by (13):

$$I_D = \sqrt{2-D} * \frac{I_{in_max}}{2 * N} = \sqrt{2-0.65} * \frac{14.32}{2 * 2.5} = 3.32 \text{ A} \quad (13)$$

The switching period is given by (14):

$$C_o \geq \frac{I_o * D * T_s}{\Delta V_{max}} = \frac{0.86 * 0.65 * 33.33 * 10^{-6}}{0.2 * 324} = 28.46 \mu\text{F} \quad (14)$$

The capacitor ripples can be calculated as per (15):

$$\Delta I_{cap} = \frac{I_{ind_max}}{2 * N} = \frac{14.32}{2 * 2.5} = 2.86 \text{ A} \quad (15)$$

The inductor power losses are calculated knowing average inductor current, winding resistance, and core losses data (manufacturer's datasheet) as per (16):

$$P_{ind} = \left(\frac{I_o}{1-D} \right)^2 R_{ind} + P_{core} \quad (16)$$

Based on the above calculations, the selected components for the interleaved DC-DC boost converter are given in Table III.

Table III List of selected boost DC-DC converter components as a part of the micro-inverter

Main components	Broad specification
Boost inductor coils	Ferrite core inductor (mH)
C _o at common DC bus	1000 V capacity in μF
Microcontroller	μC ATmega 328/2560
PWM IC	MCPI631HV
MOSFET, BSC320N20N53G	$V_{DS} = 200\text{V}$, $I_D = 36\text{A}$, $R_{D_ON} = 32\text{m}\Omega$, $g = 22\text{nC}$, $P_D = 125\text{W}$, $R_{TH} = 0.65 \text{ W}$
Diode schottky 1DH20G120C5	$V_{RRM} = 1200\text{V}$, $I_F = 20\text{A}$, $V_{F_MAX} = 1.5\text{V}$, $P_{TOT} = 330\text{W}$, $dv/dt = 80\text{V/ns}$
Low gate driver IED44176N01F	25V, 0.8A, $I_{SINK} = 1.75\text{A}$, $I_{SOURCE} = 0.8\text{A}$, Turn on/off time=50 nsec Enable & overcurrent protection

B. High-Frequency Transformer Design as the Next Stage of DC-DC Boost Converter

The projected design specification of the HF transformer is tabulated in Table IV.

Table IV Projected design specification of HF Transformer

Parameter	Value
VA capacity	258 VA
Turn ratio	2.5
Switching frequency	30 kHz
Input voltage	24 V
Input current RMS	1.597 A
Output voltage	230V AC
Output current	1.12 A
Projected efficiency	98%
Duty cycle	65-70%
Projected temperature rise	30 °C

The output power of the transformer can be derived as (17):

$$P_{txr} = \frac{P_{in_txr}}{\eta_{txr}} = \frac{250}{0.97} = 257.7 \text{ W} \quad (17)$$

To achieve maximum inductance and winding area at a reduced cost, volume, and weight; the design search for the shape of ferrite core is significant in commanding flux path, leakage, thermal heat dissipation without hot spots, and core losses. In EI core when the center leg shape is taken round like that of pot cores, the radius of the winding wire is shorter, smooth in laying; resulting in reduced bending stress with better airflow aces and flux linkages; thus achieving overall reduced winding losses and contributing higher efficiency about 8-11% more as compared to a square shape central.

The core loss is the energy difference between received and delivered energy to load and the lost part is decided by core properties. The energy stored in the core over one switching period is governed by (18):

$$E_T = \int_0^T V(t) \times i(t) dt \quad (18)$$

As per Faraday's law:

$$V(t) = n \times \frac{d\phi}{dt} \quad (19)$$

Further, (19) may be rewritten as (20):

$$V(t) = n \times A_c \frac{dB}{dt} \quad (20)$$

As per Ampere's law (21) may be expressed as:

$$\frac{dH(t)}{dt} = \frac{n}{l_{core}} \frac{di(t)}{dt} \text{ or } di(t) = \frac{l_{core}}{n} dH(t) \quad (21)$$

Substituting v(t) and i(t) in (18) using (20) and (21), it may be written as (22):

$$E_T = l_{core} \times A_c \int_0^T dB \times dH(t) \quad (22)$$

Thus, the total energy is consumed by the volume of core multiplied by the area of the BH loop formed during one switching period with switching on (forward) and switching off time (reverse return with different tracing paths).

Based on $W_a * A_c$ the value which is governed as (23) and corresponding magnetic data published by manufactures:

$$W_a * A_c = \frac{P_o \times D_{cma}}{K_t \times \Delta B \times f} = 3.07143 \text{ cm}^4 \quad (23)$$

where W_a is window area of core shape in cm^2 ; A_c is effective cross-sectional area of core in cm^2 ; P_{max} is maximum power (W); K_t is a constant which is based on the topology of use (dimensionless); ΔB is maximum flux density in Gauss. The value of flux density B (1500 Gauss) is chosen from data given by the manufacturer as per frequency –flux plots and the chosen figure is at 30 kHz for a general-purpose ferrite. The core loss increases after the operational frequency is increased above 20 kHz. f is switching frequency (Hz); D_{cma} is current density in circle.mils area/A.

The known topology constants are summarised in Table V for design calculation.

Table V Summary of topology constants used in inductor/transformer designs

Topology	K_t constant
Half-bridge	0.0014
Full bridge	0.0014
Push-pull	0.001
Forward converter	0.0005
Flyback	0.00033

Table VI Possible core shapes, size, and power handling capacity at 30 kHz operation

Power (W)	Toroid shape	EI core	ETD
260	43813 TC	-	-
280	-	44020EE	44216 EER
300	43615TC	-	44444 ETD

Table VII Magnetic properties of magnetic cores under design consideration for HF transformer

Power (W)	Core type	$W_a A_c$ (cm^4)	l_e cm	A_e cm^2	V_e cm^3	MLT (m)	Size LxWxH
260	43813 TC	3.28	82.9	115.6	9652	57	38x19x13
280	00K44020EE	3.55	97	178	17300	91	43x21x15
	KoolMμ						
	44216 EER	2.98	98.7	175	17300	102	42x21x16
300	00K43615TC	3.98	89.6	95.9	8396	48	36x23x15
	KoolMμ						ODxIDxH
	44444 ETD	3.68	103	173	17800	104	45x22x15

The parameters for 280 W with EE core shape at s. no. 2 shows an optimized design choice while toroid at s. no. 3 is safer in performance and possibility of saturation at higher temperature and light in weight. The third EE core with the round shape at the center at s. no. 3 may accommodate winding with a low fill factor. The next point is cost and ease of availability. The material for all the above cases is R type of material.

The next step is to find a primary number of turns using (24):

$$N_p = \frac{V_p \times 10^8 \times D_{max}}{4 \times B \times A_c \times f} \quad (24)$$

$$N_p = \frac{24 \times 10^8 \times 0.65}{4 \times 1500 \times 95.9 \times 10^{-2} \times 30000} = 9.04 \text{ say } 10 \text{ Turns}$$

$$N_s = N \times N_p = 2.5 \times 10 = 25 \text{ Turns} \quad (25)$$

Considering skin effect the current penetration depth may be worked out as per (26):

$$\delta = \frac{66.2}{\sqrt{f}} = \frac{66.2}{\sqrt{30000}} = 0.3822 \text{ mm} \quad (26)$$

The maximum wire diameter to avoid skin effect is given by:

$$d = 2\delta = 0.76 \text{ mm} \quad (27)$$

The eddy currents penetration depends upon frequency, the conductivity of the wire, and permeability of the core. The depth at which eddy current is decreased to $1/e$ or about 37% of surface density is called standard depth; which is decreased due to a higher frequency, conductivity, and permeability. Assuming the current density as 5.0 A/mm^2 the primary wire area works out to be $14.5 \text{ A}/5 = 2.9 \text{ mm}^2$ and the wire diameter as 1.92 mm. The primary side wire gauge is 13 AWG with 2.84 mm^2 and the resistance value is 0.00656Ω per meter of length. Similarly, secondary wire cross-section area as 0.172 mm^2 and diameter as 0.46 mm is calculated. It corresponds to 24 gauge with 0.25 mm^2 cross-sectional area, current carrying capacity of 1.02 A, and the resistance value of 0.08422Ω per meter.

IV. REAL-TIME FIELD HARDWARE RESULTS & ANALYSIS

Based on the proposed design and prototype development of the micro-inverter system as per Fig. 1&2, the experimental work conducted in the field at site location coordinates as latitude 26.431° , longitude 74.707° ; the primary data-based findings are discussed in this section.

The data related to PV energy generation with MPPT, its consumption in local load, and battery energy storage (BES) charging during various timings of the day are tabulated in Table VIII, below. Further as shown in Fig. 3 under normal load conditions the micro-inverter output is a pure sine wave; free from harmonics and the DC bus is also stable. Fig. 4 is the record of the BES charging under deep discharge condition in a controlled PWM duty cycle based on its internal resistance.

Fig. 3 DC bus voltage and micro-inverter output 230 AC 50 Hz

Fig. 4 BES burst charging at its deep discharge case from DC bus

A typical BES charging pattern as leveling and streamlining the charging process is shown in Fig. 5. DC bus under dc load is stable, free from ripples without switching transients as shown in Fig. 6. The power part of the micro-inverter as shown in Fig. 1; is tested in two parts; the first being interleaved DC-DC converter with an HF transformer with a capacitive rectifying bridge (doublers) for boosting the dc voltage as pre-stage of inverter and the other is inverter bridge switching with one leg at HF and the second at 50 Hz frequency at 180° phase shift or load as the case is opted for.

The design has been worked out using high permeability ferrite core for reduced core losses at 30 kHz which is safe without using complex circuit and PCB layout trials for reduced EMI and switching losses. It is clarified that MOSFET losses are calculated based on design and core losses are based on simulation and recommendation of the manufacturer [18].

Fig. 5 BES float charging after 80% SOC by DC bus

Fig. 6 Showing stability of DC bus at load like a soft load

Table VIII Power flow status at DC bus

Time (Hr.)	Irr. w/m ²	Total generated PV power (W)	Active DC load (W)	BES load (W)	Total local load (W)	Local load (%)	Micro-inverter power (W)
6	25	16.33	16.0	0	16	97.97	0.33
7	131	83.89	16.0	38.	54	64.37	29.89
8	274	177.58	16.0	97.5	113.5	63.91	64.08
9	349	224.42	21.0	97.5	118.5	52.80	105.92
10	446	291.24	47.0	97.5	144.5	93.75	146.74
11	581	375.13	47.0	97.5	144.5	73.46	33.93
12	683	440.20	24.0	97.5	121.5	52.90	89.05
13	730	453.87	47.0	97.5	144.5	58.78	80.17
14	648	418.64	47.0	97.5	144.5	65.59	53.84
15	513	333.81	24.0	97.5	121.5	69.27	36.91
16	392	251.63	21.0	97.5	118.5	47.09	2.16
17	201	131.84	16.0	97.5	113.5	86.08	18.34
18	37	23.70	16.0	0	16	67.51	7.7
Total		3222.28	358.0	1013	1371	69.06	669.06

A. DC-DC Boost Converter Stage

The system is energized keeping switching frequency at 30 kHz using opto-isolated gate drivers, though the placement of MOSFET in the circuit is at the lower end just near to the common ground to avoid gate triggering complexity. As the input power source is stabilized (Fig. 3) being DC bus or BES there is smooth CCM operation at reduced harmonics in addition to taking advantage of interleaved switching with 180° phase shift and mitigating switching harmonics. It also helps in reducing the output capacitor rating. The test data are being tabulated in Table IX.

Table IX Interleaved boost DC-DC converter as pre-stage of the micro-inverter at 30 kHz

Load %	Input load Amp (A)	Coppe loss (W)	Core loss (W)	MOSFET loss (W) at 30 kHz	Total loss (W)	Vout at boost stage (W)	I _o (A)	P _{out} (W)	Eff. of inter-leaved boost conv. (%)
100	10.23	2.36	13.5	8.63	24.5	321	0.78	250.4	91.73
80	8.20	1.45	13.5	5.77	20.72	322	0.62	200.9	90.72
60	6.15	0.83	12.3	3.41	16.54	321	0.47	150.2	90.13
40	4.10	0.44	12.5	1.70	14.64	324	0.32	101.1	87.45
20	2.05	0.09	13.5	0.55	7.15	324	0.16	50.6	96.90
10	1.02	0.02	14.2	0.20	7.15	324	0.08	25.2	77.74

An efficiency variation at different load duty cycles is shown in Fig. 7 where it is observed that the efficiency is approximately 91.73% at full load and 77.74% at 10% load. The core losses are relatively low as the magnetic flux is largely confined to the core and leakage is limited as the transformer turn ratio is kept at a minimum at the design stage

by using a rectifier bridge with voltage doubler capacitors in one arm. MOSFET conducting losses are minimized by taking the low value of junction conductance.

Fig. 7 Efficiency variation of interleaved boost converter as pre-stage of the micro-inverter at different load duty cycle at switching frequency 30 kHz

B. Determination of Micro-inverter Efficiency

As described in Fig. 1 the power being generated from PV panels as the basic source and with due MPPT implementation the power is optimized and stabilized at DC bus. In the test exercise, the PV power is regarded as input power, and subsequent copper and core losses along with MOSFET losses including conduction and switching are found. The switching frequency is being kept in between 15 to 20 kHz and found the results at 17 kHz switching of one leg of the inverter bridge without observation of resonance.

A full day performance graph of the proposed single-phase micro-inverter is presented in Fig. 8, where it is clear that efficiency is lower below the rated load.

Fig. 8 Hourly efficiency performance of proposed micro-inverter

V. CONCLUSION

In this paper, a PV based single-phase micro-inverter for rural/remote area applications is proposed. The two-stage interleaved inductors with HF transformer followed by rectification with the capacitive doubler voltage circuit is considered as a boosting stage is proposed. The boost stage includes interleaving inductors switching at HF canceling 180° phase-shifted harmonics by gate drivers at duty cycle > 0.5. The advantage of doubling voltage circuits is to reduce the transformer turns ratio with low flux leakage and thus endeavoring for better conversion efficiency at a reduced size of magnetics. The second strategy is making use of HF switching at first leg and low switching frequency so, that switching losses are minimized at light load. The interleaved boost DC/DC converter efficiency is approximately 91.73%

at full load and 77.74% at 10% load. Further, micro-inverter overall efficiency for a day is observed in between 57.34% to 91.6%. A more detailed analysis of performance and recommendations for improvement of this solar micro-inverter will be included in a future paper.

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