A gravure-printed organic TFT technology for active-matrix addressing applications

Citation for published version (APA):

Fattori, M., Fijn, J., Harpe, P., Charbonneau, M., Lombard, S., Romanjek, K., Locatelli, D., Tournon, L., Laugier, C., & Cantatore, E. (2019). A gravure-printed organic TFT technology for active-matrix addressing applications. *IEEE Electron Device Letters*, 40(10), 1682-1685. [8822469]. <https://doi.org/10.1109/LED.2019.2938852>

DOI:

[10.1109/LED.2019.2938852](https://doi.org/10.1109/LED.2019.2938852)

Document status and date:

Published: 01/10/2019

Document Version:

Author's version before peer-review

Please check the document version of this publication:

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
- The final author version and the galley proof are versions of the publication after peer review.
- The final published version features the final layout of the paper including the volume, issue and page numbers.

[Link to publication](#)

General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal.

If the publication is distributed under the terms of Article 25fa of the Dutch Copyright Act, indicated by the "Taverne" license above, please follow below link for the End User Agreement:

www.tue.nl/taverne

Take down policy

If you believe that this document breaches copyright please contact us at:

openaccess@tue.nl

providing details and we will investigate your claim.

A gravure-printed organic TFT technology for active-matrix addressing applications

Marco Fattori, Joost Fijn, Pieter Harpe, Micael Charbonneau, Stephanie Lombard, Krunoslav Romanjek, Denis Locatelli, Laurent Tournon, Christelle Laugier and Eugenio Cantatore, *Fellow, IEEE*

Abstract — In this work is presented a gravure-printed unipolar Organic Thin-Film Transistor (OTFT) technology able to achieve state-of-the-art yield performance. A multilayer cross-linked dielectric is printed to reduce gate-leakage defects, which have been found to be one of the main failure mechanisms in previous printed OTFTs. The defectivity analysis performed at transistor level reveals 99.8% defect-free devices in a sample of 540 OTFTs, manufactured on 6 successive foils. A novel row driver circuit for matrix-addressing applications has been designed and fabricated using the improved technology. The experimental characterization of the proposed 8-stage row drivers reveals a circuit yield as high as 100%, over 15 samples in 5 successive foils, corresponding to a total number of 2085 fully functional OTFTs. The availability of a printed organic technology compatible with mass production is expected to enable innovative Internet of Things (IoT) applications characterized by extremely low production cost.

Index Terms — Printed electronics, yield performance, flexible electronics, OTFTs, organic row drivers.

I. INTRODUCTION

RECENT advances in Printed Electronics (PE) have brought the attention to organic transistor technologies as a potential candidate for the mass production of inexpensive single-use devices. This could complement the mainstream silicon technology to enable innovative Internet of Things (IoT) products. Printed OTFT technologies compatible with low-cost mass-production have been recently demonstrated [1]-[4]. Nevertheless, several challenges such as modest yield performance, large parameter variability, bias stress, limited shelf life and environment instability still need to be addressed before printed organic transistors can be broadly used in commercial products. In this perspective, this work aims at identifying the major source of defectivity in a specific gravure-printed organic p-type technology [4], and at providing technological solutions to improve its yield. In order to further assess the potentiality of the improved technology, an organic row driver exploiting a novel architecture has been designed, manufactured and characterized. Row drivers are typically

demanding in terms of circuit complexity, requiring large area and a large number of OTFTs. Besides, printed driving circuits are extremely relevant from the application point of view, as they enable electronic backplanes for active-matrix solutions such as displays [5]-[6] and sensing surfaces [7]-[8]. The active-matrix addressing scheme makes it possible to minimize the number of interconnections with the external readout electronics, reducing the production costs of the full system. The current state-of-the-art provides only a few examples of row driver circuits manufactured with p-type [9]-[10] and complementary [11]-[12] organic technologies, mainly produced with photo-lithography processes. To the best of the author's knowledge, this work demonstrates for the first time multi-stage row drivers fabricated with a printed unipolar organic technology.

The paper is further organized as follows: the technology solutions used to improve yield are discussed in section II; the design of the row driver circuit and its measurement results are presented in section III and IV, respectively; and conclusions are drawn in section V.

II. ADVANCES IN THE DIELECTRIC PRINTING CAPABILITY

Progress in organic electronic materials and their improved processing, have recently enabled the development of high-performance printed organic transistors. The MERCK Lisicon® solution-based SP500 organic semiconductor exhibiting carrier mobility of 2.2 cm²/Vs together with the D320 Low-k Dielectric ($\epsilon_r=2.2$), has been optimized to fabricate gravure printed OTFTs with reproducible electrical performance, on a Pilot Line using a GEN1 sheet-based process [4]. The evaluation of the device yield performance in the proposed technology [4], highlighted high defectivity due to excessive gate leakage. This issue is typically severe in printed Top Gate device configurations, where the gate dielectric needs to provide a good interface quality with the underlying organic semiconductor (OSC) as well as chemical and mechanical resistance to the subsequent printing of the gate electrode. In order to improve the robustness of the dielectric-gate stack, and thus the overall yield performance, a dielectric printing based on a multilayer approach has been investigated. Individual 300 nm thick layers

Submitted for review on 17th June 2019. This work was supported by the European Commission (ATLASS project, Horizon 2020, Nanotechnologies, Advanced Material and Production theme, contract n°636130). The authors would like to thank A. Morley and G. Lloyd from MERCK, for their support.

M. Fattori, J. Fijn, P. Harpe and E. Cantatore are with the Eindhoven University of Technology, Eindhoven, The Netherlands

(e-mails: M.Fattori@tue.nl, J.A.Fijn@tue.nl, P.J.A.Harpe@tue.nl, E.Cantatore@tue.nl). M. Charbonneau, D. Locatelli, S. Lombard, K. Romanjek, L. Tournon and Christelle Laugier are with CEA-LITEN, Grenoble, France (e-mail: Micael.Charbonneau@cea.fr, Stephanie.Lombard@cea.fr, KrunoslavRomanjek@cea.fr, Denis.Locatelli@cea.fr, Laurent.Tournon@cea.fr, Christelle.Laugier@cea.fr).

Fig. 1: OTFTs yield analysis performed over 3 sets of OTFTs featuring increasing semiconductor areas S1 (100 OTFTs), S2 (200 OTFTs), S3 (200 OTFTs) and manufactured with different layer stack configurations. (a) 2-layer stack with D320 dielectric, $C_i \sim 3.2$ nF/cm². (b) 3-layer stack with D320 dielectric, $C_i \sim 2.2$ nF/cm². (c) 2-layer stack with hybrid dielectric D320-AP48, $C_i \sim 3.4$ nF/cm². (d) 3-layer stack with hybrid dielectric D320-AP48-AP48, $C_i \sim 2.3$ nF/cm².

have been stacked in different ways, as shown in Fig. 1. For each configuration, the yield has been evaluated over a population of 500 OTFTs featuring increasing semiconductor areas ($S1=0.07$ mm², $S2=0.36$ mm², and $S3=1.26$ mm²). In this study, an OTFT is considered faulty if its gate leakage current is > 1 nA. Despite the two-layer approach, when using the dielectric D320 (Fig. 1(a)), the yield reaches 100% only in the smallest transistors (S1) and rapidly decreases as the semiconductor area increases. The introduction of a third D320 low-k dielectric layer Fig. 1(b) reduces the defectivity but still does not achieve 100% yield (the percentage of defective OTFTs is 10% for the S3 population). A further increase of the dielectric thickness would be detrimental for device performance, leading to larger threshold voltages and stronger short-channel effects. In order to mitigate the sensitivity of the devices to gate-leakage defects, without further increasing the overall dielectric thickness, the second D320 low-k dielectric layer has been replaced with a cross-linked polymer, which provides much better mechanical robustness than the D320 and protects the OTFT stack from damage due to printing of the gate layer. This hybrid dielectric configuration is shown in Fig. 1(c). The cross-linkable dielectric polymer (AP48 Lisicon® with dielectric constant $\epsilon_r=2.5$) is also gravure-printed with a target thickness in the range of 300 nm and crosslinked by UV irradiation at a wavelength of 365 nm, with a dose of 2 J/cm². The hardness of both dielectric layers has been preliminary evaluated with pencil tests [13]: printed D320 layers start to

damage already with HB pencil and fully tear with an H grade. Printed AP48 layers instead exhibit damages only at 3H level, thus providing much better hardness than the D320 dielectric. The comparison between the results reported in Fig. 1(a) and (c), clearly highlights the benefits of this approach to reduce gate leakage. Finally, in order to maximize the device yield, a 3-layer stack configuration has been eventually used in combination with the hybrid dielectric approach (Fig. 1(d)).

The technology yield has been further quantified using a population of 540 OTFTs featuring S3 OSC area, distributed over 6 successive foils. All measured transfer characteristics and gate leakage currents are presented in Fig. 2. The yield analysis reveals that all OTFTs are functional, with only one device exceeding the leakage current threshold of 1 nA, leading to a 99.8% yield. The mobility of the OTFTs manufactured with the modified D320-AP48-AP48 stack is typically 1.9 cm²/Vs. A statistical analysis of their I_{ON} current (performed using the same dataset of Fig. 2), is further reported in Table I. The I_{ON} current values are here extracted at $V_{DS}=V_{GS}=-20$ V.

TABLE I
 I_{ON} CURRENT STATISTICAL ANALYSIS

I_{ON} current statistics	Channel length L [μm]							
	10	20	40	60	80	100	200	400
Mean [μA]	44.6	22.5	11.5	7.8	5.8	4.7	2.4	1.2
St. Dev. [μA]	6.76	3.00	1.06	0.59	0.52	0.34	0.18	0.09
St. Dev./Mean [%]	15.2	13.3	9.2	7.6	9.0	7.2	7.5	12.5

III. 8-STAGE ORGANIC ROW DRIVER DESIGN

The proposed 8-stage row drivers have been designed, simulated and laid out exploiting the Process Design Kit developed in [14]. The circuit architecture (Fig. 3(a)) is based on the cascade of dynamic delay cells (DyCs). This approach offers several advantages in terms of circuit complexity, power consumption, integration density and area occupation. Dynamic logic typically allows more compact implementations compared to static and pass-gate/transmission-gate logics (PTLs) [15], requiring a reduced number of OTFTs and minimizing power consumption. Indeed, the latter in logic circuits based on unipolar inverters is typically dominated by the DC leakage, which is due to the current flowing through driver and load transistors [15].

The dynamic approach minimizes the number of branches between supply and ground, reducing this kind of leakage power. On the other hand, the dynamic power consumption associated to the charge and discharge of the output capacitance is generally negligible, due to the modest switching frequencies that printed transistors can achieve [4].

Fig. 2: Linear regime transfer characteristics obtained from sets of 10 devices per channel length L [μm] and per foil, manufactured with the 3-layer hybrid dielectric stack (Fig. 1(d)). All the OTFTs feature $W=1000$ μm. $V_{DS}=-1$ V.

Fig. 3: Schematic of the 8-stage row drivers (a) and dynamic cell (b).

Fig. 4: Layout comparison between (a) DyC, (b) PTL and (c) static single delay stages.

The proposed DyC (Fig. 3(b)) exploits clocked logic gates [15] to control the propagation of the D input to the output Q_N . To this aim, CK and $\overline{CK}$ alternatively enable the push-pull output stages (M4-M6 and M9-M11) of a bootstrapped (M1-M3) and diode-connected (M7-M8) inverter. The switches M5 and M10 cause a reduction of the output voltage swing that could lead to circuit failures when propagating over multiple stages. This issue is solved here by using a bootstrapped inverter (M1-M3, C1) at the input of each cell. This inverter achieves nearly rail-to-rail output swing using three transistors and a 15 pF bootstrap capacitance, restoring the correct signal voltage levels. In each DyC the output signal is extracted at the node Q_{N-1} and fed to a chain of tapered inverters (Fig. 3(a)) that drives the large capacitance of the row line. For the output inverters, a pseudo-CMOS topology [16] is preferred to a diode-connected one, due to its better dynamic performance, achieved here at the expenses of a reduced output swing.

The proposed architecture outperforms equivalent implementations based on static and PTL logic in terms of energy efficiency (Energy-Delay Product, Table II) and integration density. Indeed, the proposed solution requires nearly the same number of VIAs per device compared to the PTL cell, but allows a more compact layout compared to the static and PTL cells (Fig. 4), which minimizes the routing crossovers and benefits from the absence of the pass-gate transistors. It should be highlighted that in the considered technology the gate metal layer is screen-printed and thus exhibits lower resolution and registration capability compared to the rest of the layer stack, leading to larger feature sizes. The main performance indicators and layout parameters of single delay stage circuits designed with the DyC, PTL and static approaches are listed in Table II.

IV. MEASUREMENT RESULTS

The measurements of the 8-stage organic row drivers based on DyCs have been performed 4 weeks after foil fabrication, in air and dark conditions. The circuit is driven by 200 Hz

TABLE II
SINGLE DELAY STAGE COMPARISON (BASED ON SIMULATION)

Parameter	Unit	DyC	PTL	Static
Number of VIAs		11	14	23
Number of devices		12	18	32
Area occupation	[cm ²]	0.30	0.67	1.34
Integration density	[devices/cm ²]	40	26	23
Propagation delay	[μs]	179	114	87
Power consumption	[mW]	0.22	0.71	2
Energy-Delay Product (EDP)	[pJs]	7	9.2	15.1

Fig. 5: Recorded output signals of the 8-stage row drivers. Each output line is displayed with a vertical offset to improve clarity.

complementary clocks to produce 2.5 ms row-enable pulses. The capacitance at each row output is approximately 10 pF. The complete system consumes 87.9 μ A with a dual supply voltage of ± 18 V. The current consumption is nearly equally divided between the row driver logic (44.6 μ A) and the output buffers (43.3 μ A). The maximum propagation delay measured among the output rows is 375 μ s, the largest rise time and fall time are respectively 76 μ s and 834 μ s, while the minimum output line swing spans from 17 V to -11 V.

The output waveforms recorded from one of the 8-stage organic row drivers are presented in Fig. 5. The correct functionality of all 15 row driver circuits measured on 5 different foils has been confirmed, leading to a 100% yield for the considered samples. The complete organic 8-stage row drivers (including output buffers) counts 139 transistors and 9 capacitors, requiring an area of 6.6 cm². The micrograph of the circuit is provided in Fig. 6. The achieved circuit yield performance corresponds to a total number of 2085 working OTFTs. This result is not in contrasts with the device yield analysis discussed in section II. Indeed, the multi-fingered transistors used in this circuit typically require smaller gate area compared to the TLM layouts used for OTFT characterization, and thus are less prone to defects.

Fig. 6 Micrograph of the printed 8-stage organic row drivers.

V. CONCLUSION

In this work we demonstrated yield performance improvements achieved by exploiting a cross-linked dielectric and a multilayer printing approach in a gravure-printed OTFT technology. A transistor yield value of 99.8% has been extracted over a population of 540 measured devices. Eight-stage row drivers based on a novel dynamic cell have been designed, manufactured with this OTFT technology and characterized. The driving circuit comprises 139 OTFTs and 9 capacitors, and requires an area of 6.6 cm². The technology improvements, together with the development of a robust circuit architecture allowed to obtain a 100% circuit yield for 15 measured 8-stage row drivers, fabricated over 5 successive foils. These circuits can potentially address a 120-rows matrix, enabling e.g. flexible displays featuring a Quarter Quarter Video Graphics Array (QQVGA) resolution (160 x 120 pixels).

REFERENCES

- [1] G. Grau, V. Subramanian, "Fully High-Speed Gravure Printed, Low-Variability, High-Performance Organic Polymer Transistors with Sub-5 V Operation", *Advanced Electronic Materials*, vol.2, no. 4, pp. 1-8, Apr. 2016. DOI: 10.1002/aelm.201500328.
- [2] J. Sun, H. Park, Y. Jung, G. Rajbhandari, B. B. Maskey, A. Sapkota, Y. Azuma, Y. Majima, G. Cho, "Proving Scalability of an Organic Semiconductor To Print a TFT-Active Matrix Using a Roll-to-Roll Gravure", *ACS Omega* vol. 2, no. 9, pp. 5766-5774, Sep. 2017. DOI: 10.1021/acsomega.7b00873.
- [3] Y. Takeda, Y. Yoshimura, R. Shiwaku, K. Hayasaka, T. Sekine, T. Okamoto, H. Matsui, D. Kumaki, Y. Katayama, S. Tokito, "Organic Complementary Inverter Circuits Fabricated with Reverse Offset Printing", *Advanced Electronic Materials*, vol.4, no.1, pp. 1-5, Nov. 2017. DOI: 10.1002/aelm.201700313.
- [4] M. Charbonneau, D. Locatelli, S. Lombard, C. Serbutoviez, L. Tournon, F. Torricelli, S. Abdinia, E. Cantatore, M. Fattori, "A Large-Area Gravure Printed Process for P-type Organic Thin-Film Transistors on Plastic Substrates", in *Proc. 48th ESSDERC*, Dresden, Germany, Sep. 2018, pp. 70-73. DOI: 10.1109/ESSDERC.2018.8486895.
- [5] M. Mizukami, S. Cho, K. Watanabe, M. Abiko, Y. Suzuri, S. Tokito, J. Kido, "Flexible Organic Light-Emitting Diode Displays Driven by Inkjet-Printed High-Mobility Organic Thin-Film Transistors", *IEEE Electron Device Lett.*, vol. 39, no.11, pp. 39-42, January 2018. DOI: 10.1109/LED.2017.2776296
- [6] G.-S. Ryu, M. Won Lee, C. Kun Song, "Printed flexible OTFT backplane for electrophoretic displays", *Journal of Information Display*, vol. 12, no. 4, pp. 213-217, Dec. 2011. DOI: 10.1080/15980316.2011.621336.
- [7] M. Fattori, S. Abdinia, G. Pauer, B. Stadlober, H. Gold, J. Socrates, F. Torricelli, E. Cantatore, "Organic Pressure-Sensing Surfaces Fabricated by Lamination of Flexible Substrates", *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol.8, no. 7, pp. 1159-1166, Jul. 2018. DOI: 10.1109/TCPM.2018.2799700.
- [8] Y. Kato, T. Sekitani, Y. Noguchi, M. Takamiya, T. Sakurai, T. Someya, "A large-area, flexible, ultrasonic imaging system with a printed organic transistor active matrix" in *Proc. IEDM*, San Francisco, USA, Dec. 2008. DOI: 10.1109/IEDM.2008.4796623.
- [9] P. van Lieshout, E. van Veenendaal, L. Schrijnemakers, G. Gelinck, F. Touwslager, E. Huitema, "A flexible 240 320-pixel display with integrated row drivers manufactured in organic electronics", in *Proc. ISSCC*, 2005, San Francisco, USA, Feb. 2005. DOI: 10.1109/ISSCC.2005.1494127.
- [10] G. Gelinck, E. Huitema, E. van Veenendaal, E. Cantatore, L. Schrijnemakers, J. B. P. H. van der Putten, T. C. T. Geuns, M. Beenhakkers, J. B. Giesbers, B.-H. Huisman, E. J. Meijer, E. Mena Benito, F. Touwslager, A. W. Marsman, Bas. J. E. van Rens, D. M. de Leeuw, "Flexible active-matrix displays and shift registers based on solution-processed organic transistors", *Nature Materials*, vol. 3, pp. 106-110, Feb. 2004. DOI: 10.1038/nmat1061.
- [11] S. Abdinia, T.-H. Ke, M. Ameys, J. Li, S. Steudel, J. L. Vandersteen, B. Cobb, F. Torricelli, A. van Roermund, E. Cantatore, "Organic CMOS Line Drivers on Foil", *Journal of Display Technology*, vol. 11, no. 6, pp. 564-569, Jun. 2015. DOI: 10.1109/JDT.2015.2421344.
- [12] B. Crone, A. Dodabalapur, Y.-Y. Lin, R. W. Filas, Z. Bao, A. LaDuca, R. Sarpeshkar, H. E. Katz, W. Li, "Large-scale complementary integrated circuits based on organic transistors", *Nature*, vol. 403, pp. 521-523, Feb. 2000. DOI: 10.1038/35000530.
- [13] ASTM D3363-05(2011)e2, "Standard Test Method for Film Hardness by Pencil Test", *ASTM International*, West Conshohocken, PA, 2011. DOI: 10.1520/D3363-05R11E02.
- [14] M. Fattori, J. A. Fijn, L. Hu, E. Cantatore, F. Torricelli, M. Charbonneau, "Circuit Design and Design Automation for Printed Electronics", 2019 Design, Automation & Test in Europe Conference & Exhibition (DATE), Florence, Italy, Mar. 2019. DOI: 10.23919/DATE.2019.8715095.
- [15] Y. Suzuki, K. Odagawa, T. Abe, "Clocked CMOS calculator circuitry", *IEEE Journal of Solid State Circuits*, vol. 8, pp. 462-469, Dec. 1973. DOI: 10.1109/ISSCC.1973.1155149.
- [16] T.-C. Huang, K.-T. Cheng, "Design for Low Power and Reliable Flexible Electronics: Self-Tunable Cell-Library Design", *Journal of Display Technology*, vol. 5, no.6, pp. 206-215, Jun. 2009. DOI: 10.1109/JDT.2008.2010273.