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Citation for published version (APA):

Retianza, D., van Duivenbode, J., & Huisman, H. (2021). An Objective Evaluation of Redundant High Precision Amplifier. In *Proceedings of the Energy Conversion Congress and Exposition - Asia, ECCE Asia 2021* (pp. 1205-1212). [9479055] Institute of Electrical and Electronics Engineers. <https://doi.org/10.1109/ECCE-Asia49820.2021.9479055>

DOI:

[10.1109/ECCE-Asia49820.2021.9479055](https://doi.org/10.1109/ECCE-Asia49820.2021.9479055)

Document status and date:

Published: 13/07/2021

Document Version:

Accepted manuscript including changes made at the peer-review stage

Please check the document version of this publication:

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
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An Objective Evaluation of Redundant High Precision Amplifier

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Abstract—This paper proposes an objective evaluation of three possible basic cell topologies for a three-phase high precision amplifier considering redundancy. Cold redundancy and hot redundancy are considered as redundant structures. The evaluation is based on the two performance objectives. The first one is the efficiency and power density performance, and the second one is through the converter system reliability. Results show that the hot-redundancy ANPC GaN converter operating at 183kHz is the most optimal solution amongst the considered basic cell topologies.

Index Terms—efficiency, power density, redundancy, reliability.

I. INTRODUCTION

In order to achieve a high-precision fast-moving actuator stage in a lithographic application, a power amplifier with high precision output current generation is required. With the increase of complexity in the semiconductor manufacturing process, the increase of productivity (throughput) by using higher speed and acceleration of the moving stages actuator is demanded [20]. It implies an increase of the power amplifier's output power. Additionally, decreasing the actuator cable weight is desirable as it reduces disturbance forces and model uncertainties [19]. Hence, increasing the operating voltage level is favored instead of an increase in operating current.

In the future high precision amplifier, fault-tolerance is expected to be included in the system. However, creating such a system will increase the cost and reduce the power density as some additional features are incorporated. In recent years, wide bandgap (WBG) devices based on GaN or SiC materials have become available. By using WBG devices, the converter power density can be increased due to the possibility of a further increase in switching frequency [15]. Consequently, some redundancy can be added to the system without adding to the power amplifier mass and volume compared to the previous generation.

Since voltage levels $\geq 1\text{kV}$ are desired, the application of a conventional two-level converter is facing a limitation in the term of WBG devices blocking voltage. Therefore, a multilevel structure should be implemented [6]. Using a

This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 875999. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Netherlands, Belgium, Germany, France, Austria, Hungary, United Kingdom, Romania, Israel

Fig. 1. Three considered basic cells (a) ANPC based on GaNFET (b) 2LC based on SiC (c) ANPC based on SiC.

multilevel structure can lower the device voltage stress, further increasing its reliability. It is essential to consider that the chosen topology should comply with the specified objectives in a post fault mode under single-point failure, that are:

- Reduced (maximum 50%) throughput is acceptable.
- A minor increase in losses is acceptable.
- The output accuracy should be maintained.

For achieving those objectives, a phase-leg redundant structure can be used the system. This structure has been discussed intensively in [2] and [14]. A conventional circuit redundancy that includes a fast-fuse is undesirable in the WBG implementation as its melting time is higher than the WBG short circuit breakdown time. Besides, the additional fuse in the power loop is difficult to integrate as it significantly increases the loop inductance, which would highly deteriorate the converter performance. Therefore, a structure without the addition of a fast fuse should be considered. This paper gives a new fault-tolerant perspective for high precision amplifiers in the form of efficiency, power density, and reliability performance.

II. SEMICONDUCTOR LOSSES AND HEATSINK VOLUME

The considered output power P_{out} is 20kW and the input DC voltage V_{dc} is $\geq 1\text{kV}$. By using sine-wave currents and voltages for the comparison, the peak output current I_L is written as $\frac{2P_{out}}{V_{dc}}$. In this paper, Active Neutral Point Clamped (ANPC) and Two-Level Converter (2LC) are considered as basic cells for the three-phase inverter. These cells are shown in figure 1.

Fig. 2. A possible topology implementation for Hot and Cold Redundancies

Basic cell A is an ANPC GaN converter that operates at 1kV bus voltage, while basic cell B consists of two SiC switches (S_1 and S_2). For basic cell C, V_{dc} can be increased due to the higher blocking voltage of SiC devices. Two redundant structures will be considered:

- **Hot Redundancy** – A parallel structure of the basic cell such that a part of power is delivered by redundant cells.
- **Cold Redundancy** – A parallel structure such that other paralleled basic cells are in standby mode.

A possible topology that can accommodate Hot and Cold Redundancy is constructed, which is depicted in figure 2.

Even though the redundant cell is not active during the normal situation, it should have the capability to handle full load. In contrast, as the power-sharing is permissible, a lower-rated device current conduction capability can be chosen in hot redundancy. The connector between the redundant and the basic cell is constructed from a back-to-back Silicon IGBT switch (S_{b2b}), which only suffers conduction loss. Two Si-IGBT in common emitter configuration are used to construct S_{b2b} . Since the body diode is not embedded in the GaN transistors, there is no reverse recovery. Therefore, the reverse conduction of GaN devices is dependent on the reverse conduction resistance and a constant voltage drop V_{drop} between the source and drain of the GaN transistor. The forward and reverse conduction loss, P_{fw} and P_{rev} can be formulated as

$$P_{fw} = I_{rms}^2 R_{dson}, \quad P_{rev} = V_{drop} I_{avg} + I_{rms}^2 R_{rev}, \quad (1)$$

where R_{dson} , R_{rev} , I_L , and I_{avg} are on-state drain-source resistance, reverse conduction resistance, switch rms current, and switch average current, respectively.

First, the loss calculation is derived for the ANPC. A modulation strategy such that only S_2 and S_3 are switched in high-frequency is considered, similar to [18]. The other switches are switching based on the fundamental frequency f_1 of the output voltage. The switching scenario can be expressed as

$$S_1 = S_6 = \bar{S}_4 = \bar{S}_5 = \begin{cases} 1 & 0 \leq \omega t \leq \pi \\ 0 & \pi \leq \omega t \leq 2\pi \end{cases}, \quad (2)$$

$$S_2 = \bar{S}_3 = \begin{cases} M \sin(\omega t + \phi) & 0 \leq \omega t \leq \pi \\ 1 + M \sin(\omega t + \phi) & \pi \leq \omega t \leq 2\pi \end{cases}, \quad (3)$$

where M is the modulation index.

The output load current is a pure sinusoid that lags with a phase ϕ with respect to the output voltage. The calculation can be simplified by only considering a half cycle of the current waveform as S_1 , S_2 , and S_5 are complementary to S_4 , S_3 , and S_6 , respectively. Thus, the loss analysis can be grouped into P_{14} , P_{23} and P_{56} . The conduction loss P_{14} is written as

$$P_{14c} = \frac{4MI_L^2}{3\pi n_p^2} (R_{dson} \cos^4(\phi/2) + R_{rev} \sin^4(\phi/2)) \\ \dots + \frac{I_L MV_{drop} ((\pi - \phi) \cos \phi + \sin \phi)}{2\pi n_p}. \quad (4)$$

The conduction losses P_{23c} and P_{56c} are shown in (5) and (6), respectively.

$$P_{23c} = \frac{R_{dson}(T_j)I_L^2}{\pi n_p^2} \left(\frac{4M \cos \phi}{3} + \frac{\phi - \cos \phi \sin \phi}{2} \right) \\ \dots + \frac{V_{drop} I_L}{\pi n_p} \left(\left(1 + \frac{\pi M}{2} \right) \cos \phi - 1 \right) \\ \dots + \frac{R_{rev}(T_j)I_L^2}{\pi n_p^2} \left(-\frac{4M \cos \phi}{3} + \frac{\pi - \phi + \cos \phi \sin \phi}{2} \right), \quad (5)$$

$$P_{56c} = R_{dson}(T_j) \left(\frac{I_L^2 (-8M \cos^4 \phi/2 + 3(\pi - \phi + \cos \phi \sin \phi))}{6\pi n_p^2} \right) \\ \dots + R_{rev}(T_j) \left(\frac{I_L^2 (3\phi - 8M \sin^4 \phi/2 - 3\cos \phi \sin \phi)}{6\pi n_p^2} \right) \\ \dots + \frac{I_L V_{drop} (2 + (-2 + M\phi) \cos \phi - M \sin \phi)}{2\pi n_p}. \quad (6)$$

T_j and I_L are the device junction temperature and peak load current, respectively. n_p is equal to one for cold redundancy and two for hot redundancy. Switching energy losses are extracted from the SPICE model of the GaN switch, and a polynomial model fitted to this data. The double pulse test bench with a specified DC input voltage is created in SPICE, including all parasitic elements which are identified in the test bench. The result is a polynomial description of Turn-On energy E_{on} and Turn-Off energy E_{off} for different junction temperatures and currents. As an example, the result of curve fit extraction for the GS66508T GaN device is depicted in Figures 3a and 3b.

The polynomial models in Figures 3a and 3b are used to construct the switching loss equation for the ANPC converter, with the switching loss equation for switches S_2 and S_3 written as

$$P_{23sw} = f_s \left(E_{off} \left(\frac{I_L}{\pi n_p}, T_{j23} \right) + E_{on} \left(\frac{I_L}{\pi n_p}, T_{j23} \right) \right), \quad (7)$$

while the switching loss for switch S_1 and S_4 , P_{14sw} , and S_5 and S_6 , P_{56sw} , are written in equation 8 and 9, respectively.

$$P_{14sw} = f_1 E_{on} \left(\frac{I_L}{n_p} \cos \phi, T_{j14} \right). \quad (8)$$

Fig. 3. The extracted energy loss Polynomial Models of GS66508T GaN during (a)Turn-On (b)Turn-Off. The models is used for constructing the switching loss equations for considered basic cell topologies.

$$P_{56sw} = f_1 E_{off} \left(\frac{I_L}{n_p} \cos \phi, T_{j56} \right). \quad (9)$$

The total loss is the summation of all transistor losses, that can be written as

$$P_{loss,t} = \underbrace{P_{14c} + P_{14sw}}_{P_{14}} + \underbrace{P_{23c} + P_{23sw}}_{P_{23}} + \underbrace{P_{56c} + P_{56sw}}_{P_{56}}. \quad (10)$$

$$P_1 = P_4 = \frac{P_{14}}{2}, \quad P_2 = P_3 = \frac{P_{23}}{2}, \quad P_5 = P_6 = \frac{P_{56}}{2}.$$

Equations (4)-(11) can be used for the loss formulation of basic cell C as it also exhibits an ANPC topology. However, $R_{rev}(T_j)$ and V_{drop} in (4)-(6) should be changed to $R_F(T_j)$ and $V_F(T_j)$ since the current flows through the body diode during reverse conduction at SiC MOSFET. For Topology B, i.e., the two-level topology, the switching scenarios of devices S_1 and S_2 are expressed as

$$S_1 = \frac{1 + M \sin(\omega t + \phi)}{2}, \quad (11)$$

$$S_2 = \frac{1 - M \sin(\omega t + \phi)}{2}. \quad (12)$$

The conduction loss for Topology B is formulated as

$$P_{c12} = \frac{R_{dson}(T_j) I_L^2 (3\pi + 8M \cos(\phi))}{12\pi n_p^2} + \frac{V_F(T_j) I_L (4 - M\pi \cos(\phi))}{4\pi n_p} + \frac{R_F I_L^2 (T_j) (3\pi - 8M \cos(\phi))}{12\pi n_p^2}. \quad (13)$$

A similar procedure is used for calculating the switching loss, where the switching loss equation for S_1 and S_2 is formulated as

$$P_{12sw} = f_s \left(E_{off} \left(\frac{I_L}{\pi n_p}, T_{j12} \right) + E_{on} \left(\frac{I_L}{\pi n_p}, T_{j12} \right) \right), \quad (14)$$

where the total loss of the basic cell is the summation of P_{12c} and P_{12sw} . The conduction loss of the connector S_{b2b} does not depend on the modulation strategy. Therefore, the conduction loss P_{cb2b} is formulated as

$$P_{cb2b} = (R_{Fi}(T_j) + R_{CE}(T_j)) \frac{I_L^2}{2n_p^2}, \quad (15)$$

Fig. 4. Cauer model of ANPC converter

Fig. 5. (a) GaN Thermal Pad Area (b) SiC MOSFETs TO-247 Thermal Pad Area

where R_{Fi} and R_{CE} are the Body Diode and the IGBT's common-emitter resistance, respectively.

A Cooling System Performance Index (CSPI) is defined to estimate the heatsink volume v_{heat} , as

$$CSPI = \frac{1}{v_{heat} R_{th,hs}}, \quad R_{th,hs} = \frac{T_{hs,max} - T_a}{P_{loss,t} + P_{cb2b}}, \quad (16)$$

where $P_{loss,t}$ is the total switch losses, T_a is the ambient temperature and $R_{th,hs}$ is the heatsink surface to ambient thermal resistance [4]. To calculate the heatsink surface temperature, a Cauer model is created, which is illustrated in figure 4. R_{tjc} is the thermal resistance from junction to case, and R_{chs} is the case to heatsink thermal resistance due to the presence of the thermal insulation material. R_{chs} is calculated from the thermal interface material's thermal conductivity and the device thermal interface cross-sectional area.

From figure 5, the thermal cross-section area for GaN is written as

$$A_{th} = w_{pad} l_{pad}, \quad (17)$$

while the thermal cross-section area for SiC MOSFET and IGBT with TO-247 package is written as

$$A_{th} = w_{pad} l_{pad} - \pi \frac{d_{pad}^2}{4}. \quad (18)$$

Let GAPFILLER GS 3500S35-07 is chosen as a thermal interface material (TIM) [9]. The TIM has a material thickness

TABLE I
THE FILTER INDUCTOR PARAMETER

Parameter	Description	Value
Θ	AC loss fraction	0.2
γ	Core loss fraction	1
ρ_w	Copper conductivity	$1.72 \cdot 10^{-8} \Omega m$
k_u	Fill factor	0.4
B_{max}	Max. core magnetic density	0.25T
ΔT	Core surface temp. raise	30K
κ	Core thermal constant	$3m^{\frac{2}{3}} K/W$
k_w	Winding Volume Constant	5
k_c	Core Volume Constant	7
k_v	Inductor Volume Constant	13.6

of 0.178 mm and thermal conductivity $3.6 \frac{W}{mK}$. Therefore, R_{chs} is calculated as

$$R_{chs} = \frac{t_{TIM}}{\lambda_{TIM} A_{th}}. \quad (19)$$

The maximum heatsink temperature $T_{hs,max}$ can be expressed as

$$T_{hs,max} = \min_i(T_{j,set} - (P_i(R_{tjc,i} + R_{chs,i}))), \quad (20)$$

where R_{tjc} , R_{chs} , and $T_{j,set}$ are the junction-case thermal resistance, the case-heatsink thermal resistance and the design permitted junction temperature, respectively. i is the switch number of the basic cell. Temperature $T_{j,set}$ is set to 373K. Assuming an ambient temperature T_a of 298K, an air-forced cooling heatsink has CSPI Index 6-20 [4]. In this application, the air-forced cooling with CSPI = 10 is used as a design parameter.

III. OUTPUT FILTER AND DC-LINK

A. Output Filter Inductor

Let Δi_L be 10% of I_L as a design objective. The inductance of output the filter for the maximum output current ripple is formulated as

$$L_f = \frac{V_{dc}}{4N\Delta i_L f_s}, \quad (21)$$

where N is equal to 1 for two-level and 2 for the ANPC converter. The output inductor filter volume v_{ind} is designed based on the modified Area Product A_p , which is given by (22).

$$A_p = \left(\frac{L_f I_L^2 \sqrt{1 + \Theta + \gamma}}{n_L B_{max} \sqrt{\frac{2\sqrt{k_c}}{\kappa \rho_w k_w}} \sqrt{k_u \Delta T}} \right)^{8/5}, \quad v_{ind} = n_L k_v A_p^{\frac{3}{4}}, \quad (22)$$

where L_f is the inductance value and n_L is the number of parallel inductors. The values of k_w , k_c , and k_v are extracted from the EPCOS EE Ferrite flat core datasheet [5]. The other parameters are described in the table I.

Note that, it is necessary to keep the value of L_f after paralleling similar to the value before paralleling such that the output current ripple objective Δi_L should be 10% of I_L . The design is based on the EE Ferrite flat core for low core losses

Fig. 6. (a) The illustration of Inductor Volume Analysis (b) Core structure in x-z and x-y direction

Fig. 7. Volume Estimation of Inductor with respect to the switching frequency

in high frequency and with a low profile for better heat transfer. The inductor volume and the core and winding structure are illustrated in figure 6a and 6b, respectively.

The estimated volumes for single and paralleled inductors are presented in Figure 7. Increasing the number of paralleled flat inductors is reducing the total inductor volume. However, as the switching frequency increases, the effect is negligible.

To losses due to the inductor $P_{loss,l}$ are estimated as

$$P_{loss,l} = (1 + \Theta + \gamma)(n_L \rho_w v_w k_u J^2), \quad (23)$$

where v_w is the winding volume and J is the winding current density. J is expressed as

$$J = \sqrt{\frac{\sqrt{k_c} \Delta T}{(1 + \Theta + \gamma)(\kappa \rho_w k_w k_u)}} \frac{1}{\sqrt{A_p^3}}. \quad (24)$$

The winding volume v_w and core volume v_c of the individual inductor are formulated based on the area product, which is written as

$$v_w = k_w A_p^{\frac{3}{4}}, \quad v_c = k_c A_p^{\frac{3}{4}}. \quad (25)$$

B. Output Filter Capacitor

The calculation of output capacitance has been derived in [13], which is written as

$$C_f = \frac{1}{(2\pi f_s)^2 n_L L_f \text{Att}_{req}}, \quad (26)$$

where Att_{req} is the required attenuation of the filter. Here, the attenuation is chosen to be 0.01 such that it provides

an adequate damping at the considered switching frequency while keeping the resonance frequency far from the switching frequency [8]. It is assumed that the volume of the output filter capacitor is related to the stored energy, which is formulated as

$$v_{capi} = k_c C_f V_{dc}^2 \quad (27)$$

where k_c is a capacitor volumetric coefficient extracted from datasheets [13]. Here, the value of k_c is $93.10^{-3} \frac{L}{FV^2}$.

C. DC-Link Capacitor

The DC-Link capacitor formula's derivation is based on the capacitor's rms current I_c as the impact of the DC-Link capacitance value is omitted from the comparison of volume analysis. The maximum capacitor ripple voltage is decreasing with the increase of f_s due to the WBG implementation. Based on the modulation in (2) and (3), the ANPC can be divided into two sub-converters. The first one is active during $0 \leq \omega t < \pi$, that is, the converter current will flow through S_1, S_2, S_3, S_6 , and the upper capacitor while the second one is active during $\pi \leq \omega t < 2\pi$. During this interval, the converter current will flow through S_2, S_3, S_4, S_5 , and the lower capacitor. By using a derivation similar to the ones presented in [3], [7], the I_c in one capacitor of the three-phase ANPC is similar to the case of the three phases two-level topology, which is written as

$$I_c = I_L \sqrt{M \left(\frac{\sqrt{3}}{4\pi} + \left(\frac{\sqrt{3}}{\pi} - \frac{9M}{16} \right) \cos^2 \phi \right)}. \quad (28)$$

s_c is introduced as a specific current density, such that the DC-Link capacitor volume v_{capi} can be directly related to I_c [13]. v_{capi} is written as

$$v_{capi} = \frac{I_c}{s_c}, \quad (29)$$

where s_c is approximated from the selected capacitor datasheets for the considered voltage rating. In this paper, the 600V DC-link TDK MKP series is chosen, with the value of s_c is approximated as $100 \frac{A}{L}$ [21].

IV. OBJECTIVE EVALUATION THROUGH EFFICIENCY-POWER DENSITY

The combination of Efficiency and Power Density ($\eta - \rho$) of the system is used to obtain an objective evaluation. The efficiency is formulated as

$$\eta = \frac{P_{out}}{P_{out} + (P_{loss,t} + P_{loss,l} + P_{cb2b})}, \quad (30)$$

while the Power Density is expressed as

$$\rho_{conv} = \frac{P_{out}}{v_{ind} + v_{heat} + v_{capi} + v_{capi}}. \quad (31)$$

In this analysis, GaN devices from GaN systems and SiC devices from Cree Wolfspeed are used. Five WBG devices are considered, GS66508T and GS66516T, for GaN devices, and C3M0075120K, C3M003210K, and C3M0160120D, for SiC devices. The topologies' efficiency and power density

Fig. 8. η - ρ map of considered topologies. Basic Cell A (ANPC GaN) Hot Redundancy is chosen as it has the highest weighted η - ρ value.

Fig. 9. Optimal solution loss and volume comparison for hot redundancy structure

are mapped in Figure 8. The optimal design corresponds to the maximum of the weighted sum of η and ρ , which is located close to the maximum of the curves in the ρ direction. Power Loss and volume details of the optimal solution for hot-redundant structures is depicted in figure 9. From figure 8, the following properties can be observed:

- The parallel hot-redundancy shows a higher system power density and overall efficiency than the cold-redundant version. It happens since load sharing is permitted in hot-redundancy, which leads to reduced losses in semi-conductors.
- The implementation of a GaN device significantly improves the power density, as it is capable of switching at high frequency with low losses.
- The introduction of a multilevel topology for the high precision amplifier increases the power density by 2-3 times compared to the two-level converter.

From the observation, it is clear that considering hot-redundancy for the system is preferred. Therefore, Basic cell A hot-redundancy, which uses GS66508T and operates at 183kHz, is the selected design candidate.

V. OBJECTIVE EVALUATION THROUGH RELIABILITY

To evaluate the system reliability, a failure rate $\lambda(t)$, which corresponds to statistically one failure per billion hours of operation, is used. Note that the failure rate is a function

of time which is typically illustrated as a 'bathtub' curve. During the system's useful time, the failure rate λ can be approximated as a constant. In this paper, λ is used for a basic assumption for the objective evaluation. It corresponds to a random distribution of single-point failures, such as a Single-Event Burnout (SEB) in semiconductor devices [10]. Hence, a short-circuit failure mode is used for constructing the reliability function.

The exponential reliability function of a system is written as

$$R_{sys} = e^{-\lambda_{sys}t}, \quad (32)$$

where λ_{sys} is a constant failure rate of the considered system. To know the value of λ_{sys} , it is important to formulate the device failure rate. From the latest GaN reliability test [1], the failure rate of GaN and SiC devices is on the same order of magnitude as its silicon-based predecessor. Hence, the scaled failure rate function by considering important parameters is used to simplify the analysis. Based on [12], a failure rate function depends on three factors: the operating voltage, the junction temperature, and the dependence on the altitude. In this analysis, only the first two factors are considered. Considering the GaN device of Basic Cell A, which has a ratio V_{ds}/V_{dsMax} is 500V/650V, T_j is 373K, to be used as a failure rate reference λ_{ref} . Reformulating the equation from [17], the failure rate function, which depends on considered factors, is formulated as

$$\lambda(V_{ds}, V_{dsMax}, T_j) = \lambda_{ref} e^{4640 \left(\frac{1}{373} - \frac{1}{T_j + 273} \right)} e^{1.7 \left(\frac{V_{ds}}{V_{dsMax}} - \frac{500}{600} \right)} \quad (33)$$

where V_{ds} is the device operating voltage and V_{dsMax} is the maximum device blocking voltage. Note that T_j is specified in °C. It is important to be noted that λ_{ref} is canceled out from the following comparative analysis, as all of the failure rates will be normalized to λ_{ref} .

Figure 10 shows the structure and reliability block diagram (RBD) of the considered systems, i.e., two-level and ANPC converter. Both systems do not exhibit any fault-tolerant feature, i.e., if one switch is shorted, the system will not comply with the specified objectives. Therefore, the failure rate is directly given by the summation of the individual device's failure rates, such that the RBD can be drawn as a series structure. From the RBD in figure 10, the phase leg failure rate λ_{leg} of the two-level converter is written as

$$\lambda_{2L} = 2\lambda_{S12}. \quad (34)$$

The failure rate of S_1 and S_2 are similar such that it is named as λ_{S12} . Then, λ_{leg} of the ANPC converter is formulated as

$$\lambda_{ANPC} = 2\lambda_{S14} + 2\lambda_{S23} + 2\lambda_{S56}. \quad (35)$$

The failure rate grouping from (35) is inline with the previous discussion on the loss analysis, i.e., the switch group shares a similar junction temperature, which means the same failure rate.

The RBD of hot redundancy is shown in figure 11. The reliability modeling is based on a 'k-out-of-n' redundant

Fig. 10. Structure and Reliability Block for Two-Level and ANPC basic cell

Fig. 11. Reliability Block Diagram of Hot Redundancy

structure, that is, a structure will works if at least k of the n components works can be used. The primary and redundant cell share a similar load, such that the condition $\lambda_p = \lambda_r$ holds, where λ_p and λ_r are the primary and redundant cell. The mathematical model of identical failure rate 'k-out-of-n' has been derived in [11], which is written as

$$R_{koon}(t) = \sum_k^n C_n^k R_{leg}(t)^k (1 - R_{leg}(t))^{n-k}, \quad (36)$$

where C is a combination operator and R_{leg} is a phase leg reliability function based on the failure rate which is formulated from (34) or (35). From figure 11, the R_{1o2} is the reliability function of a single phase leg that consists of primary and redundant cells. R_{1o2} can be modeled based on '1-out-of-2', which is written as

$$R_{1o2}(t) = 2e^{-\lambda_p t} - e^{-2\lambda_p t}. \quad (37)$$

The reliability of three-phase hot redundancy R_{hr} is constructed from from the connection of three sections with reliability R_{1o2} in series, which is formulated as

$$R_{hr}(t) = \prod_{i=1}^3 R_{1o2} = e^{-6\lambda_p t} (-1 + 2e^{\lambda_p t})^3. \quad (38)$$

The reliability of cold redundancy is depicted in figure 12. Based on the converter reconfiguration in the post fault mode, two possibilities of cold redundancy structure exist. The first structure, i.e., Type A, is a structure where all primary cells are switched to the redundant cell after a fault. The second structure, i.e., Type B, is a structure where each primary cell

Fig. 12. Reliability Block Diagram of Cold Redundancy (a) Type A - All of the primary system are switched to the redundant system after the occurrence of a fault (b) Type B - An Individual primary system is switched to the redundant system after the occurrence of a fault

can be switched to its respective redundant cell in a post-fault mode. In constructing the cold redundancy model, four assumptions are made, that are:

- The redundant cell has the initial failure rate λ_{r0} , and all of the switch operate at $T_j = 298K$.
- The short circuit protection and identification is robust, such that the probability of fault-triggering alarm is zero.
- The connector is always operating.
- The redundant cell can deliver 100% power.

Therefore, based on the previous assumption, The system is able to meet the redundancy objectives at the interval $(0, t]$ in two disjoint events:

- Primary cell does not fail in $(0, t]$. (event 1)
- Primary cell fails at the time interval $(\tau, \tau + d\tau)$, while redundant cell does not fail at $(0, \tau]$. The redundant cell is activated at τ and active at the interval $(\tau, t]$. (event 2)

Thus, the mathematical model for those events is formulated as

$$R_c = \underbrace{e^{-\lambda_p t}}_{\text{event 1}} + \underbrace{\frac{\lambda_p}{\lambda_{r0} + \lambda_p - \lambda_r} \left(e^{-\lambda_r t} - e^{-(\lambda_{r0} + \lambda_p)t} \right)}_{\text{event 2}}. \quad (39)$$

The mathematical proof of event 2 can be assessed further at [16]. It is aforementioned that the redundant cell is able to deliver 100% power such that the condition $\lambda_p = \lambda_r$ holds. Therefore, (39) is reformulated as

$$R_c = e^{-\lambda_p t} \left(1 + \frac{\lambda_p}{\lambda_{r0}} (1 - e^{-\lambda_{r0} t}) \right). \quad (40)$$

From figure 12a, a series connection of each phase leg in primary and redundant cells leads to a threefold increase in the failure rates, which means the cold-redundancy Type A reliability R_{cra} is formulated as

$$R_{cra} = e^{-3\lambda_p t} \left(1 + \frac{\lambda_p}{\lambda_{r0}} (1 - e^{-3\lambda_{r0} t}) \right). \quad (41)$$

Meanwhile, a different series structure in figure 12b leads to a different formulation of the reliability of the cold-redundancy Type B R_{crb} , which can be written as

$$R_{crb} = \prod_{i=1}^3 R_c = e^{-3\lambda_p t} \left(1 + \frac{\lambda_p}{\lambda_{r0}} (1 - e^{-\lambda_{r0} t}) \right)^3. \quad (42)$$

Fig. 13. Comparison of unreliability between considered topologies. $T_j=383K$.

The comparison of reliability function in figure 13 is constructed by linearizing the cumulative density function or unreliability function, $F(t) = 1 - R(t)$, with respect to the $\ln t$ in the x-axis, such that the y-axis of the plot is $\ln(-\ln(1 - F(t)))$.

Let 1000 defects per million (dpm) be the objective evaluation for the comparison. From figure 13, the following properties can be observed:

- The introduction of redundancy significantly improves the Mean Time To Failure (MTTF), 33 times compared to the non-redundant converter.
- The cold-redundancy type B gives the best reliability performance amongst the other considered redundancy structures.
- Utilizing Basic cell B gives a slight reliability improvement as it uses the lowest part count compared to the other considered Basic cells.
- Low discrepancy of MTTF on any considered redundant structure and the basic cell is observed, i.e., it ranged from 0.013-0.032 of GaN device MTTF, as can be seen at the zoomed parts of figure 13.

Based on the objective evaluation through $\rho - \eta$ and reliability, Basic Cell A - Hot Redundancy that operates at 183kHz is chosen as the best candidates for a redundancy strategy as it has the best $\rho - \eta$ performance while significantly improving the reliability.

Furthermore, the objective of efficiency-power density can be combined with the reliability such that the system trade-off can be known. It is aforementioned that the device reliability depends on the junction temperature, which is related to the $\rho - \eta$ calculation. To better evaluate the impact, Mean Time Between Failure (MTBF), which is an expectation of the system's continuous operating time until failure, is obtained from the area underlying the reliability curve. MTBF can be formulated as

$$\text{MTBF} = \int_0^\infty R_{conv}(t) dt, \quad (43)$$

Fig. 14. The reliability and power density trade off for Basic Cell A - Hot Redundancy

where R_{conv} is the reliability function of the considered redundant topology as derived in equation (38), (41), and (42). By solving, (43), the MTBF of hot redundancy, $MTBF_{hr}$, is written as

$$MTBF_{hr}(T_j) = \frac{7}{10\lambda_p(T_j)}, \quad (44)$$

the MTBF for cold-redundancy Type A, $MTBF_{cra}$, is written as

$$MTBF_{cra}(T_j) = \frac{2\lambda_p(T_j) + \lambda_{r0}}{3\lambda_p^2(T_j) + 3\lambda_p(T_j)\lambda_{r0}}, \quad (45)$$

and the MTBF for the cold redundancy Type B, $MTBF_{crb}$, is formulated as

$$MTBF_{crb}(T_j) = \frac{(2\lambda_p(T_j) + \lambda_{r0}) (13\lambda_p^2(T_j) + 13\lambda_p(T_j)\lambda_{r0} + 2\lambda_{r0}^2)}{3\lambda_p(T_j) (\lambda_p(T_j) + \lambda_{r0}) (3\lambda_p(T_j) + \lambda_{r0}) (3\lambda_p(T_j) + 2\lambda_{r0})}. \quad (46)$$

Consider Basic Cell A - Hot Redundancy as an example of the trade-off analysis. Without changing the CSPI, the reliability, power density, and efficiency trade off is illustrated in figure 14. It is shown that reducing the allowable junction temperature in the system from 373K to 348K will increase the MTBF by a factor of 2.14. However, a significant heatsink volume should be added as the price of decreasing T_j . It is also noted that the lower T_j will slightly improve the efficiency because of the reduced loss in the semiconductors.

CONCLUSION

In this paper, redundant topologies for high precision amplifiers are compared. Results presented in the η - ρ map show that the hot-redundancy ANPC GaN converter, which operates at 183kHz, is the most promising solution amongst the other considered basic cells. From the objective evaluation through reliability, redundancy in any considered redundant structure significantly increases the reliability performance. It is also known that the Basic cell B-cold redundancy type A has the best reliability performance since it has the lowest part count. The objective evaluation through reliability and $\rho - \eta$ is also

presented such that the system trade-off can be analyzed. By using the basic cell A-hot redundancy, reducing the allowable junction temperature in the system from 373K to 348K is increasing the MTBF by a factor of 2.14, although with the price of a significant increase in the heatsink volume.

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