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A 0.38-pJ/b Simplex and a 1.2-pJ/b Full-Duplex Chip-to-Chip Digital Communication Interface With Data Rate and Load Capacitance Adaptability

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Abstract—This work presents a simplex and a full-duplex digital communication interface in 65 nm CMOS that enhance the energy efficiency of chip-to-chip digital communication in low-speed low-power systems, e.g., for Internet-of-Things applications. A capacitive fully dynamic simplex interface is proposed first. A self-interference cancellation network is then applied to achieve full-duplex operation. Thanks to the all-dynamic architecture, the proposed interfaces allow efficient power scaling and can provide a BER of 5.10^{-12} . The simplex and full-duplex interfaces achieve an energy consumption of 0.38 and 1.2 pJ/b, respectively (with 19 pF load). The simplex interface achieves a power reduction of $2\times$ to $27\times$ compared to conventional low-voltage CMOS for data rates from 10 kb/s to 50 Mb/s. The full-duplex interface achieves a power reduction of $5\times$ to $11\times$ for data rates from 100 kb/s to 50 Mb/s.

Index Terms—Adaptable, chip-to-chip, digital communication interface, energy efficiency, full duplex.

I. INTRODUCTION

Thanks to CMOS scaling, electronics is becoming increasingly more power-efficient and integrated. Sensor interface circuits are following this trend and can already achieve sub-nW power consumption, as shown, e.g., in [1]. The power consumption of digital chip-to-chip communication, thus, starts to become dominant in these ultralow power sensing systems. Energy efficient chip-to-chip digital communication is required (Fig. 1) when several sensor interfaces and digital signal processing blocks need to be connected on a PCB, in a multichip package, or via short cables. Examples include versatile sensing for Internet-of-Things (IoT), where multiple parameters, such as temperature, humidity, pressure, etc., need to be measured, or biomedical sensing systems with multiple active electrodes connected to a central processing unit via short cables.

Most chip-to-chip communication systems focus on improving the speed of operation, and efficiency is particularly optimized for high speeds. State-of-the-art designs can achieve 1.1 pJ/b at 100 GS/s [2]. However, these systems usually require static power consumption. Because of that, the efficiency improvement for low communication speed (data rates <100 Mb/s) remains limited.

To address digital communication efficiency in low-power low-speed systems, a conventional approach is to use low-voltage CMOS (LVCMOS) communication, where rail-to-rail signals are transmitted at a reduced supply level. Fig. 2 shows a simplified model of LVCMOS. The average energy consumption per bit of a conventional LVCMOS driver is given by

$$E_{LVCMOS} = \frac{1}{4} C_L V_{DD}^2 \quad (1)$$

where C_L is the load capacitance, V_{DD} the supply voltage, and the factor $1/4$ takes into account the fact that only $0 \rightarrow 1$ transition costs energy. (It is assumed that the probabilities of a $0 \rightarrow 0$, $0 \rightarrow 1$, $1 \rightarrow 0$, and $1 \rightarrow 1$ transition are equal.) The load capacitance

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Fig. 1. Chip-to-chip communication in low-power low speed systems.

Fig. 2. Simplified model of an LVCMOS interface.

between two chips on a PCB can easily be in the order of 5 pF. This means that an energy of 1.8 pJ/b is required using a 1.2 V LVCMOS interface. This will dominate the power budget when applied, e.g., to the 10-bit temperature sensor interface described in [1], which needs 2.43 pJ per temperature sample, and thus consumes only 0.24 pJ/b for sensing and digitalization. Therefore, it is necessary to reduce the energy consumption of the digital chip-to-chip interface. Existing low-power wireline interfaces [3], [4] use smart supplies to further improve the energy efficiency. However, the achievable efficiency depends on the operating frequency and the maximum efficiency point is only possible with an ultralow supply voltage (0.24 V) and low data rate (<1 kb/s). As a result, an extra dc-dc converter may be needed, which causes overhead at the system level. Body channel communication circuits also aim for low-power communication [5], [6], but use the human body as a transmission medium and are not immediately comparable to wireline interfaces.

Besides energy efficiency, full-duplex communication is sometimes preferred to minimize wire count, for instance in biomedical systems with active digital electrodes as shown in Fig. 1.

This work presents a simplex digital interface and a full-duplex digital interface enabling energy-efficient, reliable, and adaptable chip-to-chip communication for low-speed low-power systems. The adaptability makes the interfaces suitable for a variety of applications, with data rates from 10 kb/s to 50 Mb/s and load capacitances from a few pF to a few tens of pF, while maintaining high energy efficiency.

This letter is organized as follows. The proposed simplex digital interface and full-duplex digital interface are introduced in Section II, measurement results are presented in Section III, and conclusions are drawn in Section IV.

II. ARCHITECTURE

A. Simplex Interface

As shown in (1), the transmission power for LVCMOS is related to the transmission levels which are rail to rail. Hence, smart supply or signal attenuation techniques could be used to reduce the transmission

Fig. 3. Architecture of the proposed simplex interface.

Fig. 4. Tunable attenuation capacitor for C_{AP} and C_{AN} . (4 bit control).

power. Supply scaling was used in prior-art, but requires adaptable supplies, and low supply voltages (e.g., subthreshold) will degrade the maximum speed of operation. Therefore, in this work, a nominal 1.2 V supply is used and a programmable signal attenuation is implemented to reduce power.

Fig. 3 shows the architecture of the proposed differential simplex digital interface. The TX is built by two programmable attenuation capacitors (C_{AP} , C_{AN}) and drivers. By inserting these attenuation capacitors, the transmitted signal amplitude is reduced to

$$A_{TX} = \frac{C_A}{C_A + C_L} VDD. \quad (2)$$

As the load capacitance seen by each inverter is the series of C_A and C_L , the average energy consumption of the driver is reduced to

$$E_{TX,S} = \frac{1}{2} \frac{C_A C_L}{C_A + C_L} VDD^2. \quad (3)$$

The original factor 1/4 in (1) is increased to 1/2 in (3) due to the differential implementation. By adjusting the signal amplitude with capacitors, no extra power supply is needed to reduce power, while the capacitive division results in a dynamic consumption that scales down with the actual data rate, enabling low-power low-speed operation.

The attenuation capacitors (Fig. 3) are programmable to adjust the attenuation factor, and to accommodate different loading scenarios. For example, when the load capacitance is 24 pF and the supply voltage is 1.2 V, a 1.2 pF attenuation capacitor can be selected to have about 60 mV signal range or a 0.4 pF capacitor can be selected to have about 20 mV signal range. The tunable capacitors are implemented as MIM capacitors with switches (Fig. 4). Their value can be programmed from 80 fF to 1.2 pF with a step of 80 fF by a 4-bit word CAPCTRL. This will enable the interface to drive up to 24 pF load capacitance with about 60 mV signal range or up to 72 pF load capacitance with about 20 mV signal range. Larger or smaller tunable capacitors could be added to accommodate other loads. The matching of the capacitors is not critical as it only results in minor deviations of the amplitude.

A fully dynamic comparator working in the subthreshold region is used as RX. The minimum transmitted amplitude should be larger than the comparator's offset and noise level to prevent bit errors. A low-offset and low-noise comparator leads to lower TX power but higher RX power. With a TX amplitude of for instance 60 mV at 1.2 V supply, the transmission power is reduced to <10% of LVCMOS. At the same time, an amplitude of several tens of mV still enables a rather low-power comparator. In this work, a fully dynamic comparator composed of a preamplifier and a latch is used [7] (Fig. 5). The comparator has a simulated input-referred noise

Fig. 5. Dynamic comparator [7] with DC bias via pseudo resistors.

of 0.45 mV_{rms} and an estimated 3 σ -offset of 11 mV while consuming 0.14 pJ/b.

As the input signal is AC coupled, bias resistors (R_{BP} , R_{BN}) are added to define the DC bias voltage at the comparator input. These are implemented as highly resistive pseudo resistors (about 3.5 G Ω), to enable correct interface operation down to low data rates (<10 kb/s). The pseudo resistors suffer from large mismatch, which could result in comparator offset due to input leakage currents. However, thanks to the relaxed noise requirements, the input transistors of the comparator are only 4 μ m/60 nm in size, which limits their gate leakage current. In this way, the mismatch of the pseudo resistors is acceptable.

Note that similar to LVCMOS, this work does not yet include clock synchronization between the chips, as this depends on the application and optional data encoding. Like LVCMOS which has typically separate data and clock connections, one option is to use the proposed power-saving TX to transmit a master clock signal to all nodes. However, the receivers of such clocks will require continuous-time receivers or clocked receivers with a clock recovery circuit. Alternatively, data encoding and suitable circuits could be used such that the clock can be recovered from the data itself.

B. Full-Duplex Interface

To achieve full-duplex communication, self-interference cancellation is required.

Fig. 6 shows the architecture of the proposed full-duplex digital interface. Based on the simplex interface, a passive capacitive self-interference cancellation network (Fig. 7) is added. The bias network is implemented in the same way as in Fig. 3.

The self-transmitted signal will go through two paths with opposite polarity back to its own receiver (path1: $C_B + C_{S2}$, path2: C_{S1}), the transmitted signal amplitude at the RX comparator input can be approximated by

$$A_{TX1 \rightarrow RX1} = k_1 VDD \left(k_2 \frac{C_{S2}}{C_{S1} + C_{S2}} - \frac{C_{S1}}{C_{S1} + C_{S2}} \right) \quad (4)$$

where k_1 is the attenuation factor caused by C_A

$$k_1 = \frac{2C_A^2 C_B + C_A^2 C_L + C_A C_B^2 + C_A C_B C_L}{(2C_A C_B + C_A C_L + C_B C_L)(C_A + C_B)} \quad (5)$$

and k_2 is the attenuation factor caused by C_B

$$k_2 = \frac{C_A C_B + C_B^2}{2C_A C_B + C_A C_L + C_B^2 + C_B C_L}. \quad (6)$$

The received signal (Figs. 6 and 7) will also go through two paths (path1: C_{S2} , path2: $C_B + C_{S1}$), the received signal amplitude at the RX comparator input can be approximated by

$$A_{TX2 \rightarrow RX1} = k_1 k_2 VDD \left(\frac{C_{S2}}{C_{S1} + C_{S2}} - \frac{C_B}{C_A + C_B} \cdot \frac{C_{S1}}{C_{S1} + C_{S2}} \right). \quad (7)$$

The received signal is only mildly affected (e.g., <1 dB loss with the selected capacitors) due to the self-cancellation network. It will still be attenuated by the series of the capacitors C_A and C_B to save transmission power.

To maintain self-cancellation for different load capacitances, both C_A and C_B need to be adjusted as function of C_L , such that k_2 remains

Fig. 6. Architecture of the proposed full-duplex interface.

Fig. 7. Model of the self-interference cancellation network.

approximately constant and (4) remains approximately zero. In the prototype, C_A can be programmed from 320 fF to 4.8 pF while C_B can be programmed from 160 fF to 2.4 pF. This enables the full-duplex interface to drive about 20 pF load capacitance with about 60 mV differential signal at the comparator input. The existence of capacitors C_{S1} and C_{S2} has an attenuation effect on the transmitted signals. Hence, their values are preferably much smaller than the values of C_A and C_B , and thus they are set to 9.4 fF and 90 fF, respectively. The ratio of C_{S1} and C_{S2} is determined by the desired signal swing and the ratio of C_A and C_B . With the selected capacitor values, signal attenuation, and self-cancellation are achieved as shown in Fig. 7. During full-duplex operation, the received and transmitted signal are of equal magnitude at nodes TP and TN, but the received signal will dominate at the RX comparator input.

Theoretically, the self-transmitted signal can be cancelled by appropriate sizing of the capacitors to make (4) equal to zero. In practice, considering capacitor mismatch and extra parasitic capacitance, the self-transmitted signal will not be perfectly cancelled, while the received desired signal may also vary. However, if the residue from the self-transmitted signal combined with the worst-case comparator offset and noise is smaller than the received signal, the received signal can still be recovered correctly. Fig. 8 shows the simulated sensitivity of the desired and undesired signal components as function of individual capacitor deviations. As shown, with up to 20% deviation, there is still 60% of the nominal margin remaining. With a 60 mV nominal amplitude, this provides sufficient margin to cover for comparator offset and noise under mismatch conditions.

The energy consumption of the driver is reduced to approximately

$$E_{TX,FD} = \frac{1}{2} \frac{C_A C_B (C_A C_B + C_A C_L + C_B C_L)}{(C_A + C_B)(2C_A C_B + C_A C_L + C_B C_L)} V_{DD}^2. \quad (8)$$

With about 60 mV differential signal at the comparator input, the transmission power can be reduced to 13% of LVCMOS with the same load capacitance.

Similar to the simplex interface, the bias resistors and the capacitor network filter out low-frequency signals. The cut-off frequency of the full-duplex interface is higher than the cut-off frequency of the simplex interface because C_{S1} and C_{S2} are much smaller than C_A , C_B , and they determine the new cut-off frequency. Also, the energy consumption of a full-duplex interface is a bit higher since extra attenuation is introduced by the self-interference cancellation

Fig. 8. Sensitivity of the desired and undesired signal versus capacitor deviations.

Fig. 9. Chip micrograph in 65 nm CMOS.

Fig. 10. Measured power consumption versus data rate for the simplex interface (a) and the full-duplex interface (b) for different load capacitors.

network and margins need to be included to overcome the residual self-interference, both of which are overcome with a proportionally larger signal amplitude.

III. MEASURED RESULTS

The proposed digital interfaces are fabricated in 65 nm CMOS, as shown in Fig. 9. The simplex TX, simplex RX, and full-duplex TRX occupy an area of 0.0125, 0.00015, and 0.029 mm², respectively. More than 90% of the area is occupied by the tunable capacitors.

The interfaces use a 1.2 V supply since it is a standard supply voltage in 65 nm CMOS. Lower supply voltages are also feasible, at the cost of maximum data rate. The control clocks are provided externally for enhanced flexibility. Two chips are placed on one PCB at a few centimeters distance. To test the interface adaptability to different load capacitances, additional capacitors are soldered to the nodes TP and TN. The CAPCTRL signal is provided through an on-chip serial register.

Fig. 10(a) shows the measured power consumption of the simplex interface (including TX with capacitor drive circuitry and RX) with different data rates and load capacitances using a 20 mV signal swing. Most of this power is used in the TX to drive the capacitor network. Compared to LVCMOS, additional RX power is introduced, which is about 0.16 pJ/b at 50 Mb/s and 0.84 pJ/b at 10 kb/s (the imperfect dynamic scaling is due to an increased impact from static leakage power at low data rates). When the load capacitance becomes larger, the RX power becomes less relevant. The proposed simplex interface works for a large range of data rates (10 kb/s to 50 Mb/s) and load capacitances (0–72 pF). It achieves a power reduction of 27× with a 72 pF load capacitance at 50 Mb/s and a power reduction of 2.4×

Fig. 11. Measured BER bathtub curves for the simplex interface (a) and the full-duplex interface (b). For most of the phase settings, the BER is better than 10^{-9} .

Fig. 12. Recorded signals (at nodes TP, TN) at 5 Mb/s for (a) simplex interface and (b) full-duplex interface.

Fig. 13. Benchmark of the proposed interfaces against prior art.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work		[4]	[5]	[6]
Technology (nm)	65		130	65	180
V _{DD} (V)	1.2		0.24-1	1.2, 1	1
Simplex/ Full duplex	Simplex	Full duplex	Simplex	Full duplex	Simplex
Data rate (b/s)	10k-50M	100k-50M	1k-3M	5M-80M	100M
Power (μ W)	0.018 -30.88 *	0.13 -60.09 *	0.0054 -132	1700 -2600	3155
E/b (pJ/b)	0.38-1.47 *	1.20-1.31 *	3.61-44.1	78.8	31.55
BER	$<5 \cdot 10^{-12}$ **	$<5 \cdot 10^{-12}$ **	10^{-6}	10^{-5}	10^{-9}
Area (mm ²)	0.0142	0.029	0.0012	5.76	1.2577

* With 19pF load capacitance.

** With 99% confidence level; no errors detected for 1Tbit data.

with a 9 pF load capacitance at 10 kb/s compared to conventional 1.2 V LVC MOS. The maximum data rate of 50 Mb/s is limited by the comparator decision time, as well as the RC constants formed by the capacitive network in combination with the output resistance of the TX drivers and the on-resistance of the switches in the tunable capacitors. The maximum data rate could be increased by resizing these components, at the cost of lower efficiency.

The power consumption of the full-duplex interface at about 60 mV signal swing shows a similar trend as the simplex interface

[Fig. 10(b)], but the absolute consumption is higher, mainly due to the larger signal swing. Even so, the proposed full-duplex interface consumes much less power than LVC MOS and can maintain its power efficiency for a large range of data rates and load capacitances. The power consumption of the full-duplex interface could be further reduced by extending the programmability of C_{S1} and C_{S2} to lower the signal amplitude. According to simulations, the power consumption of the full-duplex interface would be about 10% larger than that of the simplex interface, if the same signal amplitude would be used.

In terms of reliability, both interfaces have a BER of $< 5 \cdot 10^{-12}$ (99% confidence level, 1T bits were measured at 10 Mb/s, and no errors were detected). Fig. 11 shows the measured BER bathtub curves with the same signal amplitudes as mentioned before, where each point is obtained by measuring 1 Gbit of data: in terms of phase error, both interfaces can achieve a BER $< 10^{-9}$ over 90% of the phase. Fig. 12(a) shows the eye diagram of the simplex interface while communicating at 5 Mb/s. The recorded eye heights and widths at BER $< 10^{-9}$ are 20 mV and 0.988 UI. Fig. 12(b) shows the recorded signal between two chips of the full duplex interface. The signal for the full-duplex interface is a mix of equal-magnitude TX and RX signals and thus shows 3 levels. The RX signal can be recovered at the receiving chip after self-interference cancellation. Two chips can also communicate with each other at different data rates and phases simultaneously.

IV. CONCLUSION

Table I summarizes the measured performance and the comparison against state-of-the-art. Compared to [4]–[6], this work has a wider tunability of data rate, a lower BER, and an energy efficiency that is about $2.5\times$ to $60\times$ better, thanks to the fully dynamic and mostly passive architecture. Fig. 13 shows that the simplex interface achieves a power reduction of $2\times$ to $27\times$ compared to conventional LVC MOS with the same VDD and the same load capacitance (10 kb/s to 50 Mb/s), while the full-duplex interface achieves a power reduction of $5\times$ to $11\times$ (100 kb/s to 50 Mb/s). Also, compared to existing high-speed standards and state-of-the-art low-power interfaces, this work achieves the best efficiency.

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