Design and Analysis of a High-Efficiency All-SiC Dynamic Voltage Restorer for Wide-Range Sag/Swell Mitigation

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Design and Analysis of a High-Efficiency All-SiC Dynamic Voltage Restorer for Wide-Range Sag/Swell Mitigation

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Abstract—This paper presents the design, modeling, and simulation process of a 30-kVA dynamic voltage restorer (DVR) layout for the compensation of voltage sags and swells ranging from 0.2 to 2 p.u. of the nominal grid voltage for up to 60 s. The converter is supplied by a battery energy storage system (BESS) and reaches analytical peak efficiency above 99%, by using silicon carbide (SiC) power MOSFETs and an improved circuit architecture. The circuit topology combines a T-Type inverter and a three-phase-interleaved bidirectional dc-dc stage in a dual-dc-port structure, where most of the energy flows from/to the battery directly through the inverter, while the dc-dc stage is only enabled to handle heavy sags/swells at low battery charge. The architecture, control strategy and efficiency analysis are examined in this work, relying on a simulation workflow developed in MATLAB/Simulink. A comparison of the proposed converter design to other DVR topologies is also made to demonstrate the efficiency improvement.

Keywords—Dynamic Voltage Restorer, Power Quality, Silicon Carbide, Converter Simulation

I. INTRODUCTION

Many end-user loads on the low voltage (LV) utility grid are susceptible to power quality (PQ) issues, the most common being voltage sags and swells induced by faults on the medium voltage (MV) side [1]. These temporary voltage fluctuation on the utility side can cause electrical equipment to trip and interruption in the power supply that may cause significant malfunctions to the connected loads. Most of these disturbances are characterized by short duration (<5 s) and low magnitude (<0.5 p.u. of the nominal voltage) [2]. A solution to this issue can be the robust and fault tolerant design of the equipment or the installation of uninterruptible power supplies (UPS). Although, for high power systems, this could become very costly. Dynamic voltage restorers (DVRs), first proposed in [3], are established to be a cost-effective protection interface from voltage disturbances for sensitive loads. DVRs are designed to inject an appropriate in-phase voltage in series with the source and compensate the sags/swells, so that the load voltage is always a pure sine with nominal amplitude. The range and duration of possible voltage compensation is defined by the converter topology and power rating.

Additionally, DVRs can provide flexible operation and perform several power quality improvement functions such as voltage unbalances [4] and harmonic compensation [5, 6], by functioning as a series active power filter (APF), increasing the utilization factor for the converter.

Several different DVR topologies have been proposed during the years [7], with mainly two categories: designs without energy storage and designs with energy storage. The former type taps energy from the grid through a shunt converter connected either to the supply or the load side, whereas the latter are fed by energy stored in a dc link or an energy storage system. The DVR with integrated energy storage was proven to be the best performing solution for many applications, mainly because it is independent from the faulty grid and can provide enough active power to compensate deep sags. Although the limited availability of large-capacity energy storage solutions has hindered its widespread adoption in the past, the recent cost reduction of grid-scale energy storage has seen renewed interest in this DVR topology, based on batteries, supercapacitors, flywheels and superconductive magnets [8–10]. The battery-fed DVR is usually a two-stage circuit, with a dc-dc converter cascaded with a voltage source inverter (VSI), as depicted in Fig. 1. The bidirectional dc stage serves to keep the voltage on the dc-link constant despite the voltage variation of the BESS, which allows the inverter to always operate in the linear region.

An interesting DVR topology for sag compensation has been proposed in [11], featuring a dual-dc-port structure, where the dc-dc stage power rating can be significantly reduced, thus increasing the overall efficiency. The VSI is arranged in a T-Type layout (TT-VSI) [12], being able to tap power directly from the battery in two-level operation for most of the compensation range, or supply additional peak power processed by the dc-dc stage in three-level operation.

Fig. 1. Schematic of series-connected DVR used as a protection interface in a LV grid.

Fig. 2. Circuit schematic of the proposed dynamic voltage restorer (DVR) topology.

A main drawback in the operation of high-power DVRs is the power consumption in standby mode in both stages, since current always flows through the series transformer. This impact can be mitigated by improving the design and component selection.

All of the solutions found in the literature opt for traditional silicon (Si) IGBTs as the switching device of choice. However, SiC power MOSFETs can outperform Si IGBTs of similar rating in terms of power losses and thermal properties [13]. These advantages come together with the challenge of higher circuit integration, low-parasitic design and optimization, which can be supported by computer-aided modeling and simulation techniques.

The aim of this work is to present a design workflow for an improved DVR topology, focusing on higher efficiency and power density. Comparatively better performances are achieved by using wide-bandgap devices and an interleaved bidirectional dc stage with compact powder core inductors.

The power losses and efficiency calculation are carried out using a detailed simulation-driven approach developed in MATLAB/Simulink, which enables fast and accurate parametric study and comparison with alternative DVR topologies and switch technology. This work represents the basis for the implementation of a 30-kW prototype of DVR.

II. PROPOSED DVR LAYOUT

The proposed DVR design is represented in Fig. 2. The efficient dual-dc-port design [11] is combined with a three-phase-interleaved bidirectional dc-dc stage (3PI-DC) and uses SiC MOSFETs as power switches. The interleaved layout requires lower current rating for the switches and the inductors and overall lower conduction losses and current ripple. Additionally, it offers the possibility of fault-tolerant

operation and reconfiguration of the converter for alternative functions.

As showed in Fig. 2, the voltage on the load u^l is given by

$$u_i^l = u_i^g + u_i^s, \quad (1)$$

where u^g is the grid supply voltage and u^s is the series voltage injected by the DVR, for each phase $i = a, b, c$.

The chosen series transformer turn ratio (TR) is 1:2 with a delta-connected secondary, on the DVR side. This allows a better dc-bus voltage utilization ratio and reduces the nominal current in the DVR, while also removing triple harmonics in the injected voltage. This means that the relationship between the inverter rms line-to-line voltage $U_{LL,rms}$ and the rms injected voltage $U_{s,rms}$ is

$$U_{LL,rms} = 2 U_{s,rms}, \quad (2)$$

while the relationship between inverter rms phase current $I_{i,rms}$ and grid rms phase current $I_{i,rms}^g$ is

$$I_{i,rms} = \frac{\sqrt{3}}{2} I_{i,rms}^g. \quad (3)$$

The chosen interval of p.u. grid voltage magnitude u_{pu}^g and, subsequently, the DVR injected voltage u_{pu}^s range are

$$0.2 \leq u_{pu}^g \leq 2 \quad (4)$$

$$-1 \leq u_{pu}^s \leq 0.8 \quad (5)$$

In order to operate in the linear region for the whole compensation range,

$$U_H > \frac{4\sqrt{2}}{\sqrt{3}} \hat{U}_{s,rms} \cong 3.27 \hat{U}_{s,rms} \quad (6)$$

has to hold true. Therefore, considering a maximum rms series voltage $\hat{U}_{s,rms}$ of 230 V, a U_H of 800 V is enough to satisfy this requirement.

Fig.3. Proposed DVR control scheme.

The operation mode of the DVR changes depending on the magnitude of the sag/swell and the battery voltage U_L , which depends on the state of charge. In particular, the DVR operates in two-level mode when $0 \leq 3.27 U_{s,rms} \leq U_L$. In this condition, all the power flows directly from the battery through the inverter and the dc stage is inactive. When otherwise $U_L < 3.27 U_{s,rms} < U_H$, part of the power flows through the dc stage and the TT-VSI operates in three-level mode.

Another issue with the compensation of voltage sags in a battery-fed DVR, is the necessity to dissipate energy when the battery is fully charged. Here, the matter has been addressed by including a battery overvoltage protection (BOP) circuit which dissipates the excess energy on a power resistor. The BOP features a simple chopper layout with a PWM-controlled switch.

A. Control Strategy

Several control schemes have been proposed for DVRs. In particular, three main techniques are reported in [14, 15] namely: *pre-sag* compensation, *in-phase* compensation and *energy-optimized* compensation. The *in-phase* method has been chosen for the purpose of this study and in the simulations. In this method the voltage is compensated in phase with the grid, thus the converter mainly relies on active power injection, which is the preferred option in battery-fed DVRs. A diagram of the adopted control scheme is depicted in Fig. 3. A phase-locked loop (PLL) is synchronized with the grid voltage. In this way, the amplitude of the injected voltage is minimized, although this method does not mitigate phase jumps that could occur with voltage disturbances.

The bidirectional dc stage is controlled using a unified voltage loop, as described in [16], which ensures a smooth transition between charging and discharging of the HV dc-link. The gate signals of each leg are phase-shifted by 120° .

Since the LV dc bus voltage is variable, the standard space vector modulation (SVPWM) has to be adapted for the converter operation. An asymmetrical three-level space-vector modulation SVPWM was used here for the dual-port

inverter, similar to the one presented in [11], and is not described in detail here.

III. CONVERTER DESIGN

A. Switching Device Selection

One of the main advantages in the use of SiC MOSFETs is the combination of high-voltage rating and good reverse-conduction capability without the need for an anti-parallel diode. The unavailability of commercial common-drain SiC modules drove the choice of discrete components. This impacts the low-parasitic design and power density, and needs to be taken into account when modeling the converter power losses. The selected switch is part number NVH4L020N120SC1 1.2-kV/102-A discrete SiC MOSFET by ON Semiconductor.

B. DC-link Capacitors

The design criteria used for the design of the high voltage dc-link include: the voltage rating to withstand the full V_H , sufficient hold-up energy, and the rms current rating. The dc-link must be able to supply or absorb full power P_H for the response time needed by the control loop to regulate the voltage within the required limits [17]. Assuming a worst-case response time $T_d = 1$ ms, and a maximum voltage deviation $\Delta U_H = 50$ V, the minimum required capacitance $C_{H,min}$ value can be calculated as

$$C_{H,min} > \frac{P_H T_d}{2 U_H \Delta U_H}. \quad (7)$$

According to [18], the rms value of the capacitor rms current $I_{ch,rms}$ for a three-phase, three-level inverter can be derived from

$$I_{ch,rms} = \sqrt{\frac{3mI_{pk}^2}{4\pi} \left(\sqrt{3} + \frac{2 \cos(2\varphi)}{\sqrt{3}} \right) - \frac{3}{4} m^2 I_{pk}^2 \cos^2 \varphi}, \quad (8)$$

where it depends on the modulation index m , the phase current peak value I_{pk} and the displacement angle φ . It is worth mentioning that in the proposed topology the high-voltage dc-link is not utilized as much as it would be in a symmetric three-level topology, so this value is only used as reference. In practice, the capacitor rms current in the proposed DVR is expected to be lower. The exact value would be more time-consuming to calculate and would have to take into account both the asymmetric modulation used in the TT-VSI and the bidirectional 3PI-DC operation.

The chosen layout for the capacitor bank is therefore a combination of 22 electrolytic capacitor (220 μ F, 400V, 2 in series, 11 in parallel), providing higher energy density and 4 additional film capacitors (5 μ F, 1.1kV) to provide additional current capability and minimize the switching noise in the dc-bus. The entire bank sums up to 1.23 mF capacitance and 45.2 A rms current rating.

The low voltage dc-link, which is connected to the battery, does not require a high value capacitors bank. Therefore, 6 low value film capacitors are placed here in order to decouple the converter PCB and battery stray inductances.

C. Interleaved DC inductor Design

The design of the filter inductors for the 3PI-DC is key to the performance of the proposed DVR and impacts significantly the overall efficiency power density of the converter. Since the inductors are continuously sustaining the current ripple during the converter operation (even if the average active power transfer is zero), a lower ripple is desirable to minimize the losses at no-load conditions. This can be achieved by keeping the battery at high charge state, increasing the switching frequency or increasing the inductance value. A trade-off between maximum current ripple $\Delta I_{L,pk}$, losses and volume has been carried out, considering a maximum core temperature rise of 70°C. The maximum active power transferred by the 3PI-DC stage is equal to the peak active power flowing through the high-voltage dc-link. Simulations have shown that this corresponds to about 55% the rated power for the DVR, in the full-load scenario of a 2 p.u. voltage sag with minimum battery voltage $U_{L,min} = 470$ V, with the dc stage working in buck mode. Hence, in a 3 phase interleaved dc stage, the dc current for the n -th inductor can be calculated as

$$I_{Ln} = \frac{\hat{P}_H}{3 U_{L,min}}, \text{ where } n = 1, 2, 3. \quad (10)$$

Choosing $\Delta I_{L,pk} = 0.5 \cdot I_{Ln}$, the minimum required inductance value for the converter is 414 μ H, given by

$$L_n \geq \frac{U_H - U_{L,min}}{2 \cdot \Delta I_{L,pk} \cdot f_s} \frac{U_{L,min}}{U_H}, \quad (11)$$

and the rms inductor current $I_{Ln,rms}$ is 12.2 A, given by

$$I_{Ln,rms} = \sqrt{I_{Ln}^2 + \frac{\Delta I_{L,pk}^2}{3}}. \quad (12)$$

The use of toroidal Fe-Ni powder magnetic cores with distributed airgap ensures high saturation flux, low specific core losses and good volume index LI^2 . The designed 450- μ H inductors consist each of two stacked 58-mm toroidal cores with 42 turns of 0.1mm $\times$ 400 litz wire.

IV. MODELING AND SIMULATION

The converter layout and control scheme were simulated in MATLAB/Simulink. Table I reports the chosen design specifications for the circuit, which were used in the simulations. The voltage compensation can be observed in Fig. 4-7 for the two peak-power scenarios with low battery voltage ($U_L=500$ V). Fig. 4 reports the grid, injected and load voltage waveforms in case of a 0.2 p.u. voltage sag. Fig. 5 shows the dc-stage current and voltage waveforms at the low- and high- voltage port. The same waveforms are displayed in Fig. 6 and 7 in the case of a 2 p.u. voltage swell. The dynamic response is satisfactory, achieving complete sag/swell compensation in less than half of a fundamental cycle and no significant distortion on the load voltage. The dc-stage behavior in Fig. 5(b) and 7(b) shows the discharging/charging of the battery as U_L decreases/increases. The high-voltage dc-bus current and voltage waveforms show the bidirectional energy transfer achieved by the 3PI-DC with good dynamic

TABLE I. SIMULATION PARAMETERS

Parameter	Symbol	Value	Unit
Nominal grid voltage	$U_{g,LL}$	400	V _{rms}
DVR rated power	S_{DVR}	30	kVA
LV dc-link voltage	U_L	470-680	V
HV dc-link voltage	U_H	800	V
Switching frequency	f_s	40	kHz
Grid filter inductance	$L_{a,b,c}$	360	μ H
Grid filter capacitance	$C_{a,b,c}$	2	μ F
DC filter inductance	$L_{1,2,3}$	450	μ H
HV dc-link capacitance	C_H	1.25	mF

Fig. 4. Simulated waveforms of grid (a), DVR injected (b) and load (c) voltages during a 0.2 p.u. sag event at $U_L=500$ V.

Fig. 5. Simulated waveforms of HV dc-bus voltage and current (a), and LV dc-bus voltage and current (b) during a 0.2 p.u. sag at $U_L=500$ V.

response and ripple below 1% of the nominal U_H . The FFT analysis of the injected voltage waveforms showed that no significant distortion has been introduced on the load voltage.

Different analytical and numerical simulation tools have been used to obtain a model of the converter power losses. Methods for the fast and accurate estimation of device- and converter-level power losses were proposed, among others in [19] and [20], which are based on the condition mapping of the switch and converter operation and using electro-thermal simulation.

A similar approach was used here and a block diagram of the algorithm is reported in Fig. 8. A power loss model, created from datasheet information and numerical simulations, is used to extract averaged losses that are then

Fig. 8. Modeling flowchart for the power losses calculation of the DVR.

Fig. 6. Simulated waveforms of grid (a), DVR injected (b) and load (c) voltages during a 2 p.u. swell event at $U_L=500$ V.

Fig. 7. Simulated waveforms of HV dc-bus voltage and current (a), and LV dc-bus voltage and current (b) during a 2 p.u. swell at $U_L=500$ V.

Fig. 9. FEM analysis of the current distribution and parasitic extraction for the PCB traces of one TT-VSI phase.

Fig. 10. FEM analysis of the current distribution and parasitic extraction for the PCB traces of one TT-VSI phase.

fed to a thermal network, obtained from the packaging and heatsink geometry. The temperature calculation is then fed back to the losses model to account for thermal dependency.

A. Device Losses Modeling

The choice of discrete SiC devices makes it necessary to take into account the impact of the PCB traces and layers on the parasitic elements in the power loss calculation for the switches. In order to model this impact, the PCB layout has been exported to ANSYS Q3D for parasitics extraction using finite-element method (FEM) simulation. Fig. 9 shows part of the FEM simulation process, specifically the current density contour on the PCB traces connecting the switches on one of the TT-VSI phases.

Fig. 11. Simulated power loss for the switches S_1 - S_4 of one phase of the TT-VSI, averaged on T_s , in case of SiC MOSFETs or Si IGBTs.

Subsequently, Simulink-based circuit models were built with the extracted stray elements. The TO-247-4 package parasitics and FET capacitances were included in the model. Fig. 10 depicts the circuit model used to estimate the TT-VSI losses, including the stray inductance values extracted from the FEM analysis.

As one may notice, two different power loops (A and B) are present in the converter layout. The individual behavior of each of the devices, according to the switching sequence, needs to be modeled to obtain accurate power losses. Iterative simulations were carried out to map the conduction and switching losses over the full range of operating voltage, current and temperature and collect them in look-up tables.

B. Converter-level Modeling

A converter-level simulation output is shown in Fig. 11(a-d), with the averaged losses generated by the four switches (S_1 - S_4) of one phase in the TT-VSI. The same simulation was used to compare the losses replacing the FETs with Si IGBTs of similar rating (IKY50N120CH3 by Infineon), showing a clear performance difference due to the higher IGBT losses.

A model of the dc-stage filter inductor power losses was also included for the converter-level efficiency calculation, since it brings a significant contribution to the overall losses. The model is based on datasheet information from the core manufacturer and measurements carried out on sample

Fig. 12. Contour map of the simulated DVR power losses at different BESS voltage and output power values.

Fig. 13. Contour map of the simulated DVR efficiency at different BESS voltage and output power values.

inductors. Capacitor, connectors and gate driver power losses were not accounted for the purpose of this study.

Combining semiconductor and inductor losses, the overall converter losses and efficiency were mapped over the whole operating range with variation in output power (proportional to the sag/swell magnitude) and battery voltage and reported in Fig. 12 and Fig. 13. It can be observed that the battery state of charge influences the losses. This is due to the rising current ripple amplitude in the dc stage components as the difference $U_H - U_L$ becomes higher. It can also be noticed that, at the same battery voltage value, the losses are largely constant over the output power range, since the rms current flowing on the DVR side remains constant throughout the converter operation. The losses change at high output power, when the dc-stage is active. The peak efficiency η is estimated at 99.17% with 30 kW output power and $U_L = 680$ V.

C. Comparative Analysis

The losses calculation algorithm was used to compare three different DVR designs to the proposed one: 1) a Si IGBT-based DVR with the same topology as the proposed; 2) a traditional cascaded DVR with a 2-level VSI and dc-stage (2L+DC) and 3) a cascaded DVR with 3-level neutral-point clamped (NPC) VSI (3L+DC) and dc-stage. Both the cascaded topologies are based on SiC switches, but they include an half-bridge dc-stage instead of the interleaved layout. This means that a larger single dc-inductor had to be accounted for in the simulations. The efficiency comparison between the different circuits over the full output power range is reported in Fig. 14, when the BESS is fully charged. The efficiency difference between the 3 SiC-based topologies is

Fig. 14. Comparison of simulated DVR efficiency vs. output power for different designs at $U_L=680$ V.

Fig. 15. Simulated DVR losses breakdown vs. output power for different converter designs. Battery voltage $U_L=680$ V.

Fig. 16. Comparison of simulated DVR efficiency vs. output power for different designs at $U_L=470$ V.

Fig. 17. Simulated DVR losses breakdown vs. output power for different converter designs. Battery voltage $U_L=470$ V.

not particularly significant in this condition. This is mostly due to the low power losses on the dc-dc stage. However, the largest efficiency gap is observed between the Si- and SiC-based designs in the whole operation range. The bar plot in

Fig. 18. Rendering of the proposed DVR prototype design.

Fig. 15 reports the semiconductor power loss breakdown for the different layouts and increasing output power when $U_L=680$ V. The simulation shows that conduction losses P_c are dominant in all the designs, and slightly lower for the 2-level topology, due to fewer switches. In this condition, the inductor losses P_{ind} and dc-stage switch losses P_{dc} are minimum, due to the low voltage difference between HV dc-bus and battery. A small increase can be observed in the 2L and 3L topologies at higher output power, when the dc-stage has to process a larger power. The same efficiency comparison was reported in Fig. 16, with minimum BESS voltage $U_L = 470$ V. A larger difference is observed in this case, with the 2L and 3L converters presenting worse performance and the proposed topology still offering about 99% peak efficiency. The reason for such behavior is clearly visible in the loss breakdown of Fig. 13. As expected, the dc-stage losses are generally higher due to the larger voltage difference between dc-bus and battery. As the output power increases, the advantage of a 3PI-DC stage and the dual dc-bus topology is evident, as the dc-stage losses are limited.

D. Power Density

The efficiency gain with the chosen topology allows for a smaller, more compact design. A rendering of the proposed converter prototype with physical dimensions is depicted in Fig. 18. The whole topology could fit in a 24×30 cm PCB, including BOP circuit, dc filter inductors and dc-bus capacitors. Smaller PCBs are used for the gate drivers and control interface. A single forced-air cooling aggregate was used for thermal management. The overall calculated power density for this architecture is 3.3 kW/dm².

V. CONCLUSION

An all-SiC dynamic voltage restorer layout was proposed in this work to compensate a wide range of grid voltage fluctuations. Additionally, computer-aided design procedure was used to analyze the converter performance. The simulation results for the proposed DVR, based on the dual-dc-port layout, show a significant performance improvement

when compared to other state-of-the-art topologies. In particular, the use of SiC devices offers a substantial efficiency gain compared to Si IGBTs, which results in reduced need for cooling and extends the operational range for a battery-fed DVR in the compensation of deep sags and swells. The introduction of a 3PI-DC stage allows for further reduction of the conduction losses and enhanced power density. The modeling and simulation workflow provided detailed insight in the converter operation and performance and laid the basis for the implementation of an experimental test bench to demonstrate the DVR and validate the model. Additionally, further developments are possible in the control strategy to avoid long idle periods for the converter, which entails significant power consumption. In this respect, the possibility to repurpose the converter to perform additional grid-support functionalities, such as harmonic mitigation, is of great interest and will be explored in a future work.

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