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Maurer Computers with Single-Thread Control

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Abstract. We present the development of a theory of stored threads and their execution. The work builds upon Maurer’s theory of computer instructions and the thread algebra of Bergstra et al. The theory being developed is primarily relevant to the design of new processor architectures. We also relate Maurer’s model for computers with Turing machines, and stored threads with programs as considered in the program algebra of Bergstra et al.

Keywords: Maurer computers, thread algebra, instructions, stored threads, control threads, Turing machines, program algebra.


1 Introduction

In [11], a paper from almost 40 years ago, Maurer proposes a model for computers that is quite different from the well-known models such as pushdown automata and Turing machines (see e.g. [7]). The strength of Maurer’s model is that it is close to real computers. Computer instructions play a prominent part in his model. We use the phrase \textit{Maurer computer} for what is a computer according to Maurer’s definition of a computer.

We plan to develop an approach to design processor architectures based on Maurer computers. As a first step, we develop in the current paper a theory of stored threads and their execution. We show that a single thread can control the execution on a Maurer computer of an arbitrary finite-state thread stored in the memory of the Maurer computer, provided that the basic actions of the stored thread correspond to instructions of the Maurer computer. We demonstrate that finite-state threads of arbitrary size can be dealt with if the Maurer computer on which the execution takes place leaves the fetching of the basic actions to another Maurer computer of which the memory size is sufficient for the thread concerned.
To describe threads, we use BTA (Basic Thread Algebra), introduced in [4] under the name BPPA (Basic Polarized Process Algebra). BTA is a form of process algebra which is tailored to the description of the behaviour of deterministic sequential programs under execution. Using some kind of strategic interleaving, several single-thread controlled Maurer computers can be put in parallel, which is relevant to the design of new processor architectures. Several kinds of strategic interleaving have been elaborated in earlier work, see e.g. [5]. In this paper, a simple kind of strategic interleaving, called cyclic interleaving, is used to demonstrate that finite-state threads of arbitrary size can be dealt with by setting the fetching of basic actions apart.

A straightforward way to simulate a Turing machine by a Maurer computer clarifies that the instruction implicitly executed by a Turing machine on a test or write step must be capable of reading or overwriting the contents of any cell from the infinite number of cells on the tape of the Turing machine – the cell of which the contents is actually read or overwritten depends on the head position. In Maurer’s terminology, a test instruction has an infinite input region and a write instruction has an infinite output region. Real computers do not have such instructions. Using Maurer computers, we show that the instructions concerned can be replaced by instructions with a finite input region and a finite output region if we allow Turing machines with an infinite set of states.

We also demonstrate that there is a close connection between stored threads and PGLD programs. PGLD is one of the simpler programming languages based on PGA (ProGram Algebra) introduced in [4]. From each stored thread, a PGLD program can be extracted of which the behaviour is the thread represented by the stored thread. The PGLD program extracted from a stored thread shows hardly any difference with the stored thread. However, PGLD permits a more efficient representation of threads than the one obtained in this indirect way.

The structure of this paper is as follows. First of all, we review Maurer computers (Section 2) and Basic Thread Algebra (Section 3). Following this, we introduce an operator which allows for threads to transform the states of a Maurer computer by means of its instructions. (Section 4). After that, we enhance Maurer computers step by step till we can show that a single thread can control the execution of any stored finite-state thread (Sections 5–8). We also show that such control can be accomplished with a single control instruction (Section 9). Next, we introduce parallel composition of Maurer computers and cyclic interleaving of threads (Section 10) and demonstrate that finite-state threads of arbitrary size can be dealt with by setting the fetching of basic actions apart (Section 11). Then, we clarify some interesting points about Turing machines using Maurer computers (Section 12), and relate PGLD programs to stored threads (Section 13). Finally, we make some concluding remarks (Section 14).

2 Maurer Computers

In this section, we shortly review Maurer computers, i.e. computers as defined by Maurer in [11]. The proofs of the presented theorems can be found in [10].
A Maurer computer $C$ consists of the following components:

- a set $M$;
- a set $B$ with $\text{card}(B) \geq 2$;
- a set $S$ of functions $S : M \to B$;
- a set $I$ of functions $I : S \to S$;

and satisfies the following conditions:

- if $S_1, S_2 \in S$, $M' \subseteq M$ and $S_3 : M \to B$ is such that $S_3(x) = S_1(x)$ if $x \in M'$ and $S_3(x) = S_2(x)$ if $x \notin M'$, then $S_3 \in S$;
- if $S_1, S_2 \in S$, then the set $\{x \in M \mid S_1(x) \neq S_2(x)\}$ is finite.

$M$ is called the memory, $B$ is called the base set, the members of $S$ are called the states, and the members of $I$ are called the instructions. It is obvious that the first condition is satisfied if $C$ is complete, i.e. if $S$ is the set of all functions $S : M \to B$, and that the second condition is satisfied if $C$ is finite, i.e. if $M$ and $B$ are finite sets.

The following proposition gives an interesting characterization of the set of states of a Maurer computer.

**Proposition 1 (Characterization of the set of states).** Let $(M, B, S, I)$ be a Maurer computer, let $S_0 \in S$, and let $B_x = \{b \in B \mid \exists S \in S \cdot S(x) = b\}$ for all $x \in M$. Then $S$ is the set of all functions $S : M \to B$ such that $S(x) \in B_x$ for $x \in M$ and $\{x \in M \mid S_0(x) \neq S(x)\}$ is finite.

Let $(M, B, S, I)$ be a Maurer computer, and let $I : S \to S$. Then the input region of $I$, written $\text{IR}(I)$, and the output region of $I$, written $\text{OR}(I)$, are the subsets of $M$ defined as follows:

$$\text{IR}(I) = \{x \in M \mid \exists S_1, S_2 \in S, y \in \text{OR}(I) \cdot \forall z \in M \setminus \{x\} \cdot S_1(z) = S_2(z) \land I(S_1)(y) \neq I(S_2)(y)\},$$

$$\text{OR}(I) = \{x \in M \mid \exists S \in S \cdot S(x) \neq I(S)(x)\}.$$

$\text{OR}(I)$ is the set of all memory elements that are possibly affected by $I$; and $\text{IR}(I)$ is the set of all memory elements that possibly affect elements of $\text{OR}(I)$ under $I$. We have the following theorem about the relation between the input region and output region of an instruction.

**Theorem 1 (Input and output regions of instructions).** Let $(M, B, S, I)$ be a Maurer computer, let $S_1, S_2 \in S$, and let $I \in I$. Then $S_1 \cap \text{IR}(I) = S_2 \cap \text{IR}(I)$ implies $I(S_1) \upharpoonright \text{OR}(I) = I(S_2) \upharpoonright \text{OR}(I)$.

Both conditions in the definition of Maurer computers are necessary for Theorem 1 to hold.

We have the following theorem about the input region and the output region of the composition of two instructions.
**Theorem 2 (Composition of instructions).** Let \((M, B, S, \mathcal{I})\) be a Maurer computer, let \(I_1, I_2 \in \mathcal{I}\), and let \(J : S \to S\) be defined by \(J(S) = I_2(I_1(S))\). Then \(IR(J) \subseteq IR(I_1) \cup IR(I_2)\) and \(OR(I_1) \setminus IR(I_2) \subseteq OR(I) \subseteq OR(I_1) \cup OR(I_2)\). If \(OR(I) \cap IR(I_2) = \emptyset\), then \(IR(I_2) \subseteq IR(J)\) and \(OR(J) = OR(I_1) \cup OR(I_2)\). Moreover, if \(OR(J) = OR(I_1) \cup OR(I_2)\) and \(OR(I_1) \cap OR(I_2) = \emptyset\), then also \(IR(I_1) \subseteq IR(J)\). If \(OR(I_1) \cap IR(I_2) = \emptyset\), \(IR(I_1) \cap OR(I_2) = \emptyset\) and \(OR(I_1) \cap OR(I_2) = \emptyset\), then \(J = J'\) where \(J' : S \to S\) is defined by \(J'(S) = I_1(I_2(S))\).

We have the following theorem about the decomposition of an instruction.

**Theorem 3 (Decomposition of instructions).** Let \((M, B, S, \mathcal{I})\) be a Maurer computer, let \(I \in \mathcal{I}\), and let \(x \in OR(I) \setminus IR(I)\). Then there exist \(J_1, J_2 : S \to S\) with \(J_2(J_1(S)) = I(S)\) such that \(IR(J_1) \subseteq IR(I)\), \(IR(J_2) \subseteq IR(I)\), \(OR(J_1) = \{x\}\) and \(OR(J_2) = OR(I) \setminus \{x\}\).

Let \(C = (M, B, S, \mathcal{I})\) be a Maurer computer. Then the unit component of \(C\) is the set \(\{x \in M \mid \exists b \in B \cdot \forall S \in S \cdot S(x) = b\}\).

We have the following theorem about the existence of instructions for arbitrary input and output regions.

**Theorem 4 (Existence of instructions (1)).** Let \((M, B, S, \mathcal{I})\) be a Maurer computer, let \(Z\) be its unit component, and let \(P, Q \subseteq M\). Then there exists a function \(I : S \to S\) with \(IR(I) = P\) and \(OR(I) = Q\) iff \(P \cap Z = \emptyset\), \(Q \cap Z = \emptyset\), and \(P \neq \emptyset \Rightarrow Q \neq \emptyset\).

Let \((M, B, S, \mathcal{I})\) be a Maurer computer, let \(I \in \mathcal{I}\), let \(M' \subseteq OR(I)\), and let \(M'' \subseteq IR(I)\). Then the region affected by \(M'\) under \(I\), written \(RA(M', I)\), and the region affected by \(M''\) under \(I\), written \(AR(M'', I)\), are the subsets of \(M\) defined as follows:

\[
RA(M', I) = \{x \in IR(I) \mid AR(\{x\}, I) \cap M' \neq \emptyset\},
\]

\[
AR(M'', I) = \{x \in OR(I) \mid \exists S_1, S_2 \in S \cdot \forall z \in IR(I) \setminus M'' \cdot S_1(z) = S_2(z) \land I(S_1(x) \neq I(S_2)(x))\}.
\]

\(AR(M'', I)\) is the set of all elements of \(OR(I)\) that are possibly affected by the elements of \(M''\) under \(I\); and \(RA(M', I)\) is the set of all elements of \(IR(I)\) that possibly affect elements of \(M'\) under \(I\). We have the following theorem about the existence of instructions for arbitrary input, output and affected regions.

**Theorem 5 (Existence of instructions (2)).** Let \((M, B, S, \mathcal{I})\) be a Maurer computer with countable \(M\), let \(Z\) be its unit component, let \(P, Q \subseteq M\) with \(P \cap Z = \emptyset\), \(Q \cap Z = \emptyset\), and \(P \neq \emptyset \Rightarrow Q \neq \emptyset\), and let \(Q_x \subseteq Q\) with \(Q_x \neq \emptyset\) for each \(x \in P\). Moreover, assume that the following two conditions are satisfied:

- there exist only finitely many \(x \in M\) such that \(x \in Q_x\) for all \(y \in M \setminus \{x\}\), and \(\text{card}\{b \in B \mid \exists S \in S \cdot S(x) = b\}\) = 2;
- for all infinite \(Q_0 \subseteq \bigcup_{x \in P} Q_x\), the set \(\{x \in P \mid Q_x \cap Q_0 \neq \emptyset\}\) is either infinite or contains an element \(y\) for which the set \(\{b \in B \mid \exists S \in S \cdot S(y) = b\}\) is infinite.
Then there exists a function $I : S \rightarrow S$ with $IR(I) = P$, $OR(I) = Q$ and $AR(\{x\}, I) = Q_x$ for each $x \in P$.

Both conditions in Theorem 5 are satisfied if $\bigcup_{x \in P} Q_x$ is a finite set.

3 Basic Thread Algebra

In this section, we review BTA (Basic Thread Algebra), a form of process algebra which is tailored to the description of the behaviour of deterministic sequential programs under execution. The behaviours concerned are called threads.

In BTA, it is assumed that there is a fixed but arbitrary set of basic actions $A$. BTA has the following constants and operators:

- the deadlock constant $D$;
- the termination constant $S$;
- for each $a \in A$, a binary postconditional composition operator $\preceq a \succeq$.

We use infix notation for postconditional composition. We introduce action prefixing as an abbreviation: $a \circ p$, where $p$ is a term of BTA, abbreviates $p \preceq a \succeq p$.

The intuition is that each basic action performed by a thread is taken as a command to be processed by the execution environment of the thread. The processing of a command may involve a change of state of the execution environment. At completion of the processing of the command, the execution environment produces a reply value. This reply is either $T$ or $F$ and is returned to the thread concerned. Let $p$ and $q$ be closed terms of BTA. Then $p \preceq a \succeq q$ will proceed as $p$ if the processing of $a$ leads to the reply $T$ (called a positive reply), and it will proceed as $q$ if the processing of $a$ leads to the reply $F$ (called a negative reply).

A recursive specification over BTA is a set of equations $E = \{ X = t_X \mid X \in V \}$, where $V$ is a set of variables and each $t_X$ is a term of BTA that only contains variables from $V$. Let $t$ be a term of BTA containing a variable $X$. Then an occurrence of $X$ in $t$ is guarded if $t$ has a subterm of the form $t' \preceq a \succeq t''$ containing this occurrence of $X$. A recursive specification over BTA is guarded if all occurrences of variables in the right-hand sides of its equations are guarded or it can be rewritten to such a recursive specification using the equations of the recursive specification. In the projective limit model of BTA, which is presented in [2, 4], guarded recursive specifications have unique solutions. A thread that is the solution of a finite guarded recursive specification over BTA is called a finite-state thread. BTA with recursion has, in addition to the constants and operators of BTA, for each guarded recursive specification $E$ over BTA and each variable $X$ that occurs as the left-hand side of an equation in $E$, a constant standing for the unique solution of $E$ for $X$, which is denoted by $\langle X \mid E \rangle$. We often write $X$ for $\langle X \mid E \rangle$ if $E$ is clear from the context. It should be borne in mind that, in such cases, we use $X$ as a constant.

The projective limit characterization of process equivalence on threads is based on the notion of a finite approximation of depth $n$. When for all $n$ these
approximations are identical for two given threads, both threads are considered identical. Following [2, 4], approximation of depth $n$ is phrased in terms of a unary projection operator $\pi_n(\_ \_ )$. The projection operators are defined inductively by means of the axioms in Table 1. In this table, and all subsequent tables with axioms in which $a$ occurs, $a$ stands for an arbitrary basic action from $A$.

In the structural operational semantics, we represent an execution environment by a function $\rho : A^+ \rightarrow \{T, F\}$. We write $E$ for the set of all those functions and $B$ for the set $\{T, F\}$. Given an execution environment $\rho$ and a basic action $a$, the derived execution environment $\rho a$ is defined by $\rho a (\alpha) = \rho (\langle a \rangle \cdot \alpha)$.

The chosen representation of execution environments is based on the assumption that it depends at any stage only on their history, i.e. the sequence of basic actions processed before, whether the reply is positive or negative. This is a realistic assumption for deterministic execution environments.

The following transition relations on closed terms are used in the structural operational semantics of BTA:

- a binary relation $\langle p, \rho \rangle \xrightarrow{a} \langle p', \rho' \rangle$ for each $a \in A$ and $\rho, \rho' \in E$;
- unary relations $\langle p, \rho \rangle \downarrow$ and $\langle p, \rho \rangle \uparrow$ for each $\rho \in E$.

These transition relations can be explained as follows:

- $\langle p, \rho \rangle \xrightarrow{a} \langle p', \rho' \rangle$: in execution environment $\rho$, thread $p$ is capable of first performing basic action $a$ and then proceeding as thread $p'$ in execution environment $\rho'$;
- $\langle p, \rho \rangle \downarrow$: in execution environment $\rho$, thread $p$ is capable of terminating successfully;
- $\langle p, \rho \rangle \uparrow$: in execution environment $\rho$, thread $p$ is neither capable of performing a basic action nor capable of terminating successfully.

The structural operational semantics of BTA with recursion and projection is described by the transition rules given in Table 2. In this table, and all subsequent tables with transition rules in which $a$ occurs, $a$ stands for an arbitrary basic action from $A$. We write $\langle t \mid E \rangle$ for $t$ with, for all $X$ that occur on the left-hand side of an equation in $E$, all occurrences of $X$ in $t$ replaced by $\langle X \mid E \rangle$.

4 We write $\langle \_ \_ \_ \rangle$ for the empty sequence, $\langle d \rangle$ for the sequence having $d$ as sole element, and $\alpha \cdot \beta$ for the concatenation of sequences $\alpha$ and $\beta$. We assume that the identities $\alpha \cdot \langle \_ \_ \_ \rangle = \langle \_ \_ \_ \rangle \cdot \alpha = \alpha$ hold.
Table 2. Transition rules for BTA with recursion and projection

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$(S, \rho) \downarrow$</td>
<td>$\rho((a)) = T$</td>
</tr>
<tr>
<td>$(D, \rho) \uparrow$</td>
<td>$\rho((a)) = F$</td>
</tr>
<tr>
<td>$\langle x \subseteq a \supseteq y, \rho \rangle \xrightarrow{\rho} \langle x, \frac{\partial}{\partial a} \rho \rangle$</td>
<td>$X = t \in E$</td>
</tr>
<tr>
<td>$\langle (X</td>
<td>E), \rho \rangle \xrightarrow{\rho} \langle x', \rho' \rangle$</td>
</tr>
<tr>
<td>$\langle (\pi_{n+1}(x), \rho) \rangle \xrightarrow{\rho} \langle \pi_{n}(x'), \rho' \rangle$</td>
<td>$X = t \in E$</td>
</tr>
</tbody>
</table>

Bisimulation equivalence is defined as follows. A bisimulation is a symmetric binary relation $B$ on closed terms such that for all closed terms $p$ and $q$:

- if $B(p, q)$ and $(p, \rho) \xrightarrow{\rho} (p', \rho')$, then there is a $q'$ such that $(q, \rho) \xrightarrow{\rho} (q', \rho')$;
- if $B(p, q)$ and $(p, \rho) \downarrow$, then $(q, \rho) \downarrow$;
- if $B(p, q)$ and $(p, \rho) \uparrow$, then $(q, \rho) \uparrow$.

Two closed terms $p$ and $q$ are bisimulation equivalent, written $p \leftrightarrow q$, if there exists a bisimulation $B$ such that $B(p, q)$.

Bisimulation equivalence is a congruence with respect to all operators involved. This follows from the fact that the transition rules from Table 2 constitute a transition system specification in path format (see e.g. [1]).

Henceforth, we write $T_{\text{finrec}}$ for the set of all terms of BTA with recursion in which no constants $\langle X | E \rangle$ for infinite $E$ occur, and $T_{\text{finrec}}$ for the set of all closed terms of BTA with recursion in which no constants $\langle X | E \rangle$ for infinite $E$ occur. Moreover, we write $T_{\text{finrec}}(A)$, where $A \subseteq A$, for the set of all closed terms from $T_{\text{finrec}}$ that only contain basic actions from $A$.

4 Applying Threads to Maurer Machines

In this section, we introduce Maurer machines and add for each Maurer machine $H$ a binary apply operator $\cdot_H \cdot$ to BTA.

A Maurer machine is a tuple $H = (M, B, S, I, A, [\cdot])$, where $(M, B, S, I)$ is a Maurer computer and:

- $A \subseteq A$;
- $[\cdot] : A \rightarrow (I \times M)$.

The elements of $A$ are called the basic actions of $H$, and $[\cdot]$ is called the basic action interpretation function of $H$.

The apply operators associated with Maurer machines are related to the apply operators introduced in [6]. They allow for threads to transform states of the
associated Maurer machine by means of its instructions. Such state transformations produce either a state of the associated Maurer machine or the undefined state $\uparrow$. It is assumed that $\uparrow$ is not a state of any Maurer machine. We extend function restriction to $\uparrow$ by stipulating that $\uparrow \vDash M = \uparrow$ for any set $M$. The first operand of the apply operator $\bullet_H$ associated with Maurer machine $H = (M, B, S, I, A, \lfloor \_ \rfloor)$ must be a term from $T_{\text{finrec}}(A)$ and its second argument must be a state from $S \cup \{\uparrow\}$.

Let $H = (M, B, S, I, A, \lfloor \_ \rfloor)$ be a Maurer machine, let $p \in T_{\text{finrec}}(A)$, and let $S \in S$. Then $p \bullet_H S$ is the state from $S$ that results if all basic actions performed by thread $p$ are processed by the Maurer machine $H$ from initial state $S$. Moreover, let $(I_a, m_a) = [a]$ for all $a \in A$. Then the processing of a basic action $a$ by $H$ amounts to a state change according to the instruction $I_a$. In the resulting state, the reply produced by $H$ is contained in memory element $m_a$. If $p$ is $S$, then there will be no state change. If $p$ is $D$, then the result is $\uparrow$.

Let $H = (M, B, S, I, A, \lfloor \_ \rfloor)$ be a Maurer machine, and let $(I_a, m_a) = [a]$ for all $a \in A$. Then the apply operator $\bullet_H$ is defined by the equations given in Table 3 (for $a \in A$ and $S \in S$) and the rule given in Table 4 (for $S \in S$). We say that $p \bullet_H S$ is convergent if $\exists n \in \mathbb{N} \cdot \pi_n(p) \bullet_H S \neq \uparrow$. If $p \bullet_H S$ is convergent, then the number of computation steps of $p \bullet_H S$, written $|p \bullet_H S|$, is the smallest $n \in \mathbb{N}$ such that $\pi_n(p) \bullet_H S \neq \uparrow$. If $p \bullet_H S$ is not convergent, then $|p \bullet_H S|$ is undefined. We say that $p \bullet_H S$ is divergent if $p \bullet_H S$ is not convergent. Notice that the rule from Table 4 can be read as follows: if $x \bullet_H S$ is divergent, then it equals $\uparrow$.

We introduce some auxiliary notions, which are useful in proofs. Let $H = (M, B, S, I, A, \lfloor \_ \rfloor)$ be a Maurer machine, and let $(I_a, m_a) = [a]$ for all $a \in A$. Then the step relation $\vdash_H$ is inductively defined as follows:

- if $I_a(S)(m_a) = T$ and $p = p' \leq a \triangleright p''$, then $(p, S) \vdash_H (p', I_a(S))$;
- if $I_a(S)(m_a) = F$ and $p = p' \leq a \triangleright p''$, then $(p, S) \vdash_H (p'', I_a(S))$.

Table 3. Defining equations for apply operator

<table>
<thead>
<tr>
<th>$S \bullet_H S$</th>
<th>$S$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$D \bullet_H S$</td>
<td>$\uparrow$</td>
</tr>
<tr>
<td>$x \bullet_H \uparrow$</td>
<td>$\uparrow$</td>
</tr>
<tr>
<td>$(x \leq a \triangleright y) \bullet_H S = x \bullet_H I_a(S)$</td>
<td>if $I_a(S)(m_a) = T$</td>
</tr>
<tr>
<td>$(x \leq a \triangleright y) \bullet_H S = y \bullet_H I_a(S)$</td>
<td>if $I_a(S)(m_a) = F$</td>
</tr>
</tbody>
</table>

Table 4. Rule for divergence

| $\forall a \in \mathbb{N} \quad \pi_n(x) \bullet_H S = \uparrow$ |
|-----------------|-----|
| $x \bullet_H S = \uparrow$ |
If \((p, S) \vdash_H (p', S')\), then \(p \cdot_H S = p' \cdot_H S'\). Moreover, let \(p \in T_{\text{next}}(A)\), and let \(S \in S\). Then the full path of \(p \cdot_H S\) is the unique full path in \(\vdash_H\) from \((p, S)\).

A full path in \(\vdash_H\) is one of the following:

- a finite path \(((p_0, S_0), \ldots, (p_n, S_n))\) in \(\vdash_H\) such that there exists no \((p_{n+1}, S_{n+1}) \in T_{\text{store}}(A) \times S\) with \((p_n, S_n) \vdash_H (p_{n+1}, S_{n+1})\);

- an infinite path \(((p_0, S_0), (p_1, S_1), \ldots)\) in \(\vdash_H\).

If \(p \cdot_H S\) is convergent, then its full path is a path of length \(|p \cdot_H S|\) from \((p, S)\) to \((S, S')\), where \(S' = p \cdot_H S\). Such a full path is also called a computation.

5 Executing Stored Basic Actions

In this section, we enhance Maurer machines such that processing of a basic action performed by a thread amounts to first storing it in a special memory element and then executing the instruction associated with the basic action stored in that special memory element. That is, we extend the memory with a basic action register \((\text{bar})\) and a reply register \((\text{rr})\), and the instruction set with store instructions for each action \(a\) of the original Maurer machine \((I_{\text{store},a})\) and an execute stored basic action instruction \((I_{\text{exsba}})\). Moreover, we replace the basic actions of the original Maurer machine by basic actions with which the extra instructions are associated. The resulting Maurer machines are called SBA-enhancements. SBA stands for stored basic action.

Let \(A \subseteq A\) be such that for all \(a \in A\), \(\text{store}: a \not\in A\). Then it is assumed that \(\text{store}: a \in A\) for all \(a \in A\). Moreover, it is assumed that \(\text{exsba} \subseteq A\).

Let \(H = (M, B, S, T, A, [\ldots])\) be a Maurer machine with \(\text{bar}, \text{rr} \notin M\), \(I_{\text{store},a} \notin T\) for all \(a \in A\), \(I_{\text{exsba}} \notin T\), \(\text{store}: a \notin A\) for all \(a \in A\) and \(\text{exsba} \notin A\), and let \((I_a, m_a) = [a]\) for all \(a \in A\). Then the SBA-enhancement of \(H\) is the Maurer machine \((M', B', S', T', A', [\ldots])\) such that

\[
M' = M \cup \{\text{bar}, \text{rr}\},
\]

\[
B' = B \cup A \cup \mathbb{B},
\]

\[
S' = \{S' : M' \rightarrow B' | S' \in S \land S'(\text{bar}) \in A \land S'('rr) \in \mathbb{B}\},
\]

\[
T' = \{I' : S' \rightarrow S' | \exists I \in T \land S' \in S',
\]

\[
I'(S') \downarrow M = I(S' \downarrow M) \land I'(S') \uparrow (M' \setminus M) = S' \uparrow (M' \setminus M)
\]

\[
\cup \{I_{\text{store},a} | a \in A\} \cup \{I_{\text{exsba}}\},
\]

\[
A' = \{\text{store}: a | a \in A\} \cup \{\text{exsba}\},
\]

\[
[a]' = (I_a, \text{rr}) \text{ for all } a \in A'.
\]

Here, for each \(a \in A\), \(I_{\text{store},a}\) is the unique function from \(S'\) to \(S'\) such that for all \(S' \in S'\):

\[
I_{\text{store},a}(S') \downarrow M = S' \downarrow M,
\]

\[
I_{\text{store},a}(S')(\text{bar}) = a,
\]

\[
I_{\text{store},a}(S')(\text{rr}) = S'(\text{rr}).
\]
Theorem 6 (SBA-enhancement). Let $H$ be the transformation of $p$ by applying thread $p$ enhancements as well.

Because the memory is extended with only finitely many memory elements, it is easy to check, using Proposition 1, that an SBA-enhancement of a Maurer machine is a Maurer machine indeed. The same remark applies to all subsequent enhancements as well.

We define inductively a transformation function $\phi$ on $T_{\text{finrec}}$.

Applying thread $p$ to a state of Maurer machine $H$ has the same effect as applying the transformation of $p$ to the corresponding state of the SBA-enhancement of $H$.

Theorem 6 (SBA-enhancement). Let $H' = (M', B', S', T', A', [], []')$ be the SBA-enhancement of $H = (M, B, S, T, A, [], [])$, let $S'_0 \in S'$, and let $p \in T_{\text{finrec}}(A)$. Then $p \bullet_H (S'_0 \upharpoonright M) = (\phi(p) \bullet_H, S'_0) \upharpoonright M$.

Proof. Let $(I_a, m_a) = [a]$ for all $a \in A$, and let $(I_a, rr) = [a']$ for all $a \in A'$. It is easy to see that for all $a \in A$ and $S' \in S'$:

$$I_a(S' \upharpoonright M) = I_{\text{exsba}}(I_{\text{store}}(a)(S')) \upharpoonright M, \quad I_a(S' \upharpoonright M)(m_a) = I_{\text{exsba}}(I_{\text{store}}(a)(S'))(rr).$$

In the case where $p \bullet_H (S'_0 \upharpoonright M)$ is convergent, it is easy to prove the theorem by induction on $[p \bullet_H (S'_0 \upharpoonright M)]$, using equations (1) and (2). In the case where $p \bullet_H (S'_0 \upharpoonright M)$ is not convergent, the theorem follows immediately from the claim that $\pi_n(p) \bullet_H (S'_0 \upharpoonright M) = (\pi_{2n}(\phi(p)) \bullet_H, S'_0) \upharpoonright M$ for all $n \in \mathbb{N}$. This claim is easily proved by induction on $n$, using equations (1) and (2).

On the SBA-enhancement of a Maurer machine $H$, processing of a basic action performed by a thread $p$ amounts to first storing it in the special memory element $\text{bar}$ and then executing the instruction associated with the basic action stored in $\text{bar}$. For storing basic actions in $\text{bar}$ and executing basic actions stored in $\text{bar}$, the special basic actions $\text{store}:a$ and $\text{exsba}$ are introduced. Thus, processing can be brought under control of a variant of the thread $p$, viz. the thread obtained by applying the transformation $\phi$ to $p$.

In subsequent sections, we will introduce several other kinds of enhancement of Maurer machines based on the idea of processing of a basic action performed by a thread $p$ amounts to first storing it in a special memory element.
and then executing the instruction associated with the basic action stored in that special memory element. However, for each of those other kinds, processing can be brought under control of a single special thread. This is in most cases accomplished by storing a representation of the thread \( p \) in a part of the memory of the enhanced Maurer machine.

6 Representation of Threads

In this section, we make precise how to represent threads in the memory of a Maurer machine.

It is assumed that a fixed but arbitrary finite set \( M_t \) and a fixed but arbitrary bijection \( m : [0, \text{card}(M_t) - 1] \rightarrow M_t \) have been given. \( M_t \) is called the thread memory. We write \( \text{size}(M_t) \) for \( \text{card}(M_t) \). Let \( n, n' \in [0, \text{size}(M_t) - 1] \) be such that \( n \leq n' \). Then, we write \( M_t[n] \) for \( m_t(n) \), and \( M_t[n, n'] \) for \( \{m_t(k) \mid n \leq k \leq n'\} \).

The thread memory is a memory of which the elements can be addressed by means of elements of \([0, \text{size}(M_t) - 1]\). We write \( A_t \) for \([0, \text{size}(M_t) - 1]\).

The thread memory elements are meant for containing the representations of nodes that form part of a simple graph representation of a thread. Here, the representation of a node is either \( S \), \( D \) or a triple consisting of a basic action and two natural numbers addressing thread memory elements containing representations of other nodes.

Let \( n, n' \in A_t \) be such that \( n \leq n' \). Then, we write \( B_t[n, n'] \) for \( (\{S, D\} \cup ([n, n'] \times A \times [n, n'])\). We write \( B_t \) for \( B_t[0, \text{size}(M_t) - 1] \). \( B_t \) is called the thread memory base set. We write \( S_t \) for the set of all functions \( S_t : M_t \rightarrow B_t \).

Let \( p \in \mathcal{T}_{\text{finrec}} \). Then the nodes of the graph representation of \( p \), written \( \text{Nodes}(p) \), is the smallest subset of \( \mathcal{T}_{\text{finrec}} \) such that:

- \( p \in \text{Nodes}(p) \);
- if \( p' \trianglelefteq a \triangleright q' \in \text{Nodes}(p) \), then \( p', q' \in \text{Nodes}(p) \);
- if \( \{X_0, X_1, \ldots, X_n = t_n\} \in \text{Nodes}(p) \), \( \{t_0, \{X_0 = t_0, \ldots, X_n = t_n\}\} \in \text{Nodes}(p) \).

We write \( \text{size}(p) \) for \( \text{card}(\text{Nodes}(p)) \).

It is assumed that for all \( p \in \mathcal{T}_{\text{finrec}} \), a fixed but arbitrary bijection \( \text{node}_p : [0, \text{size}(p) - 1] \rightarrow \text{Nodes}(p) \) with \( \text{node}_p(0) = p \) has been given.

Let \( p \in \mathcal{T}_{\text{finrec}} \) be such that \( \text{size}(p) \leq \text{size}(M_t) \). Then the stored graph representation of \( p \), written \( s_t(p) \), is the unique \( s_t : M_t[0, \text{size}(p) - 1] \rightarrow B_t[0, \text{size}(p) - 1] \) such that for all \( n \in [0, \text{size}(p) - 1] \), \( s_t[M_t[n]] = \text{nrepr}_p(\text{node}_p(n)) \), where \( \text{nrepr}_p : \text{Nodes}(p) \rightarrow B_t[0, \text{size}(p) - 1] \) is defined as follows:

\[
\text{nrepr}_p(S) = S, \\
\text{nrepr}_p(D) = D, \\
\text{nrepr}_p(p' \trianglelefteq a \triangleright q') = (\text{node}_p^{-1}(p'), a, \text{node}_p^{-1}(q')), \\
\text{nrepr}_p(\{X_0 = t_0, \ldots, X_n = t_n\}) = \text{nrepr}_p(\{t_0, \{X_0 = t_0, \ldots, X_n = t_n\}\}).
\]
We call \( s_t(p) \) a stored thread.

Notice that \( s_t(p) \) is not defined for \( p \) with \( \text{size}(p) > \text{size}(M_t) \). The size of the thread memory restricts the threads that can be stored.

7 No Stored Threads, but a Single Control Thread

Before we make use of stored threads to accomplish that a single control thread is sufficient, we demonstrate in this section that this can also be accomplished without stored threads at the cost of flexibility.

We enhance Maurer machines by extending the memory with a node register (\( \text{nr} \)), a basic action register (\( \text{bar} \)) and a reply register (\( \text{rr} \)), and the instruction set with a halt instruction (\( I_{\text{halt}} \)), two fetch instructions (\( I_{\text{fetch}} \)) and an execute stored basic action instruction (\( I_{\text{exsba}} \)). Moreover, we replace the basic actions of the original Maurer machine by basic actions with which the extra instructions are associated. The resulting Maurer machines are called SBA'-enhancements.

In the definition of an SBA'-enhancement of a Maurer machine given below, \( n\text{repr}_p(n) \), where \( n \in [0, \text{size}(p) - 1] \), abbreviates \( n\text{repr}_p(\text{node}_p(n)) \).

It is assumed that \( \text{halt} \in A \), that \( \text{fetch}:r \in A \) for all \( r \in \mathbb{B} \), and that \( \text{exsba} \in A \).

Let \( H = (M, B, S, I, T, \mathbb{I}, \ldots) \) be a Maurer machine with \( \text{nr}, \text{bar}, \text{rr} \notin M \), \( I_{\text{halt}} \notin I \), \( I_{\text{fetch},r} \notin I \) for all \( r \in \mathbb{B} \), \( I_{\text{exsba}} \notin I \), \text{halt} \notin A \), \text{fetch}:r \notin A \) for all \( r \in \mathbb{B} \) and \( \text{exsba} \notin A \), and let \( (I_a, m_a) = [a] \) for all \( a \in A \). Let also \( p \in T_{\text{finite}}(A) \). Then the SBA'-enhancement of \( H \) for \( p \) is the Maurer machine \( H' = (M', B', S', I', T', \mathbb{I}', \ldots) \) such that

\[
M' = M \cup \{\text{nr}, \text{bar}, \text{rr}\},
B' = B \cup [-1, \text{size}(p) - 1] \cup A \cup \mathbb{B},
S' = \{S' : M' \rightarrow B' \mid S' \mid M \in S \land S'(\text{nr}) \in [-1, \text{size}(p) - 1] \land S'(\text{bar}) \in A \land S'(\text{rr}) \in \mathbb{B}\},
I' = \{I' : S' \rightarrow S' \mid \exists I \in I \vee S' \in S' \land I'(S') \mid M = I(S' \mid M) \land I'(S') \mid (M' \setminus M) = S' \mid (M' \setminus M)\}
\cup \{I_{\text{halt}}\} \cup \{I_{\text{fetch},r} \mid r \in \mathbb{B}\} \cup \{I_{\text{exsba}}\},
A' = \{\text{halt}\} \cup \{\text{fetch}:r \mid r \in \mathbb{B}\} \cup \{\text{exsba}\},
[a]' = (I_a, \text{rr}) \text{ for all } a \in A'.
\]

Here, \( I_{\text{halt}} \) is the unique function from \( S' \) to \( S' \) such that for all \( S' \in S' \):

\[
I_{\text{halt}}(S'(\text{nr})) = S'(\text{nr}),
I_{\text{halt}}(S'(\text{bar})) = S'(\text{bar}),
I_{\text{halt}}(S'(\text{rr})) = \mathbb{T} \text{ if } \text{node}_p(S'(\text{nr})) = S,
I_{\text{halt}}(S'(\text{rr})) = \mathbb{F} \text{ if } \text{node}_p(S'(\text{nr})) \neq S;
\]
for each \( r \in \mathbb{B} \), \( I_{\text{fetch}, r} \) is the unique function from \( S' \) to \( S' \) such that for all \( S' \in S' \):

\[
\begin{align*}
I_{\text{fetch}, r}(S') &\mid M = S' \mid M, \\
I_{\text{fetch}, r}(S')(n) &\mid n = nnn(S', r), \\
I_{\text{fetch}, r}(S')(\bar{n}) &\mid n = \pi_2(nre\pi_p(nnn(S', r))) \quad \text{if } \text{node}_p(nnn(S', r)) \notin \{S, D\}, \\
I_{\text{fetch}, r}(S')(\bar{n}) &\mid n = S'(\bar{n}) \quad \text{if } \text{node}_p(nnn(S', r)) \in \{S, D\}, \\
I_{\text{fetch}, r}(S')(\top) &\mid r = T \quad \text{if } \text{node}_p(nnn(S', r)) \notin \{S, D\}, \\
I_{\text{fetch}, r}(S')(\top) &\mid r = F \quad \text{if } \text{node}_p(nnn(S', r)) \in \{S, D\},
\end{align*}
\]

where \( nnn : S' \times \mathbb{B} \to [0, \text{size}(p) - 1] \) is defined as follows:

\[
\begin{align*}
nnn(S', \top) = \pi_1(nre\pi_p(S'(n))) &\quad \text{if } S'(n) \neq -1 \land \text{node}_p(S'(n)) \notin \{S, D\}, \\
nnn(S', F) = \pi_1(nre\pi_p(S'(n))) &\quad \text{if } S'(n) \neq -1 \land \text{node}_p(S'(n)) \notin \{S, D\}, \\
nnn(S', r) = S'(n) &\quad \text{if } S'(n) \neq -1 \land \text{node}_p(S'(n)) \in \{S, D\}, \\
nnn(S', r) = 0 &\quad \text{if } S'(n) = -1;
\end{align*}
\]

and \( I_{\text{exsba}} \) is the unique function from \( S' \) to \( S' \) such that for all \( S' \in S' \):

\[
\begin{align*}
I_{\text{exsba}}(S') \mid M &\mid M = I_{\text{exsba}(\bar{n})}(S' \mid M), \\
I_{\text{exsba}}(S')(n) &\mid n = S'(n), \\
I_{\text{exsba}}(S')(\bar{n}) &\mid n = S'(\bar{n}), \\
I_{\text{exsba}}(S')(\top) &\mid r = I_{\text{exsba}(\bar{n})}(S' \mid M)(m_{S'(\bar{n})}).
\end{align*}
\]

The node register \( n \) is meant for containing the number that corresponds to
the node of the graph representation of \( p \) from which most recently a basic action has been fetched. That node, together with the reply produced at completion of
the execution of the basic action concerned, determines the node from which next time a basic action must be fetched. To indicate that no basic action has been fetched yet, \( n \) must initially contain \(-1\). The number corresponding to the node from which the first time a basic action must be fetched, i.e. the root, is \( 0 \).

Consider the guarded recursive specification over BTA that consists of the following equations:

\[
\begin{align*}
CT &\triangleq (CT \triangleq \text{exsba} \triangleright CT') \triangleq \text{fetch:}T \triangleright (S \triangleq \text{halt} \triangleright D), \\
CT' &\triangleq (CT \triangleq \text{exsba} \triangleright CT') \triangleq \text{fetch:F} \triangleright (S \triangleq \text{halt} \triangleright D).
\end{align*}
\]

Applying thread \( p \) to a state of Maurer machine \( H \) has the same effect as applying control thread \( CT \) to the corresponding state of the SBA'-enhancement of \( H \) for \( p \).

**Theorem 7 (SBA'-enhancement).** Let \( H' = (M', B', S', T', A', \llbracket A \rrbracket') \) be the SBA'-enhancement of \( H = (M, B, S, T, A, \llbracket A \rrbracket) \) for \( p \in T_{\text{inoc}}(A) \), and let \( S_0' \in S' \) be such that \( S_0'(n) = -1 \). Then \( p \bullet_H (S_0' \mid M) = (CT \bullet_H S_0') \mid M \).
Proof. Let \((I_a, m_a) = \llbracket a \rrbracket\) for all \(a \in A\), and let \((I_a, \text{rr}) = \llbracket a' \rrbracket\) for all \(a \in A'\). Then it is easy to see that for all \(S' \in S'\) with \(\text{node}_p(\text{mn}(S', S'(r))) \notin \{S, D\}\):

\[
\begin{align*}
I_a(S' \upharpoonright M) &= I_{\text{exsba}}(I_{\text{fetch}, r}(S')) \upharpoonright M, \\
I_a(S' \upharpoonright M)(m_a) &= I_{\text{exsba}}(I_{\text{fetch}, r}(S'))(r),
\end{align*}
\]

(3)

where \(a = \pi_2(\text{mnre}^p(\text{node}_p(\text{mn}(S', S'(r)))))\) and \(r = S'(r)\).

Let \((p_n, S_n)\) be the \(n+1\)-th element in the full path of \(p \bullet_H S_0\), and let \((p'_n, S'_n)\) be the \(n+1\)-th element in the full path of \(CT \bullet_H S_0\). Then it is easy to prove by induction on \(n\) that

\[
\begin{align*}
p'_{2n+2} &= CT & \text{if } S'_{2n+1}(r) = T & \land S'_{2n+2}(r) = T \\
p'_{2n+2} &= CT' & \text{if } S'_{2n+1}(r) = T & \land S'_{2n+2}(r) = F \\
p'_{2n+2} &= S & \text{if } S'_{2n+1}(r) = F & \land S'_{2n+2}(r) = T \\
p'_{2n+2} &= D & \text{if } S'_{2n+1}(r) = F & \land S'_{2n+2}(r) = F
\end{align*}
\]

for \(2n + 2 < |CT \bullet_H S_0|\) if \(CT \bullet_H S_0\) is convergent. Moreover, using (3), (4) and (5), it is straightforward to prove by induction on \(n\) that:

- \(p_{n+1}\) is represented by the part of the graph representation of \(p\) of which the root is \(\text{node}_p(\text{mn}(S_{2n+2}, S'_{2n+2}(r)))\);
- \(S_{n+1} = S_{2n+2} \upharpoonright M\).

(for \(n + 1 < |p \bullet_H (S_0 \upharpoonright M)|\) if \(p \bullet_H (S_0 \upharpoonright M)\) is convergent). From this, the theorem follows immediately. \(\square\)

The SBA'-enhancements of a Maurer machine for different threads have different fetch instructions. That is why SBA'-enhancements are inflexible from a practical point of view: it is virtually impossible to change an instruction available on a real machine. On the other hand, it is easy to change the stored thread present in the memory of a real machine.

8 Fetching Basic Actions from a Stored Thread

In this section, we make use of stored threads to accomplish that a single control thread is sufficient.

We enhance Maurer machines by extending the memory with a thread memory (\(M_t\)), a thread location register (\(\text{tlr}\)), a basic action register (\(\text{bar}\)) and a reply register (\(\text{rr}\)), and the instruction set with a halt instruction (\(I_{\text{halt}}\)), two fetch instructions (\(I_{\text{fetch}, 1}, I_{\text{fetch}, F}\)) and an execute stored basic action instruction (\(I_{\text{exsba}}\)). Moreover, we replace the basic actions of the original Maurer machine by basic actions with which the extra instructions are associated. The resulting Maurer machines are called ST-4I-enhancements. ST stands for stored thread and 4I indicates that there are four control instructions available.

Let \(H = (M, B, S, I, A, \llbracket \_ \rrbracket)\) be a Maurer machine with \(M, \text{tlr}, \text{bar}, \text{rr} \notin M, I_{\text{halt}} \notin I, I_{\text{fetch}, r} \notin I\) for all \(r \in B, I_{\text{exsba}} \notin I, \text{halt} \notin A, \text{fetch}:r \notin A\) for all \(r \in B\) and \(\text{exsba} \notin A\), and let \((I_a, m_a) = \llbracket a \rrbracket\) for all \(a \in A\). Then the ST-4I-
enhancement of $H$ is the Maurer machine $H' = (M', B', S', I', A', [\_]'')$ such that

\[
M' = M \cup M_t \cup \{ \text{thr}, \text{bar}, \text{rr} \}, \\
B' = B \cup B_t \cup A_t \cup \{-1\} \cup A \cup B, \\
S' = \{ S' : M' \to B' \mid S' \mid M \in S \land S' \mid M_t \in S_t \land \}
\]

\[
S'(\text{thr}) \in A_t \cup \{-1\} \land S'(\text{bar}) \in A \land S'(\text{rr}) \in B, \\
I' = \{ I : S' \to S' \mid \exists I \in I' \forall S' \in S' \bullet \}
\]

\[
I'(S') \mid M = I(S' \mid M) \land I'(S') \mid (M' \setminus M) = S' \mid (M' \setminus M) \\
\]

\[
\cup \{ I_{\text{halt}} \cup \{ I_{\text{fetch}, r} \mid r \in B \} \cup \{ \text{exsba} \}, \\
A' = \{ \text{halt} \cup \{ \text{fetch}, r \mid r \in B \} \cup \{ \text{exsba} \}, \\
[a]' = (I_a, \text{rr}) \quad \text{for all } a \in A'.
\]

Here, $I_{\text{halt}}$ is the unique function from $S'$ to $S'$ such that for all $S' \in S'$:

\[
I_{\text{halt}}(S') \mid M = S' \mid M, \\
I_{\text{halt}}(S') \mid M_t = S' \mid M_t, \\
I_{\text{halt}}(S')(\text{thr}) = S'(\text{thr}), \\
I_{\text{halt}}(S')(\text{bar}) = S'(\text{bar}), \\
I_{\text{halt}}(S')(\text{rr}) = T \quad \text{if } S'(\text{thr}) = S, \\
I_{\text{halt}}(S')(\text{rr}) = F \quad \text{if } S'(\text{thr}) \neq S;
\]

for each $r \in B$, $I_{\text{fetch}, r}$ is the unique function from $S'$ to $S'$ such that for all $S' \in S'$:

\[
I_{\text{fetch}, r}(S') \mid M = S' \mid M, \\
I_{\text{fetch}, r}(S') \mid M_t = S' \mid M_t, \\
I_{\text{fetch}, r}(S')(\text{thr}) = \text{ntla}(S', r), \\
I_{\text{fetch}, r}(S')(\text{bar}) = \pi_2(S'(M_t[\text{ntla}(S', r)])) \quad \text{if } S'(M_t[\text{ntla}(S', r)]) \notin \{ S, D \}, \\
I_{\text{fetch}, r}(S')(\text{bar}) = S'(\text{bar}) \quad \text{if } S'(M_t[\text{ntla}(S', r)]) \in \{ S, D \}, \\
I_{\text{fetch}, r}(S')(\text{rr}) = T \quad \text{if } S'(M_t[\text{ntla}(S', r)]) \notin \{ S, D \}, \\
I_{\text{fetch}, r}(S')(\text{rr}) = F \quad \text{if } S'(M_t[\text{ntla}(S', r)]) \in \{ S, D \},
\]

where $\text{ntla} : S' \times B \to A_t$ is defined as follows:

\[
\text{ntla}(S', T) = \pi_1(S'(M_t[S'(\text{thr})])) \quad \text{if } S'(\text{thr}) \in A_t \land S'(M_t[S'(\text{thr})]) \notin \{ S, D \}, \\
\text{ntla}(S', F) = \pi_3(S'(M_t[S'(\text{thr})])) \quad \text{if } S'(\text{thr}) \in A_t \land S'(M_t[S'(\text{thr})]) \notin \{ S, D \}, \\
\text{ntla}(S', \text{rr}) = S'(\text{thr}) \quad \text{if } S'(\text{thr}) \in A_t \land S'(M_t[S'(\text{thr})]) \in \{ S, D \}, \\
\text{ntla}(S', r) = 0 \quad \text{if } S'(\text{thr}) \notin A_t;
\]

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and $I_{\text{exsba}}$ is the unique function from $S'$ to $S'$ such that for all $S' \in S'$:

$I_{\text{exsba}}(S') \upharpoonright M = I_{S'[(\text{bar})]}(S' \upharpoonright M)$,
$I_{\text{exsba}}(S') \upharpoonright M_k = S' \upharpoonright M_k$,
$I_{\text{exsba}}(S')(\text{thr}) = S'(\text{thr})$,
$I_{\text{exsba}}(S')(\text{bar}) = S'(\text{bar})$,
$I_{\text{exsba}}(S')(\text{rr}) = I_{S'[(\text{bar})]}(S' \upharpoonright M)(m_{S'[(\text{bar})]})$.

The thread location register $\text{thr}$ is meant for containing the address of the thread memory element from which most recently a basic action has been fetched.

The contents of that thread memory element, together with the reply produced at completion of the execution of the basic action concerned, determines the thread memory element from which next time a basic action must be fetched. To indicate that no basic action has been fetched yet, $\text{thr}$ initially contains $-1$. The thread memory element from which the first time a basic action must be fetched is the one at address $0$.

Consider again the guarded recursive specification over BTA that consists of the following equations:

$$CT = (CT \leq \text{exsba} \bowtie CT') \leq \text{fetch}:T \geq (S \leq \text{halt} \bowtie D),$$
$$CT' = (CT \leq \text{exsba} \bowtie CT') \leq \text{fetch}:F \geq (S \leq \text{halt} \bowtie D).$$

Applying control thread $p$ to a state of Maurer machine $H$ has the same effect as applying control thread $CT$ to the corresponding state of the ST-4I-enhancement of $H$ in which the thread memory contains the stored graph representation of $p$.

**Theorem 8 (ST-4I-enhancement).** Let $H' = (M', B', S', I', A', [\cdot])$ be the ST-4I-enhancement of $H = (M, B, S, I, A, [\cdot])$, let $p \in T_{\text{finrec}}(A)$ be such that $\text{size}(p) \leq \text{size}(M_k)$, and let $S'_0 \in S'$ be such that $S'_0 \upharpoonright M_k[0, \text{size}(p) - 1] = s(p)$ and $S'_0(\text{rr}) = -1$. Then $p \cdot H$ ($S'_0 \upharpoonright M) = (CT \cdot H, S'_0) \upharpoonright M$.

**Proof.** Let $(I_a, m_a) = [a]$ for all $a \in A$, and let $(I_a, \text{rr}) = [a']$ for all $a \in A'$. Then it is easy to see that for all $S' \in S'$ with $S'(M_k[\text{ntla}(S', S'(\text{rr}))) \notin \{S, D\}$:

$$I_a(S' \upharpoonright M) = I_{\text{exsba}}(I_{\text{fetch}, r}(S')) \upharpoonright M,$$
$$I_a(S' \upharpoonright M)(m_a) = I_{\text{exsba}}(I_{\text{fetch}, r}(S'))(rr),$$

where $a = \tau_2(S'(M_k[\text{ntla}(S', S'(\text{rr}))))$ and $r = S'(\text{rr})$.

Let $(p_n, S_n)$ be the $n+1$-th element in the full path of $p \cdot H$ ($S'_0 \upharpoonright M$), and let $(p'_n, S'_n)$ be the $n+1$-th element in the full path of $CT \cdot H, S'_0$. Then it is easy to prove by induction on $n$ that

$$p'_{2n+2} = CT \quad \text{if } S'_{2n+1}(\text{rr}) = T \land S'_{2n+2}(\text{rr}) = T,$$
$$p'_{2n+2} = CT' \quad \text{if } S'_{2n+1}(\text{rr}) = T \land S'_{2n+2}(\text{rr}) = F,$$
$$p'_{2n+2} = S \quad \text{if } S'_{2n+1}(\text{rr}) = F \land S'_{2n+2}(\text{rr}) = T,$$
$$p'_{2n+2} = D \quad \text{if } S'_{2n+1}(\text{rr}) = F \land S'_{2n+2}(\text{rr}) = F$$

(for $2n + 2 < |CT \cdot H, S'_0|$ if $CT \cdot H, S'_0$ is convergent). Moreover, using (6), (7) and (8), it is straightforward to prove by induction on $n$ that:
\[ p_{n+1} \text{ is represented by the part of } s_t(p) \text{ to which } n\text{itra}(S_{2n+2}^t, S_{2n+2}^t(r)) \text{ points;} \]
\[ S_{n+1} = S_{2n+2}^t \mid M. \]

(for \( n+1 < |p \bullet_H (S_0^t \mid M)| \) if \( p \bullet_H (S_0^t \mid M) \) is convergent). From this, the theorem follows immediately.

Notice that the proof of Theorem 7 and the proof of Theorem 8 follow similar lines.

The size of a stored thread may exceed the size of the thread memory of an ST-4I-enhancement. In other words, an ST-4I-enhancement cannot handle finite-state threads of arbitrary size. Section 11 shows how to get around this limitation.

9 A Universal Control Instruction

On the ST-4I-enhancements of Maurer machines, four instruction are available for controlling the processing of basic actions. In this section, we enhance Maurer machines such that a single universal control instruction becomes available. That is, we extend the memory with a \textit{thread memory} (\( M_t \)), a \textit{thread location register} (\( \text{tlr} \)), a \textit{basic action register} (\( \text{bar} \)), a \textit{reply register} (\( \text{rr} \)) and a \textit{fetch mode register} (\( \text{fmr} \)), and the instruction set with a step instruction (\( \text{step} \)). Moreover, we replace the basic actions of the original Maurer machine by a basic action with which the extra instruction is associated. The resulting Maurer machines are called \textit{ST-1I-enhancements}. ST stands again for stored thread and 1I indicates that there is one control instruction available.

It is assumed that \( \text{step} \in A \).

Let \( H = (M, B, S, I, A, [\[- \]] \) be a Maurer machine with \( M_t \notin M, \text{tlr, bar, rr, fmr} \notin M, \text{step} \notin I \) and \( \text{step} \notin A \), and let \( (I_a, m_a) = [a] \) for all \( a \in A \). Then the \textit{ST-1I-enhancement} of \( H \) is the Maurer machine \( H' = (M', B', S', I', A', [\[- \]]') \) such that

\[
M' = M \cup M_t \cup \{\text{tlr, bar, rr, fmr}\},
B' = B \cup B_t \cup A_t \cup \{-1\} \cup A \cup \mathbb{B},
S' = \{S': M' \rightarrow B' | S' \mid M \in S \land S' \mid M_t \in S_t \land S'(\text{tlr}) \in A_t \cup \{-1\} \land S'(\text{bar}) \in A \land S'(\text{rr}) \in \mathbb{B} \land S'(\text{fmr}) \in \mathbb{B}\},
I' = \{I': S' \rightarrow S' | \exists I \in I \bullet S' \in S' \bullet I'(S') \mid M = I(S' \mid M) \land I'(S') \mid (M' \setminus M) = S' \mid (M' \setminus M)\}
\cup \{\text{step}\},
A' = \{\text{step}\},
[\text{step}]' = (I_{\text{step}}, \text{rr}).
\]
Here, $I_{\text{step}}$ is the unique function from $S' \times S$ to $S'$ such that for all $S' \in S'$:

\[
\begin{align*}
I_{\text{step}}(S') \mid M'' & = I_{\text{fetch}}(S') \mid M'' & \text{if } S'('fmr') = T \land S'('rr') = r , \\
I_{\text{step}}(S') \mid M'' & = I_{\text{exsba}}(S') \mid M'' & \text{if } S'('fmr') = F \land S'('rr') = T , \\
I_{\text{step}}(S') \mid M'' & = I_{\text{halt}}(S') \mid M'' & \text{if } S'('fmr') = F \land S'('rr') = F , \\
I_{\text{step}}(S')(fmr) & = F & \text{if } S'('fmr') = T , \\
I_{\text{step}}(S')(fmr) & = T & \text{if } S'('fmr') = F ,
\end{align*}
\]

where $M'' = M \cup M_1 \cup \{\text{tlr, bar, rr}\}$ and $I_{\text{fetch}}, I_{\text{exsba}}$ and $I_{\text{halt}}$ are defined as in the definition of the ST-4I-enhancement.

Consecutive executions of the instruction step alternate between a fetch mode and an execute mode. The fetch mode register $fmr$ is meant for containing a flag that indicates whether the next time step is executed the mode is fetch mode. The contents of that register, together with the contents of the reply register, determine whether the next time step is executed actually halt, fetch: $T$, fetch: $F$ or exsba is executed.

Consider the guarded recursive specification over BTA that consists of the following equations:

\[
CT'' = (\text{step} \circ CT'') \leq \text{step} \geq (S \leq \text{step} \geq D).
\]

Notice that odd steps are actually fetch steps, which may fail because of termination or deadlock of the controlled thread. Applying thread $p$ to a state of Maurer machine $H$ has the same effect as applying control thread $CT''$ to the corresponding state of the ST-1I-enhancement of $H$ in which the thread memory contains the stored graph representation of $p$.

**Theorem 9 (ST-1I-enhancement).** Let $H' = (M', B', S', T', A', [\cdot])$ be the ST-1I-enhancement of $H = (M, B, S, T, A, [\cdot])$, let $p \in T_{\text{core}}(A)$ be such that size($p$) $\leq$ size($M_0$), and let $S_0' \in S'$ be such that $S_0' \mid M_0[0, \text{size}(p) - 1] = S(p)$, $S_0'(\text{tlr}) = -1$ and $S_0'(\text{fmr}) = T$. Then $p \bullet_H (S_0' \mid M) = (CT'' \bullet_H S_0' \mid M$.

**Proof.** The proof follows the same line as the proof of Theorem 8. In the proof, the equations corresponding to equations (6) and (7) hold only for states $S'$ with $S'(\text{fmr}) = T$. This does not stand in the way of following the same line, because this extra condition is satisfied by all states $S'$ that have to be related to the state component of an element in the full path of $p \bullet_H (S_0' \mid M)$. \qed

## 10 Parallel Maurer Machines and Interleaving of Threads

In Section 11, we will demonstrate that a Maurer machine with a fixed finite memory can deal with any finite-state thread, provided that it is put in parallel with a Maurer machine of a suitable kind that can hold the thread concerned. In this section, we introduce the parallel composition of Maurer machines. Moreover, because the control threads of the Maurer machines have to be interleaved if they are put in parallel, we add an operator for that purpose to BTA.
Table 5. Axioms for cyclic interleaving

<table>
<thead>
<tr>
<th>Axiom</th>
<th>CSI</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\parallel(\langle \rangle) = S$</td>
<td></td>
</tr>
<tr>
<td>$\parallel(\langle S \rangle \cdot \alpha) = \parallel(\alpha)$</td>
<td></td>
</tr>
<tr>
<td>$\parallel(\langle D \rangle \cdot \alpha) = S_D(\parallel(\alpha))$</td>
<td></td>
</tr>
<tr>
<td>$\parallel(\langle x \cdot a \cdot y \rangle \cdot \alpha) = \parallel(\alpha \cdot \langle x \rangle) \cdot a \cdot \parallel(\alpha \cdot \langle y \rangle)$</td>
<td></td>
</tr>
</tbody>
</table>

Table 6. Axioms for deadlock at termination

<table>
<thead>
<tr>
<th>Axiom</th>
<th>S2D</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_D(S) = D$</td>
<td></td>
</tr>
<tr>
<td>$S_D(D) = D$</td>
<td></td>
</tr>
<tr>
<td>$S_D(x \cdot a \cdot y) = S_D(x) \cdot a \cdot S_D(y)$</td>
<td></td>
</tr>
</tbody>
</table>

Let $H_i = (M_i, B_i, S_i, I_i, A_i, \llbracket \cdot \rrbracket_i)$, for $i = 1, 2$, be Maurer machines with for all $x \in M_1 \cap M_2$ either $\forall I_1 \in I_1 \cdot x \not\in OR(I_1)$ or $\forall I_2 \in I_2 \cdot x \not\in OR(I_2)$, and $A_1 \cap A_2 = \emptyset$. Then the parallel composition of $H_1$ and $H_2$, written $H_1 \parallel H_2$, is the unique Maurer machine $(M, B, S, I, A, \llbracket \cdot \rrbracket)$ such that

- $M = M_1 \cup M_2$,
- $B = B_1 \cup B_2$,
- $S = \{ S : M \to B | S \in S_1 \land S \in S_2 \}$,
- $I = I_1 \cup I_2$,
- $A = A_1 \cup A_2$,
- $\llbracket a \rrbracket_1$ if $a \in A_1$,
- $\llbracket a \rrbracket_2$ if $a \in A_2$.

Notice that the parallel composition of two Maurer machines is defined only if each common memory element is read-only for at least one of the Maurer machines. It is usual that the common memory elements do duty for communication between the parallel Maurer machines.

A thread vector is a sequence of threads. Strategic interleaving operators turn a thread vector of arbitrary length into a single thread. Several kinds of strategic interleaving have been elaborated in earlier work, see e.g. [5]. In this section, we only cover the simplest interleaving strategy, namely cyclic interleaving. The strategic interleaving operator for cyclic interleaving is denoted by $\parallel(\cdot)$.

The axioms for cyclic interleaving are given in Table 5. In CSI3, the auxiliary deadlock at termination operator $S_D(\cdot)$ is used. It turns termination into deadlock. Its axioms appear in Table 6.

The structural operational semantics of BTA extended with recursion, projection and cyclic interleaving is described by the transition rules given in Tables 2 and 7. Here $\langle x, \rho \rangle \not\to$ stands for the set of all conditions $\neg (\langle x, \rho \rangle \xrightarrow{a} \langle p', \rho' \rangle)$ where $p'$ is a closed term of this extension, $\rho' \in E$, $a \in A$.

Bisimulation equivalence is also a congruence with respect to the cyclic interleaving operator and the deadlock at termination operator. This follows imme-
such that
for all $rrr$ of which the memory size is sufficient for the thread concerned. In this section, we demonstrate that we can deal with finite-state threads of arbitrary size by means of an enhanced Maurer machine that does the execution of stored basic actions of the original Maurer machine by basic actions with which the fetch instruction is associated. The fetch register consists of a remote reply register $(rrr)$, a stop mode register $(smr)$, and an execute stored basic action instruction $(exsba)$. Moreover, this Maurer machine has a basic action with which the fetch instruction is associated. The resulting Maurer machine is called RST-enhancements. RST stands for remote stored thread.

We also introduce a Maurer machine with a memory consisting of a thread memory $(M_t)$, a thread location register $(tlr)$, a basic action register $(bar)$, a reply register $(rr)$, a remote reply register $(rrr)$, and an instruction set consisting of a halt instruction $(halt)$ and an execute stored basic action instruction $(exsba)$. Moreover, this Maurer machine has a basic action with which the fetch instruction is associated. The resulting Maurer machine is called the remote machine for stored threads.

Let $H = (M, B, S, I, A, [\cdot])$ be a Maurer machine with $M_t \not\subseteq M$, $tlr, bar, rr, rrr, smr \not\in M$, $halt \not\in I$, $fetch \not\in A$ for all $r \in B$, $exsba \not\in I$, $halt \not\in A$, $fetch \not\in A$ for all $r \in B$. Then the $RST$-enhancement of $H$ is the Maurer machine $H' = (M', B', S', I', A', [\cdot]'\{\cdot\})$.  

\begin{table}[h]
\centering
\caption{Transition rules for cyclic interleaving and deadlock at termination}
\begin{tabular}{ll}
\hline
$(x_1, \rho), \ldots, (x_{k+1}, \rho) \xrightarrow{\alpha} (x'_{k+1}, \rho')$ & (k ≥ 0) \\
\hline
$(\|((x_1) \wedge \ldots \wedge (x_{k+1}) \wedge \alpha), \rho) \xrightarrow{\|((\alpha \wedge (x'_{k+1})), \rho')}$ \\
$\vdots$ & \\
$(x_1, \rho), \ldots, (x_k, \rho), (x_{k+1}, \rho) \xrightarrow{(x'_{k+1}, \rho')}$ & (k ≥ l > 0) \\
$\|((x_1) \wedge \ldots \wedge (x_{k+1}) \wedge \alpha), \rho) \xrightarrow{\|((\alpha \wedge (x_k)), \rho')}$ \\
$\vdots$ & \\
$(x_1, \rho), \ldots, (x_k, \rho), (x_{k+1}, \rho) \xrightarrow{(x', \rho')}$ & (k ≥ l > 0) \\
$\|((x_1) \wedge \ldots \wedge (x_k), \rho')$ \\
$\vdots$ & \\
$(S_D (x), \rho) \xrightarrow{(S_D (x'), \rho')}$ & (k ≥ l > 0) \\
\hline
\end{tabular}
\end{table}

\section{Dealing with Finite-State Threads of Arbitrary Size}

In this section, we demonstrate that we can deal with finite-state threads of arbitrary size by means of an enhanced Maurer machine that does the execution of stored basic actions, but leaves the fetching of those basic actions to a remote Maurer machine of which the memory size is sufficient for the thread concerned.

We enhance Maurer machines by extending the memory with a basic action register $(bar)$, a reply register $(rr)$, a remote reply register $(rrr)$ and a stop mode register $(smr)$, and the instruction set with a halt instruction $(halt)$ and an execute stored basic action instruction $(exsba)$. Moreover, we replace the basic actions of the original Maurer machine by basic actions with which the extra instructions are associated. The resulting Maurer machines are called RST-enhancements.

We also introduce a Maurer machine with a memory consisting of a thread memory $(M_t)$, a thread location register $(tlr)$, a basic action register $(bar)$, a reply register $(rr)$, a remote reply register $(rrr)$, and a stop mode register $(smr)$, and an instruction set consisting of a fetch instruction $(fetch)$. Moreover, this Maurer machine has a basic action with which the fetch instruction is associated. The resulting Maurer machine is called the remote machine for stored threads.

Let $H = (M, B, S, I, A, [\cdot])$ be a Maurer machine with $M_t \not\subseteq M$, $tlr, bar, rr, rrr, smr \not\in M$, $halt \not\in I$, $fetch \not\in A$ for all $r \in B$, $exsba \not\in I$, $halt \not\in A$, $fetch \not\in A$ for all $r \in B$. Then the $RST$-enhancement of $H$ is the Maurer machine $H' = (M', B', S', I', A', [\cdot]'\{\cdot\})$ such that

\begin{align*}
M' &= M \cup \{bar, rr, rrr, smr\} \\
B' &= B \cup A \cup B
\end{align*}
Here, \( I_{\text{halt}} \) is the unique function from \( S' \) to \( S' \) such that for all \( S' \in S' \):

\[
I_{\text{halt}}(S') \upharpoonright M = S' \upharpoonright M ,
\]

\[
I_{\text{halt}}(S')(\text{bar}) = S'(\text{bar}) ,
\]

\[
I_{\text{halt}}(S')(\text{rr}) = S'(\text{smr}) ,
\]

\[
I_{\text{halt}}(S')(\text{rrr}) = S'(\text{rrr}) ,
\]

\[
I_{\text{halt}}(S')(\text{smr}) = S'(\text{smr}) ;
\]

and \( I_{\text{exsba}} \) is the unique function from \( S' \) to \( S' \) such that for all \( S' \in S' \):

\[
I_{\text{exsba}}(S') \upharpoonright M = I_{\text{halt}}(S'(\text{bar})) ,
\]

\[
I_{\text{exsba}}(S') \upharpoonright M = S' \upharpoonright M ,
\]

\[
I_{\text{exsba}}(S')(\text{bar}) = S'(\text{bar}) ,
\]

\[
I_{\text{exsba}}(S')(\text{rr}) = I_{\text{halt}}(S'(\text{bar}))(m_{S'(\text{bar})}) ,
\]

\[
I_{\text{exsba}}(S')(\text{rrr}) = S'(\text{rrr}) ,
\]

\[
I_{\text{exsba}}(S')(\text{smr}) = S'(\text{smr}) .
\]

Moreover, the remote machine for stored threads is the Maurer machine \( H'' = (M'', B'', S'', I'', A'', \llbracket \cdot \rrbracket'') \) such that

\[
M'' = M_t \cup \{ \text{tlr, bar, rr, rrr, smr} \} ,
\]

\[
B'' = B_t \cup A_t \cup \{ -1 \} \cup A \cup B ,
\]

\[
S'' = \{ S' : M'' \to B'' | S'' \upharpoonright M_t \in S_t \wedge S''(\text{tlr}) \in A_t \cup \{ -1 \} \wedge S''(\text{bar}) \in A \wedge S''(\text{rr}) \in B \wedge S''(\text{rrr}) \in B \wedge S''(\text{smr}) \in B \} ,
\]

\[
I'' = \{ I_{\text{fetch}} \} ,
\]

\[
A'' = \{ \text{fetch} \} ,
\]

\[
\llbracket \text{fetch} \rrbracket'' = (I_{\text{fetch}}, \text{rrr}) .
\]

Here, \( I_{\text{fetch}} \) is the unique function from \( S'' \) to \( S'' \) such that for all \( S'' \in S'' \):

\[
I_{\text{fetch}}(S'') \upharpoonright M_t = S'' \upharpoonright M_t ,
\]

\[
I_{\text{fetch}}(S'')(\text{tlr}) = \text{ntla}(S'', r) ,
\]

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\[ I_{\text{fetch}}(S')(\text{bar}) = \pi_2(S'(M, \text{ntla}(S', r))) \]
\[ I_{\text{fetch}}(S')(\text{bar}) = S'(\text{bar}) \quad \text{if } S'(M, \text{ntla}(S', r)) \notin \{S, D\}, \]
\[ I_{\text{fetch}}(S')(\text{rr}) = S'(\text{rr}) \]
\[ I_{\text{fetch}}(S')(\text{rrr}) = T \quad \text{if } S'(M, \text{ntla}(S', r)) \notin \{S, D\}, \]
\[ I_{\text{fetch}}(S')(\text{rr}) = F \quad \text{if } S'(M, \text{ntla}(S', r)) \in \{S, D\}, \]
\[ I_{\text{fetch}}(S')(\text{smr}) = T \quad \text{if } S'(M, \text{ntla}(S', r)) = S, \]
\[ I_{\text{fetch}}(S')(\text{smr}) = F \quad \text{if } S'(M, \text{ntla}(S', r)) \neq S, \]

where \( r = S'(rr) \), and where \( \text{ntla} : S'' \times B \to A_t \) is defined as in the definition of an ST-4I-enhancement.

The common memory elements of the RST-enhancement \( H' \) of a Maurer machine and the remote machine \( H'' \) for a stored thread are \text{bar}, \text{rr}, \text{rrr}, \text{smr}. The memory elements \text{bar}, \text{rr}, \text{smr} are not changed by any instructions of \( H' \) and the memory element \text{rr} is not changed by any instructions of \( H'' \). So, the parallel composition \( H' \parallel H'' \) is defined (cf. Section 10). The fetch, execute and halt instructions found here are similar to the ones of an ST-4I-enhancement. The instruction \text{fetch} has the same effect as either \text{fetch}:T or \text{fetch}:F depending on the contents of \text{rr}. The instruction \text{exsba} has no effect if \text{rrr} contains \text{F}.

Consider the guarded recursive specifications over BTA that consists of the following equations:

\[
\begin{align*}
CT' &= CT' \preceq \text{exsba} \succeq (S \preceq \text{halt} \succeq D), \\
CT'' &= CT'' \preceq \text{fetch} \succeq S.
\end{align*}
\]

\( CT' \) and \( CT'' \) are control threads for RST-enhancements of Maurer machines and remote machines for stored threads, respectively. Applying thread \( p \) to a state of Maurer machine \( H \) has the same effect as applying the cyclic interleaving of control threads \( CT' \) and \( CT'' \), starting with \( CT'' \), to the corresponding state of the parallel composition of the RST-enhancement of \( H \) and the remote machine for stored threads in which the thread memory contains the stored graph representation of \( p \).

**Theorem 10 (RST-enhancement).** Let \( H' = (M', B', S', \mathcal{T}', A', [\_]) \) be the RST-enhancement of \( H = (M, B, S, \mathcal{T}, A, [\_]) \), let \( H'' \) be the remote machine for stored threads, let \( p \in T_{\text{proc}}(A) \) be such that \( \text{size}(p) \leq \text{size}(M) \), let \( S^* \) be the set of states of \( H' \parallel H'' \), and let \( S_0^* \in S^* \) be such that \( S_0^* \mid [M][0, \text{size}(p) - 1] = s_t(p), S_0^*(\text{trl}) = -1, S_0^*(\text{rr}) = T \). Then \( p \bullet H(S_0^* | M) = \{(CT'') \cap (CT') \bullet H' \parallel H'', S_0^*) | M\} \).

**Proof.** Firstly, \( ((CT'') \cap (CT')) \) is the solution of the guarded recursive specification over BTA that consists of the following equation:

\[
CT^* = (CT' \preceq \text{exsba} \succeq CT'') \preceq \text{fetch} \succeq CT',
\]

where \( CT'' \) abbreviates \( ((CT'') \cap (S \preceq \text{halt} \succeq D)) \).
Secondly, \( H' \parallel H'' \) is the Maurer machine \( H = (M^*, B^*, S^*, I^*, A^*, [ \bot ]^*) \) such that
\[
M^* = M \cup M_t \cup \{ \text{tlr, bar, rr, rrr, smr} \}, \\
B^* = B \cup B_t \cup A_t \cup \{-1\} \cup A \cup \mathbb{B}, \\
S^* = \{ S^* : M^* \to B^* | \\
S^* \upharpoonright M \in S \land S^* \upharpoonright M_t \in S_t \land S^* (\text{tlr}) \in A_t \cup \{-1\} \land \\
S^* (\text{bar}) \in A \land S^* (\text{rr}) \in \mathbb{B} \land S^* (\text{rrr}) \in \mathbb{B} \land S^* (\text{smr}) \in \mathbb{B} \}, \\
I^* = \{ I^* : S^* \to S^* | \exists I \in I \land \forall S^* \in S^* \bullet \\
I^* (S^*) | M = I (S^* \mid M) \land I^* (S^*) \mid (M^* \setminus M) = S^* \mid (M^* \setminus M) \}
\]
\[
\bigcup \{ I_{\text{halt}}, I_{\text{fetch}}, I_{\text{exsba}} \}, \\
A^* = \{ \text{halt, fetch, exsba} \}, \\
[\text{halt}]^* = (I_{\text{halt}}, \text{rr}), \\
[\text{fetch}]^* = (I_{\text{fetch}}, \text{rrr}), \\
[\text{exsba}]^* = (I_{\text{exsba}}, \text{rrr}) .
\]
Here, \( I_{\text{halt}}, I_{\text{fetch}} \) and \( I_{\text{exsba}} \) are the extensions of the instructions \( I_{\text{halt}}, I_{\text{fetch}} \) and \( I_{\text{exsba}} \) of \( H' \) and \( H'' \) to \( S^* \) such that \( I_{\text{halt}}(S^*) \mid (M^* \setminus M') = S^* \mid (M^* \setminus M'), \)
\( I_{\text{fetch}}(S^*) \mid (M^* \setminus M') = S^* \mid (M^* \setminus M') \) and \( I_{\text{exsba}}(S^*) \mid (M^* \setminus M') = S^* \mid (M^* \setminus M'). \)

The remainder of the proof follows the same line as the proof of Theorem 8.

\[ \square \]

Variations of the way to deal with arbitrary finite-state threads presented above are possible. For example, the fetch and execute instructions could have been kept essentially the same as the ones of an ST-4I-enhancement. In that case, test instructions would have been needed to check the most recently produced reply of the other Maurer machine. Moreover, a cyclic interleaving strategy would have been needed that gives each control thread two consecutive turns.

# 12 Maurer Machines and Turing Machines

Turing machines were proposed almost 70 years ago by Turing in [13]. In this section, we relate Maurer machines and Turing machines. First of all, we show how Turing machines can be simulated by means of Maurer machines.

Assume that a fixed but arbitrary countably infinite set \( M_{\text{tape}} \) and a fixed but arbitrary bijection \( m_{\text{tape}} : \mathbb{N} \to M_{\text{tape}} \) have been given. \( M_{\text{tape}} \) is called the tape. Let \( n \in \mathbb{N} \). Then we write \( M_{\text{tape}}[n] \) for \( m_{\text{tape}}(n) \).

The tape is an infinite memory of which the elements can be addressed by means of elements of \( \mathbb{N} \). We write \( A_{\text{tape}} \) for \( \mathbb{N} \). The elements of the tape contain 0, 1 or \( \square \) (blank). We write \( B_{\text{tape}} \) for the set \( \{0, 1, \square\} \), and we write \( S_{\text{tape}} \) for the set of all functions \( S_{\text{tape}} : M_{\text{tape}} \to B_{\text{tape}} \) for which there exists an \( n \in A_{\text{tape}} \) such that for all \( m \in A_{\text{tape}} \) with \( m \geq n \), \( S_{\text{tape}}(M_{\text{tape}}[m]) = \square \).

It is assumed that test:\( s \), write:\( s \in A \) for all \( s \in B_{\text{tape}} \), and that mover, mover \( \in A \).
$TM$ is the Maurer machine $(M, B, S, T, A, [\_])$ such that

$M = M_{\text{tape}} \cup \{\text{head}, rr\}$, 
$B = B_{\text{tape}} \cup A_{\text{tape}} \cup B$, 
$S = \{S : M \rightarrow B \mid S | M_{\text{tape}} = S_{\text{tape}} \wedge S(\text{head}) \in A_{\text{tape}} \wedge S(rr) \in B\}$, 
$T = \{I_{\text{test}}, I_{\text{write}} | s \in B_{\text{tape}}\} \cup \{I_{\text{mover}}, I_{\text{movel}}\}$, 
$A = \{\text{test}, s, \text{write} : s | s \in B_{\text{tape}}\} \cup \{\text{mover}, \text{movel}\}$, 
$[a] = (I_{a}, rr)$ for all $a \in A$.

Here, for each $s \in B_{\text{tape}}$, $I_{\text{test}} : s$ is the unique function from $S$ to $S$ such that for all $S \in S$:

$I_{\text{test}} : s(S) | M_{\text{tape}} = S | M_{\text{tape}}$, 
$I_{\text{test}} : s(S)(\text{head}) = S(\text{head})$, 
$I_{\text{test}} : s(S)(rr) = T$ if $S(M_{\text{tape}}[S(\text{head})]) = s$, 
$I_{\text{test}} : s(S)(rr) = F$ if $S(M_{\text{tape}}[S(\text{head})]) \neq s$;

for each $s \in B_{\text{tape}}$, $I_{\text{write}} : s$ is the unique function from $S$ to $S$ such that for all $S \in S$ and $n \in A_{\text{tape}}$:

$I_{\text{write}} : s(S)(M_{\text{tape}}[S(\text{head})]) = s$, 
$I_{\text{write}} : s(S)(M_{\text{tape}}[n]) = S(M_{\text{tape}}[n])$ if $S(\text{head}) \neq n$, 
$I_{\text{write}} : s(S)(\text{head}) = S(\text{head})$, 
$I_{\text{write}} : s(S)(rr) = T$;

$I_{\text{mover}}$ is the unique function from $S$ to $S$ such that for all $S \in S$:

$I_{\text{mover}} : S | M_{\text{tape}} = S | M_{\text{tape}}$, 
$I_{\text{mover}} : S(\text{head}) = S(\text{head}) + 1$, 
$I_{\text{mover}} : S(rr) = T$;

and, $I_{\text{movel}}$ is the unique function from $S$ to $S$ such that for all $S \in S$:

$I_{\text{movel}} : S | M_{\text{tape}} = S | M_{\text{tape}}$, 
$I_{\text{movel}} : S(\text{head}) = S(\text{head}) - 1$ if $S(\text{head}) > 0$, 
$I_{\text{movel}} : S(rr) = T$ if $S(\text{head}) > 0$, 
$I_{\text{movel}} : S(rr) = F$ if $S(\text{head}) = 0$.

We write $S_{TM}$ and $A_{TM}$ for the set of states of $TM$ and the set of basic actions of $TM$, respectively.

A Turing thread is a constant $(X_0, [X_0 = t_0, \ldots, X_n = t_n]) \in T_{\text{finrec}}$, where $t_0, \ldots, t_n$ are terms of the form $t \triangleleft \text{test}: 0 \triangleright (t' \triangleleft \text{test}: 1 \triangleright t'')$ with $t, t'$ and $t''$ of the form write: $s \circ X$, mover $\circ X$, $X \triangleleft \text{movel} \triangleright D$ or $S$ ($s \in B_{\text{tape}}$, $X \in \{X_0, \ldots, X_n\}$).
Clearly, for each Turing machine, there is a Turing thread \( p \in \mathcal{T}_{\text{finrec}}(A_{TM}) \) such that for all \( S \in S_{TM} \), \( p \circ_{TM} S \) can simulate the computations of that Turing machine from the initial tape contents \( S \upharpoonright M_{\text{tape}} \) and initial head position \( S(\text{head}) \).

Looking at the instructions used in the simulation of Turing machines by means of a Maurer machine, we observe that the test instructions \( I_{\text{test.s.n}} \) have an infinite input region and a finite output region and that the write instructions \( I_{\text{write.s.n}} \) have a finite input region and an infinite output region. It is not difficult to see that these infinite regions are essential for the simulation of many Turing machines. However, if we expand Turing threads to threads definable by infinite recursive specifications, we can simulate all Turing machines using test and write instructions with a finite input region and a finite output region.

In order to simulate Turing machines using test and write instructions with a finite input region and a finite output region, we have to adapt the Maurer machine \( TM \). Moreover, for each Turing machine, we have to adapt the corresponding Turing thread. It happens that the Turing threads can be adapted in a uniform way.

It is assumed that \( \text{test.s.n}, \text{write.s.n} \in A \) for all \( s \in B_{\text{tape}} \) and \( n \in A_{\text{tape}} \).

\( TM' \) is the Maurer machine \( (M', B', S', A', [.]') \) such that

\[
M' = M_{\text{tape}} \cup \{\text{rr}\}, \\
B' = B_{\text{tape}} \cup \mathbb{B}, \\
S' = \{S': M' \rightarrow B' | S' \upharpoonright M_{\text{tape}} = S_{\text{tape}} \land S'(\text{rr}) \in \mathbb{B}\}, \\
I' = \{I_{\text{test.s.n}}, I_{\text{write.s.n}} | s \in B_{\text{tape}} \land n \in A_{\text{tape}}\}, \\
A' = \{\text{test.s.n}, \text{write.s.n} | s \in B_{\text{tape}} \land n \in A_{\text{tape}}\}, \\
[a]' = (I_a, \text{rr}) \text{ for all } a \in A'.
\]

Here, for each \( s \in B_{\text{tape}} \) and \( n \in A_{\text{tape}} \), \( I_{\text{test.s.n}} \) is the unique function from \( S' \) to \( S' \) such that for all \( S' \in S' \):

\[
I_{\text{test.s.n}}(S') \upharpoonright M_{\text{tape}} = S' \upharpoonright M_{\text{tape}}, \\
I_{\text{test.s.n}}(S')(\text{rr}) = \text{T} \text{ if } S'(M_{\text{tape}}[n]) = s, \\
I_{\text{test.s.n}}(S')(\text{rr}) = \text{F} \text{ if } S'(M_{\text{tape}}[n]) \neq s;
\]

for each \( s \in B_{\text{tape}} \) and \( n \in A_{\text{tape}} \), \( I_{\text{write.s.n}} \) is the unique function from \( S' \) to \( S' \) such that for all \( S' \in S' \) and \( m \in A_{\text{tape}} \):

\[
I_{\text{write.s.n}}(S')(M_{\text{tape}}[n]) = s, \\
I_{\text{write.s.n}}(S')(M_{\text{tape}}[m]) = S'(M_{\text{tape}}[m]) \text{ if } n \neq m, \\
I_{\text{write.s.n}}(S')(\text{rr}) = \text{T}.
\]

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5 We consider Turing machines with one-way infinite tape, which are as powerful as Turing machines with two-way infinite tape. We interpret the usual remark “no left move is permitted when the read-write head is at the [left] boundary” (see e.g. [9]) as “a left move leads to inaction when the read-write head is at the left boundary.”
We write $S_{TM'}$ and $A_{TM'}$ for the set of states of $TM'$ and the set of basic actions of $TM'$, respectively.

Let $\langle X_0 | E \rangle$, where $E = \{X_0 = t_0, \ldots, X_n = t_n\}$, be a Turing thread, let $i \in \{0, \ldots, n\}$, and let $k \in \mathbb{N}$. Moreover, let $T_0$ be the set of all subterms of a term $t \in \mathbb{T}_{\text{finrec}}$ for which $t_0 = t$ is derivable from $E$. Then the relation $\mathcal{H}_X = T_0 \times (\{0\} \cup \{-1\})$ is inductively defined as follows:

- if $X_i \in T_0$, then $\mathcal{H}_X = (X_i, 0)$;
- if $\mathcal{H}_X = (t, l)$, $t \leq \text{test} : s \geq t' \in T_0$ and $l \geq 0$, then $\mathcal{H}_X = (t \leq \text{test} : s \geq t', l)$;
- if $\mathcal{H}_X = (t, l)$, $t' \leq \text{test} : s \geq t \in T_0$ and $l \geq 0$, then $\mathcal{H}_X = (\text{test} : s \geq t', l)$;
- if $\mathcal{H}_X = (t, l)$, write : $s \circ t \in T_0$ and $l \geq 0$, then $\mathcal{H}_X = (\text{write} : s \circ t, l)$;
- if $\mathcal{H}_X = (t, l)$, mover \ $\circ t \in T_0$ and $l \geq 0$, then $\mathcal{H}_X = (\text{mover} \ \circ t, l + 1)$;
- if $\mathcal{H}_X = (t, l)$, $t \lessdot \text{mover} \ \geq D \in T_0$ and $l \geq 0$, then $\mathcal{H}_X = (t \lessdot \text{mover} \ \geq D, l - 1)$.

We write $X_0 \xrightarrow{k_E} X_i$ to indicate that there exist a $t \in \mathbb{T}_{\text{finrec}}$ such that $t_0 = t$ is derivable from $E$ and $\mathcal{H}_X = (t, k)$ holds. The recursive specification $\psi(E)$ is inductively defined as follows:

- if $X_0 \xrightarrow{k_E} X_i$, then $X_{ik} = t_{ik} \in \psi(E)$,
  where $t_{ik}$ is obtained from $t_i$ by applying the following replacement rules:
  - $\text{test} : s$ is replaced by $\text{test} : s \cdot k$;
  - $\text{write} : s \circ X_j$ is replaced by $\text{write} : s \cdot k \circ X_{jk}$;
  - $\text{mover} \ \circ X_j$ is replaced by $X_{jl}$, where $l = k + 1$;
  - if $k \neq 0$, then $X_j \leq \text{move} \ \geq D$ is replaced by $X_{jl}$, where $l = k - 1$;
  - if $k = 0$, then $X_j \leq \text{move} \ \geq D$ is replaced by $D$.

We write $\psi(\langle X_0 | E \rangle)$ for $\langle X_{00} | \psi(E) \rangle$.

The variables of a Turing thread $p$ correspond to the states of a Turing machine. If the head position is made part of the instructions, a different copy of a state is needed for each different head position that may occur when the Turing machine enters that state. The variables of $\psi(p)$ correspond to those new states. That is, applying Turing thread $p$ to a state of Maurer machine $TM$ has the same effect as applying $\psi(p)$ to the corresponding state of Maurer machine $TM'$.

**Theorem 11 (Role of head position in Turing machines).** Let $p$ be a Turing thread, and let $S_0 \in S_{TM}$ be such that $S_0(\text{head}) = 0$. Then $(p \bullet_{TM} S_0) \upharpoonright (M_{\text{tape}} \cup \{rr\}) = \psi(p) \bullet_{TM'} (S_0 \upharpoonright (M_{\text{tape}} \cup \{rr\}))$.

**Proof.** It is easy to see that for all $S \in S_{TM}$:

\[
\begin{align*}
I_{\text{test} : s}(S) \upharpoonright (M_{\text{tape}} \cup \{rr\}) & = I_{\text{test} : s \cdot n}(S \upharpoonright (M_{\text{tape}} \cup \{rr\})) , \\
I_{\text{write} : s}(S) \upharpoontright (M_{\text{tape}} \cup \{rr\}) & = I_{\text{write} : s \cdot n}(S \upharpoontright (M_{\text{tape}} \cup \{rr\})) , \\
I_{\text{mover}}(S) \upharpoontright M_{\text{tape}} & = S \upharpoontright M_{\text{tape}} , \\
I_{\text{move} \ \geq D}(S) \upharpoontright M_{\text{tape}} & = S \upharpoontright M_{\text{tape}} ,
\end{align*}
\]

where $n = S(\text{head})$. 

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Let \((p_n, S_n)\) be the \(n+1\)-th element in the full path of \(p \cdot TM S_0\) of which the first element equals \(S\), \(D\) or \(q \sqsubseteq test:0 \sqsupseteq r\) for some \(q, r \in \mathcal{F}\), and let \((p'_n, S'_n)\) be the \(n+1\)-th element in the full path of \(\psi(p) \cdot TM' (S_0 | (\mathcal{M}_{tape} \cup \{rr\}))\) of which the first element equals \(S\), \(D\) or \(q' \sqsubseteq test:0:k \sqsupseteq r'\) for some \(k \in \mathcal{A}_{tape}\) and \(q', r' \in \mathcal{F}\). Then, using the above equations, it is straightforward to prove by induction on \(n\) that:

\[\begin{align*}
& p_{n+1} = q \sqsubseteq test:0 \sqsupseteq r \text{ and } S_{n+1}(head) = k \iff p'_{n+1} = q' \sqsubseteq test:0:k \sqsupseteq r' \text{ with } q' \text{ and } r' \text{ obtained from } q \text{ and } r \text{ by applying the replacement rules given in the definition of } \psi \text{ above}; \\
& S_{n+1} | (\mathcal{M}_{tape} \cup \{rr\}) = S'_{n+1}.
\end{align*}\]

(for \(n+1 < |p \cdot TM S_0|\) if \(p \cdot TM S_0\) is convergent). From this, the theorem follows immediately.

Consider the Turing thread \(\langle X_0 | E \rangle\), where

\[E = \{ X_0 = write:1 \circ X_1 \sqsubseteq test:0 \sqsupseteq (write:0 \circ X_1 \sqsubseteq test:1 \sqsupseteq S), \]

\[X_1 = mover \circ X_0 \sqsubseteq test:0 \sqsupseteq (mover \circ X_0 \sqsubseteq test:1 \sqsupseteq mover \circ X_0) \}.
\]

Clearly, \(X_0 \xrightarrow{E} X_0\) for each \(k \in \mathbb{N}\). Consequently, in this case \(\psi(E)\) is a countably infinite set. We conclude the following concerning Turing machines:

- the instruction implicitly executed by a Turing machine on a test step has an infinite input region and a finite output region;
- the instruction implicitly executed by a Turing machine on a write step has a finite input region and an infinite output region;
- these instructions can be replaced by instructions with a finite input region and a finite output region if we allow Turing machines with an infinite set of states.

13 Stored Threads and Programs

In this section, we discuss the connection between stored threads and programs. First, we review the program notation PGLD [4], which is close to existing assembly languages.

In PGLD, it is assumed that there is a fixed but arbitrary set of basic instructions \(\mathcal{I}\). PGLD has the following primitive instructions:

- for each \(a \in \mathcal{I}\), a positive test instruction \(+a\);
- for each \(a \in \mathcal{I}\), a negative test instruction \(-a\);
- for each \(a \in \mathcal{I}\), a void basic instruction \(a\);
- for each \(k \in \mathbb{N}\), an absolute jump instruction \(\#\#k\).

PGLD programs have the form \(u_1; \ldots; u_n\) where \(u_1, \ldots, u_n\) are primitive instructions of PGLD.

The intuition is that the execution of a basic instruction \(a\) may modify a state and produces a Boolean value at its completion. In the case of a positive
test instruction $+a$, basic instruction $a$ is executed and execution proceeds with the next primitive instruction if $T$ is produced and otherwise the next primitive instruction is skipped and execution proceeds with the primitive instruction following the skipped one. In the case where $T$ is produced and there is not at least one subsequent primitive instruction and in the case where $F$ is produced and there are not at least two subsequent primitive instructions, termination occurs. In the case of a negative test instruction $-a$, the role of the produced Boolean value is reversed. In the case of a void basic instruction $a$, the produced Boolean value is disregarded: execution always proceeds with the next primitive instruction (if present). The effect of an absolute jump instruction $##k$ is that execution proceeds with the $k$-th instruction of the program concerned. If $##k$ is itself the $k$-th instruction, then inaction (deadlock) occurs. If $k$ equals 0 or $k$ is greater than the length of the program, termination occurs.

We write $P_{\text{PGLD}}$ for the set of all PGLD programs.

The behaviour of a PGLD program, as defined in [4], is a thread which is definable by a finite guarded recursive specification over BTA. It is easy to see that each finite guarded recursive specification over BTA can be translated to a PGLD program of which the behaviour is the solution of the finite guarded recursive specification concerned (cf. Section 5 of [3]).

Next, we consider the stored threads from Section 6 again. We write $ST$ for $\{s_p \mid p \in T_{\text{finrec}} \land \text{size}(p) \leq \text{size}(M_t)\}$. We define a translation function $pgld : ST \rightarrow P_{\text{PGLD}}$ for stored threads. For all $T \in ST$, $pgld(T) = pgld'(T, 0)$, where $pgld' : ST \times \mathbb{N} \rightarrow P_{\text{PGLD}}$ is recursively defined as follows:

$$
pgld'(T, n) = pgld''(T, n) \quad \text{if } T(M_t[n+1]) \notin \text{dom}(T),
$$

$$
pgld'(T, n) = pgld''(T, n); pgld'(T, n + 1) \quad \text{if } T(M_t[n+1]) \in \text{dom}(T),
$$

where $pgld'' : ST \times \mathbb{N} \rightarrow P_{\text{PGLD}}$ is defined as follows:

$$
pgld''(T, n) = +a; ##3n'+1; ##3n''+1 \quad \text{if } T(M_t[n]) = (n', a, n''),
$$

$$
pgld''(T, n) = ##0; ##0; ##0 \quad \text{if } T(M_t[n]) = S,
$$

$$
pgld''(T, n) = ##3n+1; ##3n+2; ##3n+3 \quad \text{if } T(M_t[n]) = D.
$$

The function $pgld$ transforms addresses of thread memory elements containing representations of nodes to absolute jump instructions taking the line that each representation of a node is mapped to three primitive instructions. For that reason, $S$ and $D$ are mapped to three primitive instructions.

It can be shown that, for all $p \in T_{\text{finrec}}$ with $\text{size}(p) \leq \text{size}(M_t)$, the behaviour of $pgld(s_p(p))$ is the thread described by $p$. The function $pgld$ shows that there is hardly a difference between the stored thread $s_p(p)$ and the PGLD program $pgld(s_p(p))$ extracted from it; $s_p(p)$ can also be viewed as a stored representation of $pgld(s_p(p))$ with three primitive instruction to a memory element. However, it is likely that $pgld(s_p(p))$ contains needless jump instructions. For example, what can be achieved by a positive test instruction $+a$ followed by two identical jump instructions can also be achieved by a void basic instruction $a$. In other words, PGLD permits a more efficient representation of threads than the one obtained by way of $s_p$ and $pgld$.  

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In view of the above, a thorough investigation into stored PGLD programs and their execution looks to be worthwhile. Because the behaviour of a PGLD program is a thread which is definable by a finite guarded recursive specification over BTA, it will be easy to define a counterpart of the apply operator from Section 4 for PGLD programs. It will be trivial to make precise how to represent PGLD programs in the memory of a Maurer computer. It will be straightforward to define counterparts of ST-4I-enhancements, ST-1I-enhancements and RST-enhancements for PGLD programs. It will be relatively involved to prove counterparts of Theorems 8, 9 and 10. Therefore, we leave these matters as a whole for future work.

An interesting feature of PGLD is that PGLD programs are close to terms of PGA (Program Algebra); and a mapping has been defined by which they can be turned into terms of PGA (see e.g. [4]). Using the axioms of PGA, programs can be simplified algebraically. For example, chained jumps can be removed and thus the size of the program can be reduced.

14 Conclusions

We have developed a theory which covers basic issues concerning stored threads and their execution. Coverage of more advanced issues relevant to the design of processor architectures, primarily pipelining, is now within reach. That would enable us to formalize recent ideas intended to speed up processors, such as micro-threading [8], and to prove or disprove anticipated speed-up results.

We are not aware of other theoretical work on stored threads and their execution that builds on a model for computers as close to real computers as Maurer’s model. It happens that thread algebra fits in with Maurer computers very well. This comes as a mild surprise because Maurer computers were not at all within our sight at the time thread algebra was developed.

References