High-accuracy charge-redistribution SC video bandpass filter in standard CMOS

Citation for published version (APA):

DOI:
10.1109/4.701233

Document status and date:
Published: 01/01/1998

Document Version:
Publisher’s PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:
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Abstract—A differential switched-capacitor recursive bandpass filter is presented based on a charge-redistribution technique. The center frequency is 4.286 MHz with a quality factor of 16, and the sampling frequency is 25.7 MHz. It is specifically intended for the high-frequency deemphasis of SECAM TV video signals. The active capacitors are realized using only a sandwich construction of poly-metal1–metal2. A dual-input single-stage telescopic OTA is proposed, which has a very high current efficiency. The filter behavior is very linear, and achieves a dynamic range of 79 dB for 1% third-order intermodulation. The power consumption is only 4 mW for a 5-V supply voltage, and is realized in 0.75 mm² in a standard 0.8-μm double-metal digital CMOS process.

Index Terms—Bandpass filters, CMOS analog integrated circuits, operational transconductance amplifiers, switched-capacitor circuits, video.

I. INTRODUCTION

SWITCHED-CAPACITOR (SC) circuits are known to be well suited to the realization of filters with high dynamic range and accurate amplitude and phase characteristics. Particularly for video applications, the large signal handling capability of SC circuits is a big plus point together with their ability to create linear-phase filters [1]–[3]. Similarly, they can be used in high-frequency adaptive equalizers to reduce intersymbol interference in the read channels of storage media [4], [5].

For high-frequency applications, SC N-path structures [6]–[9], [15] and different forms of parallelism [10], [22] can be applied to increase the speed of operation of the circuits and reduce the requirements of the amplifiers with respect to dc gain and bandwidth. Another technique proposed for high sample frequencies is the use of op-amps with a precisely known gain [11]. In this way, it is possible to adjust the capacitor ratios in the SC filter design to take account of the finite gain of the op-amp.

For analog sampled data processing in standard digital CMOS, switched-current (SI) filters are a subject of continuing research, where no capacitance process option is needed for the creation of accurate filter functions [13]. SC filters have also been examined in the past for standard digital CMOS, where gate–oxide capacitance has been used to create sampling capacitors [14]. However, these oxide capacitors require a separate biasing arrangement and show signal dependency.

II. SYSTEM LEVEL CONSIDERATIONS

One of the most critical circuit blocks needed in a multistandard TV color decoder is the Cloche video BPF for demodulation of the French/East European TV standard, SECAM (sequential couleur à mémoire) [16], [17]. Two separate FM-modulated color subcarriers are used in the SECAM TV system to carry the color information which is transmitted on a TV line-sequential basis. On one TV line, the blue color difference information is transmitted on a subcarrier of nominal frequency 4.25 MHz, whereas on the following TV line, the red color difference information is transmitted on a color subcarrier of nominal frequency 4.406 MHz. The luminance information, on the other hand, is transmitted in...
the same way from line to line, and has a bandwidth of 0 to a maximum of 6 MHz. Both signals are transmitted together as one composite TV signal. Before the addition of the two signals, however, high-frequency preemphasis is applied to the chrominance using a second-order $LC$ notch filter. This preemphasis filter is designed so that it keeps the color subcarrier amplitude, and thereby its visibility, low in desaturated or dark areas of the picture, while at the same time keeping the noise immunity of the signal high in the bright and saturated areas. Since the chrominance is FM modulated, the group delay “distortion” produced in the transmitter must be undone or equalized by the high-frequency deemphasis filter in the chrominance path of the SECAM demodulator. This is the main function of the Cloche BPF.

The required specifications of an integrated Cloche video BPF under all operating conditions can be summarized as follows:

- $F_o = 4.286$ MHz ($\pm 20$ kHz), the center frequency;
- $Q = 36 \pm 1$, the quality factor;
- full signal-handling capability for differential video signals (2 $V_{pp}$ nominal, extending to 5 $V_{pp}$, worst case).

The last point mentioned implies that a 5-V supply voltage ($V_{DD}$) is required if no input attenuation is to be applied.

### III. Filter Architecture

The most popular method for designing recursive SC bandpass filters is based on the Fleischer and Laker SC biquad [18]. Even for high-frequency applications, the SC biquad is often used [10], [11]. The center frequency of the SC biquad BPF generally depends on a set of capacitor ratios which cannot be made accurately enough to satisfy the tight requirements of the Cloche BPF. Moreover, the biquad contains two SC amplifiers within a second-order loop. Another proposal for high-$Q$ BPF’s is the coupled SC resonator which contains two SC integrators in a closed loop [12]. Such a structure requires a large power consumption to be able to settle between clock periods. For a high-$Q$ video BPF with accurate center frequency in a CMOS process with no capacitor option, a simpler approach is needed.

To this end, a recursive comb filter structure was chosen for this application based on a pseudo-$N$-path technique with four (passive) multiplexed feedback paths. The filter algorithm is illustrated conceptually in Fig. 1, where the sampling frequency $F_s$ is related to the center frequency $F_o$ by $F_s = 6 \times F_o$, i.e., 25.716 MHz in the case of the Cloche BPF. In this filter, $F_o$ depends primarily on the chosen clock, whereas the $Q$ factor only depends on a simple capacitor ratio via the damping coefficient $\beta$. Poles are placed exactly at frequencies $\pm F_o$ and $3 \times F_o$, assuming that all feedback paths in Fig. 1 are equal, the total filter transfer function $H(z)$ is given by

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = (1 - \beta^2) \times \frac{1}{1 + \beta^2 z^{-2}}$$

(1)

where

$$\beta = e^{-(\pi F_o/2 F_s)}.$$  (2)

The group delay transfer function $\tau_g$ of this recursive sampled-data BPF is found from

$$\tau_g(\omega) = -\frac{d}{d(\omega T)} \arg[H(\omega T)]$$

$$= -\frac{3 \beta^2 \omega}{1 + \beta^2 + 2 \beta \cos(3 \omega T)}$$

(3)

where $T = 1/F_s$. The maximum group delay at $F_o = F_s/6$ can be derived as

$$\tau_{g \text{MAX}} = \frac{3 \beta^2 \omega}{1 - \beta^2}.$$  (4)

Note that the group delay is exactly symmetrical with respect to the center frequency since the center frequency is the pole frequency at $F_o$, with further poles appearing at exact multiples of $2 F_o$ in the positive and negative frequency directions.

The frequency spectrum of the incoming SECAM video signal is sketched in Fig. 2(a), together with the frequency

Fig. 2. Spectrum of (a) the video input signal and (b) the Cloche BPF response.
response of the sampled-data Cloche BPF in Fig. 2(b). It can be seen that, because of the superimposed luminance signal in the chrominance channel which can extend from 0 to 6 MHz, the Cloche BPF at 4.286 MHz should avoid intermodulation between the wanted chrominance and the unwanted luminance.

The filter represented in Fig. 1 is not a direct “three-path” filter in the sense that $z \rightarrow z^3$, in what is termed a left half-plane transformation [8], [15] through the multiplexing of three similar highpass filters of the form $(1 - 3^2)/(1 + 3^2 z^{-2})$. In the filter presented here, only the feedback path needs to be multiplexed, where four paths are required to realize a delay of three sample periods. This has an important advantage with respect to unwanted aliasing resulting from any path mismatch since in a direct three-path filter, aliasing of frequencies occurs at $F_o + \delta f$ back to $F_o - \delta f$ and vice versa. Hence, with any path mismatch, aliasing of in-band frequencies occurs in the direct three-path BPF. On the other hand, in this pseudo-four-path realization with a multiplexed feedback path, aliasing of out-of-band frequencies only occurs back to in-band frequencies in the BPF. For example, frequency components at $F_o/2$, $2F_o$, and $5F_o/2$ fold to $F_o$ due to any path mismatch. This filter architecture offers the possibility of reducing any aliasing due to capacitor mismatch by prefiltering. Prefiltering has no effect on in-band aliasing in a direct three-path BPF solution. For a video Cloche BPF, only luminance frequencies around $F_o/2$ are of any concern. In addition, any clock feedthrough noise peaks appear out of band at multiples of $3F_o/2$, which are outside the video baseband, and thus are not visible in terms of fixed pattern noise on the television screen.

**IV. CHARGE-REDISTRIBUTION SC DESIGN**

The SC Cloche BPF is intended for an embedded application, and so a differential realization was chosen for reasons of increased noise immunity. A simplified schematic illustrating the SC Cloche BPF is given in Fig. 3 [19]. There are four differential sequentially clocked filter paths with clock phases $\phi_1 - \phi_4$ corresponding to the filter algorithm of Fig. 1. To demonstrate the functionality of the SC BPF and because of the symmetry of the differential halves, one side of the SC BPF is redrawn in Fig. 4 for two antiphase filters paths. Each path employs an input sampling capacitor $C_0$ and a
negative output sampling capacitor $C_b$. Initially, per path, $C_a$ samples $V_{in}^+$ and $C_b$ samples $V_{out}^-$ onto their respective bottom plates. Three clock periods later, $C_a$ is placed in parallel with $C_b$ across the operational transconductance amplifier (OTA), with their bottom plates attached to $V_+^+$ and their top plates connected to the negative input of the OTA. The charge on $C_a$ and $C_b$ redistributes across the combination of $C_a$ and $C_b$ in parallel, producing the damping factor $\beta$ of (2). There is no charge transfer through the discharging of input sampling capacitors via the virtual earth node of the OTA to the OTA feedback capacitors. This means that a high loop-gain can be achieved with this filter construction compared to a standard charge-transfer technique [18].

Using the principle of charge conservation between clock cycles, the charge transfer equation becomes

$$V_{in}^+[-3] \cdot C_a - V_{out}^+[-3] \cdot C_b = V_{out}^+[-3] \cdot (C_a + C_b). \tag{5}$$

Rearranging, and equating $V_{out}^-$ with $-V_{out}^+$, the $z$-domain transfer can be obtained from

$$V_{out}^+(z) \cdot (C_a + C_b) + V_{out}^+(z) \cdot z^{-3} \cdot C_b = V_{in}^+(z) \cdot z^{-3} \cdot C_a \Rightarrow
V_{out}^+(z) = \frac{C_a}{C_a + C_b} \cdot \frac{V_{in}^+(z)}{1 + \frac{C_b}{C_a + C_b} \cdot z^{-3}}. \tag{6}$$

Apart from the three sample period delay of the input signal, (6) agrees with the transfer function of (1). $F_o$ is directly tied to the sampling frequency $F_s$ where $F_o = F_s/6$, guaranteeing a very accurate center frequency. In addition, the quality factor $Q$ is only determined by the ratio of $C_b$ to $(C_a + C_b)$, where from (2)

$$Q = -\frac{\pi}{6 \cdot \ln(\beta)}. \tag{7}$$

The damping factor $\beta$ is given by

$$\beta = \left(\frac{C_b}{C_a + C_b}\right)^{1/3}. \tag{8}$$

Note that, using this technique of charge redistribution, unity transfer gain is guaranteed at the center frequency $F_o$. This is an advantage when optimizing for dynamic range in the video signal path. Full range video signals can be processed by the BPF without any need for input attenuation which would only reduce the overall signal-to-noise ratio. For the Cloche BPF with $Q = 16$ and $F_o = 4.286$ MHz, it follows from (2) that $\beta = 0.9678$. From (8), $C_b = C_a \times \beta^3 / (1 - \beta^3)$, giving $C_b = 9.633 \times C_a$.

The feedback attenuation factor $f_b$ represents how much of the output signal is fed back to the virtual summing point at the OTA input. For the SC Cloche BPF, $f_b$ is given by

$$f_b = \frac{C_a + C_b}{C_a + C_b + C_{Pm}}. \tag{9}$$

Here, $C_{Pm}$ is the effective input capacitance of the OTA plus the top plate capacitances of $C_a$ and $C_b$ together with the junction capacitances of the switches. Since there is no extra signal capacitor at the OTA input as would be the case for a charge-transfer technique, $f_b$ can be very high for this filter construction. In this respect, it was permissible to use poly-metal1–metal2 sandwich capacitors for $C_a$ and $C_b$, and still achieve a high-speed filter circuit suitable for video frequencies. The bottom-plate capacitance of these capacitors is about 0.7 times the active capacitance. Assuming an external load capacitance $C_L$ at the output of the Cloche BPF, the closed-loop bandwidth $F_{CL}$ can be written as

$$F_{CL} = \frac{1}{2\pi} \cdot \left(\frac{gm}{(C_a + C_b) \cdot (1 - f_b) + C_L} \cdot f_b\right). \tag{10}$$

where $gm$ is the transconductance of the OTA. A dominant one-pole response is assumed here, which is typical of single-stage OTA’s. The capacitors are chosen principally out of matching and $kT/C$ noise considerations. In the realization of the Cloche BPF, $C_a$ has an effective value of 271.2 fF, while $C_b$ has an effective value of 2628 fF. The OTA $gm$ is nominally 4.6 mA/V. The external load capacitance $C_L$ has been extracted to be 10.2 pF. The closed-loop bandwidth $F_{CL}$ can be calculated to be 44 MHz, where the feedback factor $f_b$ was established to be 0.65. Equivalently, the circuit has a nominal settling time-constant of 3.5 ns, which is lower than strictly necessary for this design. However, extra margin was built into the design to account for slow process parameters, high die temperatures, slewing, and clock overlap times [9], [15], [20], [21].

V. AMPLIFIER DESIGN

Single-stage OTA’s are frequently used in high-frequency SC applications. The OTA determines to a large extent the overall performance of the SC circuit. One of the most common forms of single-stage OTA is known as the telescopic OTA [23], [24]. The simple structure of the telescopic OTA gives an essentially first-order step response, which is highly desirable. For similar reasons, it has low noise compared to more complicated OTA configurations such as the folded-cascode OTA [15], [26]. It is also power efficient since it uses almost all of the available bias current for the charging and discharging of the load capacitance. In this section, the standard telescopic OTA will be reviewed, and a new type of OTA, the dual-input telescopic OTA, will be introduced which improves on the basic telescopic OTA for differential
SC circuits. The application of this new OTA in the SC video BPF will also be described.

A. Conventional Approach: Single-Input Telescopic OTA

The most straightforward amplifier technique for SC applications is the single-input telescopic OTA (SITO), which is essentially a differential pair with a cascoded output stage. An example of an SITO with a PMOS input stage is illustrated in Fig. 5. It is configured as a high-speed double-sampling sample-and-hold [22]. For this discussion, an NMOS input stage could also be chosen, but the advantage of a PMOS input stage is that it enables the use of a low reference voltage (Ref), and hence the use of NMOS-only switches. Switches with relatively small aspect ratios can be used, which results in smaller clock feedthrough, particularly when low-value signal capacitors are needed.

Since the SITO gives a predominantly first-order response, the gain–bandwidth product (GBW) of the SITO is given by the unity-gain transition frequency

$$\text{GBW}_{\text{SITO}} = \frac{gm_p}{2\pi C_L}. \quad (11)$$

Here, $gm_p$ is the transconductance of the input stage, and $C_L$ is the defined load capacitance at the output. The second important parameter of the OTA is the open-loop dc gain $A_0$. For the SITO, $A_0$ is given by

$$A_{0\text{SITO}} = gm_p \times (\rho_{OP}||\rho_{ON}) \quad (12)$$

where $\rho_{OP}$ and $\rho_{ON}$ are the small-signal output resistances looking back into the PMOS side and NMOS side, respectively. Typically, for a good design, $\rho_{OP}$ is made approximately equal to $\rho_{ON}$.

The SITO is used frequently in high-frequency SC designs because of its low power consumption, and proposals have been made for optimizing the dimensioning of such an OTA to achieve the best speed and gain for a given application [24]. Furthermore, methods have been proposed to improve the bandwidth and gain of the SITO such as the use of a wide-band voltage preamplifier stage [2], [27]. Typically, such a preamplifier boosts the input signal by a factor of about 2, depending on the power supply used and the size of the signal to be processed. However, now, an extra pole is introduced which depends on the input capacitance of the SITO. This is another reason for limiting the amount of preamplifier gain in this application since the stability of the closed-loop amplifier is adversely affected by and the settling response becomes sensitive to process and temperature variations.

B. Proposed Approach: Dual-Input Telescopic OTA

The approach proposed here for improving amplifier bandwidth and gain is a dual-input telescopic OTA (DITO), and is based on a single amplifier topology. The use of the DITO is illustrated in Fig. 6, which is once again a high-speed sample-and-hold stage. The DITO is created by the splitting up of the NMOS current source (transistors $M_N$ and $M'_N$) of the SITO so that it acts as an NMOS input differential pair, and the further addition of a current source which is slotted in below the NMOS differential pair. For comparison, similar device geometries are assumed as for the SITO of Fig. 5.
Fig. 6. Dual-input telescopic OTA (DITO) in double-sampling sample-and-hold configuration.

The sample-and-hold feedback capacitors $C$ are split in two between the top and bottom halves of the DITO. The sample-and-hold functionality is now mirrored between the top half of the OTA with a PMOS input stage ($M_P, M'_P$) and the bottom half of the OTA with an NMOS input stage ($M_N, M'_N$).

A few points can be made about the design of the DITO. The indicated dc tail current $I$ is effectively used twice in the DITO, once for the $P$-input stage and once for the $N$-input stage. Since the device geometries are the same as those of the SITO of Fig. 5, the GBW of the DITO becomes

$$\text{GBW}_{\text{DITO}} = \frac{g_{m_P} + g_{m_N}}{2\pi C_L}$$  \hspace{1cm} (13)

where $C_L$ is the same defined load capacitance as for the SITO. Practically, the DITO gives a factor of 2 improvement in GBW for the same bias current $I$. Since the addition of the two extra transistors can be interpreted in the same way as the doubling of the aspect ratio of the $P$-input transistors, the net result is a power saving of 50% when compared to the SITO under the same load conditions. At first sight, it may appear that the slew rate is halved with respect to the SITO since the bias current is only half that of the SITO for the same load capacitance. However, the maximum current that the SITO can draw or deliver to its load is $I/2$ due to the class A output stage, and this is the same as for the DITO.

A further consequence of the doubling of the input transconductance for the same bias current of the DITO is that the open-loop dc gain is also doubled

$$A_{0,\text{DITO}} = (g_{m_P} + g_{m_N}) \times (r_{op}||r_{on})$$  \hspace{1cm} (14)

A graphical summary of the improvements of the DITO over that of the SITO is presented in Fig. 7. Only the open-loop bandwidth ($F_{OL}$) of both the SITO and the DITO is the same for similar biasing and device dimensions, where

$$F_{OL} = \frac{1}{2\pi C_L \times (r_{op}||r_{on})}.$$  \hspace{1cm} (15)

C. Amplifier Noise and Signal Range

In order to calculate the noise contribution of the SITO, the single-ended equivalent noise model can be used as indicated in Fig. 8(a). The two important noise contributors are the input transistor $M_P$, via rms noise voltage $\eta_P$, and the current source transistor $M_N$, via rms noise voltage $\eta_N$ [28]. All other transistors produce either common-mode noise (tail current) or relatively low noise that can be neglected (cascodes).
The total equivalent thermal noise variance referred to the OTA input is given by

$$\overline{v_n^2}_{\text{eqSITO}} = 2 \cdot \left( \frac{g_{m_P}^2 \cdot v_n^2 + g_{m_N}^2 \cdot v_n^2}{g_{m_P}^2} \right)$$

where the factor of 2 arises from the differential operation of the OTA.

Assuming $g_{m_P} = g_{m_N}$, then the total equivalent input noise variance for both differential OTA’s becomes

$$\overline{v_n^2}_{\text{eqSITO}} = 4 \cdot \overline{v_n^2}_p,$$

whereas

$$\overline{v_n^2}_{\text{eqDITO}} = \overline{v_n^2}_p.$$  \hspace{1cm} (18)

From this, it can be concluded that the DITO produces a quarter of the noise power of the SITO, assuming that similar load capacitance, transistor geometries, and biasing currents are used.

Heuristically, the DITO can be envisaged as the folding down of the top half of the SITO to the bottom half and vice versa. The net result is that, for each differential output, there is a current source of $I/2$ connected between $V_{DD}$ and the output, and another current source of $I/2$ connected between the output and $V_{SS}$. These current sources then do nothing else except increase the power consumption of the OTA by 50% and quadruple the noise power produced by the OTA, and so they may be discarded.

One of the problems often quoted with regard to the SITO is the required shift in common-mode level between input and output [2], [24], [27]. Considering the $P$-input SITO illustrated in Fig. 5 and assuming, say, that a single PMOS cascode stage is used, then the output level cannot go any higher than the input common-mode level plus $|V_{TP} - V_{DSSP}|$, where $V_{TP}$ is the PMOS threshold voltage and $V_{DSSP}$ is its saturation voltage. Hence, if the same common-mode voltage level is to be used for the input and the output of the SITO, the maximum signal range is just $\pm |V_{TP} - V_{DSSP}|$ in order to ensure that the OTA maintains output compliance. Thus, even for a 5 V CMOS process, where $V_{TP}$ is on the order of 1 V, the maximum signal range is only on the order of $\pm 0.7$ V.

For the DITO, on the other hand, the input and output common-mode levels can be made the same (at $Ref\,Com$) and independent of the input common-mode levels of the $P$-input and $N$-input transistor pairs, namely, $Ref\,P$ and $Ref\,N$. Say, for instance, that single cascode PMOS and NMOS stages are used in the DITO; then the maximum signal range is

$$V_{MAX} = \pm (Ref\,P + V_{TP} - V_{DSSP} - Ref\,N + V_{TN} - V_{DSSN}).$$  \hspace{1cm} (19)

The choices of $Ref\,P$ and $Ref\,N$ determine the common-mode input levels of the $P$-input and $N$-input stages, where

$$Ref\,N \geq V_{TN} + 2 \cdot V_{DSSN}$$

and

$$Ref\,P \leq V_{DD} - V_{TP} - 2 \cdot V_{DSSP}$$

in order to ensure that the input transistors and the tail-current sources remain in saturation for proper operation. Hence, the maximum signal voltage swing becomes

$$V_{MAX} = \pm (V_{DD} - 3 \cdot V_{DSSP} - 3 \cdot V_{DSSN}).$$  \hspace{1cm} (21)

Note that this is the maximum voltage swing that can be processed safely by SC circuits based on the DITO. Considering, for instance, the sample-and-hold circuit of Fig. 6, the inputs and outputs can be regarded intuitively as being on a sliding potentiometer, sliding up and down between $Ref\,P$ and $Ref\,N$. Through the use of $Ref\,P$ and $Ref\,N$ in this way, the complete circuit can be regarded as having one virtual common-mode reference voltage, namely, $Ref\,Com$.

In practice, the maximum voltage swing will not be determined by the OTA, but by the switches. For instance, for a 5 V supply, when the signal voltage goes above about 3.5 V, the NMOS switch resistance becomes prohibitively large, limiting the processing of high-frequency signals. For supply voltages of 5 V, it is permissible to use PMOS switches in combination with NMOS switches, where there is sufficient overlap of the switch resistance characteristics to enable effective rail-to-rail switch operation. This is often unattractive, though, because of the extra clocks and clock lines that are needed for realization, as well as the extra parasitic capacitance of the switches.
D. SC BPF Amplifier

The amplifier used in the design of the SC video BPF is based on the DITO and is shown in Fig. 9. Only two differential antiphase filter paths are shown for ease of illustration. The active signal capacitors $C_a$ and $C_b$ of Fig. 3 are each split in two between the top and bottom halves of the OTA, so that there is a mirroring of the functionality of the SC BPF for the top half of the OTA with a PMOS input stage as for the bottom half with an NMOS input stage. The $P$ and $N$ inputs have been designed in such a way that the $g_m$’s of both inputs are about the same and also that the input capacitance of each stage is about the same. Any mismatch between the top and bottom halves, however, is, in principle, not important since it was shown in Section V-B that both $P$ and $N$ inputs work in unison with respect to the input and output signals. The settling performance is determined by the parallel combination of the $P$ and $N$ sides of the OTA. The $P$ inputs are dimensioned as seven parallel strips, each of value $30/1$, giving a total $W/L$ of $210/1$ for each PMOS input transistor. The $N$ inputs, in turn, are dimensioned as four parallel strips of $30/1.6$, giving a total $W/L$ of $120/1.6$ for each NMOS input transistor. The nominal tail currents of the OTA are set at $600 \mu A$. This results in $g_{m_P}$ being $2.2 \text{ mA/V}$, whereas $g_{m_N}$ is $2.4 \text{ mA/V}$, and hence, the total effective transconductance becomes $4.6 \text{ mA/V}$. A feedback factor of almost $0.7$ was simulated for this OTA after having extracted all unwanted parasitic capacitances. This is very high considering that only poly-metal1–metal2 sandwich capacitors are used to achieve a high-$Q$ video BPF, and can be attributed to the charge-redistribution technique used for the filter architecture.

Only NMOS switches were used in this design. As will be demonstrated in Section VI, $C_{q}$ is split in two, with each half having its own set of switches. Similarly, each capacitor $C_b$ is split into 18 subcapacitors, each with its own set of switches. Transistors of size $6/0.8$ were used for those switches switching at $Ref P$ and at the input and output voltage levels, whereas switches of only $3/0.8$ were used for those switches switching at $Ref N$. Double PMOS cascoding was used in order to balance up the output resistances looking back into the PMOS and NMOS sides. The biasing of all of the cascodes was implemented using a form of replica biasing [2]. The reference voltages $Ref P$ and $Ref N$ were chosen as $3$ and $1.2$ V, respectively. Simulations showed that the dc gain of the OTA remained above $70$ dB for a voltage swing of $6 \text{ V}_{\text{pp}}$. Note that $Ref P$ could have been chosen as high as $3.5$ V, but because only NMOS switches were used, this would have required the use of too large switches for an acceptable “on” resistance.
Fig. 10. Cloche BPF amplifier with SC common-mode feedback circuit.

E. Common-Mode Feedback

A switched-capacitor common-mode feedback (CMFB) has been adopted for the DITO [2], [29], as depicted in Fig. 10. Double sampling is used whereby, in each clock cycle, the output common-mode voltage $V_{CM} = (V_{CM+} + V_{CM-})/2$ is sampled onto two oxide capacitors in parallel; this common voltage is then integrated onto an oxide capacitor $C_{int}$. The voltage on $C_{int}$ is compared to the common-mode reference level $RefCom$ via a small auxiliary differential pair. Only about half of the $N$-input tail current is determined by the CMFB circuit, while the rest is determined by a fixed current source. This was done to reduce the settling time constant of the CMFB with respect to the differential-mode circuit, and so ensure stability of the CMFB. The CMFB circuitry occupies only about 15% of the area of the total OTA circuitry.

VI. CHIP LAYOUT

An experimental test IC has been realized in a standard 0.8 μm, double-metal, single-poly CMOS process. A photograph of the IC is shown in Fig. 11. For proper interfacing for the sake of testing, an input track-and-hold (T&H) is used to directly sample the input video signal, while a sample-and-hold (S&H) output buffer is placed after the Cloche BPF for external probe measurements. The clock circuitry as well as the necessary voltage references have all been integrated. The essential approach to the layout of the BPF is depicted in Fig. 12 for the top half of the filter only. This, in fact, represents the positive input side to the OTA, with the negative input side having a similar construction. It was noted in Section V that the capacitors $Ca$ and $Cb$ are split in two between the top and bottom halves of the OTA, i.e., the $P$ and $N$ inputs. Furthermore, each capacitor $Ch/2$ is split into nine subcapacitors and laid out with respect to each capacitor $Ca/2$ as illustrated in Fig. 12. These individual subcapacitors
have their own set of switches so that the environment for the capacitor $C_a/2$ is imitated for each of the nine subcapacitors of $C_b/2$ for improved matching with process variations. It was mentioned in Section IV that $C_a$ has an effective capacitance of 271.2 fF, so that each individual capacitor $C_a/2$ has a value of 135.6 fF, whereas $C_b$ has a value of 2628 fF, giving each subcapacitor of $C_b$ a value of 146 fF or $1.077 \times C_a/2$. The subcapacitors of $C_b$ are constructed so that their area capacitance and edge capacitance are scaled by 1.077 with respect to $C_a/2$. Precautionary measures were taken in the design to help reduce pick-up from substrate feedthrough [30]. Separate analog and digital supplies are used, as well as replica biasing for the OTA’s. An $N$ well connected to a reference is placed under each capacitor for shielding. The area of the SC Cloche BPF is 0.75 mm$^2$. It was estimated that, had a double-poly capacitor option been available, the area of the filter would only have been about 0.2 mm$^2$ in 0.8-μm CMOS.

VII. MEASUREMENT RESULTS

In this section, the typical measurement results are presented from 12 randomly chosen test chips which were bonded from one wafer. These measurements were made for a 5-V supply voltage at room temperature. With the clock frequency set at six times the nominal center frequency, i.e., 25.716 MHz, the center frequency was measured as 4.283 MHz ($-0.07\%$ error), while the $Q$ was measured as 15.8 compared to the design value of 16 ($-1.25\%$ error). The all-important group delay characteristic has been measured on a network analyzer, and is displayed in Fig. 13. The peak group delay at $F_c$ was calculated in (4) to be $3\beta P/(1 - \beta^2)$, which for $\beta = 0.9678$ becomes $29 \times T$. However, this calculation does not include the three clock period delay required for the realization of the SC Cloche BPF, as noted in (6), plus also the two extra clock delays due to the T&H and the S&H in the measurement path. Hence, the total delay at $F_c$ should be $34 \times T$. With $T = 1/F_s = 38.9$ ns, the total measured group delay including the five clock period phase delay should be 1322 ns. The network analyzer performs a simple differentiation of the phase characteristic of the Cloche filter, and returned a peak group delay value of 1.29 $\mu$s.

The measured bandpass transfer characteristics are shown in Fig. 14 for five clock frequencies ranging from 6 to 30 MHz. It can be seen that the center frequencies remain fixed at 1/6 of the clock frequency, while the $Q$ remains relatively constant at around 16, only being dependent on a simple capacitor ratio. For the higher sampling frequencies, the transconductance of the OTA and the switch resistances play an increasing role in the incomplete settling of the filter between clock periods which help to reduce the $F_c$ and $Q$ of the filter. The full sample-and-hold characteristic is visible for a clock frequency of 6 MHz in the frequency span shown. Fig. 15 shows the resultant noise spectrum at the test IC output after 10 000 averages on a spectrum analyzer. The peak noise spectral density was measured as 177 nV/$\sqrt{Hz}$, which also includes the noise produced by the T&H, the S&H, and the active measurement probe in the measurement path. Note that the averaging process accounts for the slight discrepancy with respect to the noise reported in [19] which was measured on an analog spectrum analyzer.
The intermodulation performance can be seen in Fig. 16, where 1% intermodulation (IM3) was measured for two input signals at a level of 13.1 dBm (or 2.85 V_{pp}) with 40 kHz separation. The total noise was measured as 118 nV_{rms}, which means that the filter dynamic range becomes 79 dB for 1% IM3. The dominant clock feedthrough was at a frequency of half the input reference clock frequency, and was measured to be about 1 mV_{pp}. The maximum output voltage was 6 V_{pp} before the required specifications of the Cloche BPF were no longer achieved.

Aliasing was measured by injecting frequencies at $F_0/2$ and $2F_0$ and measuring their output at $F_0$. Aliasing levels of less than $-55$ dB were measured at $F_0$, which is more than adequate for this application.

The Cloche BPF can also be characterized via its impulse response. This is illustrated in Fig. 17. Effectively, a pulse of 0110 is applied at the input. After each period of the output waveform, the amplitude falls off with a factor of $e^{-\pi/Q}$. Hence, the $Q$ factor can obtained by dividing successive amplitudes ($P_1$, $P_2$) to give

$$Q = -\frac{\pi}{\ln \frac{P_2}{P_1}}.$$  \hspace{1cm} (22)

The attenuation of the impulse response is just $(1 - \beta^3)$ or about $-20$ dB. The center frequency of the Cloche BPF can also be ascertained via the measured impulse response. Ignoring the initial ac-coupling “bounce” effect, this can be done by examining the rotation of the sampling clock moments from one crossover point to the next, and comparing this to the resonance frequency of the impulse response. It was possible in this way to confirm the Cloche BPF center frequency as 4.283 MHz.

Finally, the functional performance of the SC Cloche BPF was tested using a SECAM video signal as input. In Fig. 18, the response of the Cloche BPF to a video frequency sweep of 3.9–4.5 MHz can be seen. The preemphasis characteristic in the transmitter is equalized by the receiver integrated Cloche filter. No attenuation is needed at the input, with the Cloche filter being able to accommodate the full video input signal.

A summary of the performance measurements on the SC Cloche BPF is presented in Table I.

VIII. CONCLUSIONS

This work shows the feasibility of designing a switched-capacitor video bandpass filter in standard digital CMOS which can achieve accurate specifications for center frequency and filter bandwidth. In spite of the large amount of parasitic capacitance that must be charged and discharged each clock cycle, big gains in signal bandwidth can be achieved through
the choice of a charge–redistribution filter architecture. The low noise and high linearity of the bandpass filter can be attributed to the uncomplicated structure chosen, in which there is only one signal transfer between the input and the output of the filter. Furthermore, the use of a single-stage dual-input telescopic OTA is highly efficient in terms of power consumption, and helps to keep the noise low. The filter can handle signals up to 6 VPP for a 5-V supply voltage, and is suitable for the processing of video signals which can have large variations in signal amplitude.

ACKNOWLEDGMENT

The author is grateful to N. Boudewijns of the Systems Laboratory Eindhoven and Prof. A. van Roermund of the Delft University of Technology for valuable discussions.

TABLE I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Measured Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC Technology</td>
<td>0.8 μm CMOS - no options</td>
</tr>
<tr>
<td>Area BPF</td>
<td>0.75 mm²</td>
</tr>
<tr>
<td>Supply</td>
<td>Single 5V</td>
</tr>
<tr>
<td>Clock Freq for Cloche BPF</td>
<td>6 x 4.286 MHz = 25.716 MHz</td>
</tr>
<tr>
<td>( F_0 )</td>
<td>4.283 MHz</td>
</tr>
<tr>
<td>( Q )</td>
<td>15.8</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>4 mW</td>
</tr>
<tr>
<td>Noise spectral density @ ( F_0 )</td>
<td>177 nV/√Hz</td>
</tr>
<tr>
<td>Max Output</td>
<td>6VPP</td>
</tr>
<tr>
<td>CMRR @ ( F_0 )</td>
<td>56 dB</td>
</tr>
<tr>
<td>PSRR @ ( F_0 )</td>
<td>32 dB</td>
</tr>
<tr>
<td>Dynamic Range (1% IM3)</td>
<td>79 dB</td>
</tr>
</tbody>
</table>

REFERENCES


Patrick J. Quinn (M’93) was born in Dublin, Ireland, in 1965. He received the B.E. degree in electronic engineering from University College Dublin (UCD) in 1986. In 1989, he received the M.Eng.Sc. degree from UCD based on the design of a direct conversion radio receiver for mobile applications.

Since 1986, he has been working for the Philips Semiconductors Systems Laboratory, Eindhoven, The Netherlands. He is currently a member of the Video Signal Processing Group, where he is leading a project in the design of sampled-data systems for video and sound processing.