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van Veldhoven, R.H.M.; Minnis, B.J.; Hegt, J.A.; van Roermund, A.H.M.

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A 3.3-mW $\Sigma\Delta$ Modulator for UMTS in 0.18-μm CMOS With 70-dB Dynamic Range in 2-MHz Bandwidth

Robert H. M. van Veldhoven, Brian J. Minnis, Senior Member, IEEE, Hans A. Hegt, Senior Member, IEEE, and Arthur H. M. van Roermund, Senior Member, IEEE

Abstract—A quadrature fourth-order, continuous-time, $\Sigma\Delta$ modulator with 1.5-b quantizer and feedback digital-to-analog converter (DAC) for a universal mobile telecommunication system (UMTS) receiver chain is presented. It achieves a dynamic range of 70 dB in a 2-MHz bandwidth and the total harmonic distortion is ~74 dB at full-scale input. When used in an integrated receiver for UMTS, the dynamic range of the modulator substantially reduces the need for analog automatic gain control and its tolerance of large out-of-band interference also permits the use of only first-order prefiltering. An IC including an $I$ and $Q$ $\Sigma\Delta$ modulator, phase-locked loop, oscillator, and bandgap dissipates 11.5 mW at 1.8 V. The active area is 0.41 mm$^2$ in a 0.18-μm 1-poly 5-metal CMOS technology.

Index Terms—1.5-b converter, $\Sigma\Delta$ ADC, telecommunication receiver, UMTS.

I. INTRODUCTION

TELECOMMUNICATIONS receiver architectures are becoming more digitized to improve multimode capability and to get more flexibility. The multimode capability originates from the impending introduction of third generation telecommunication services which will require mobile terminals to be able to operate in either global system for mobile communications (GSM) or universal mobile telecommunication system (UMTS) mode. Because of higher data rates to enable delivery of Internet and video information to the handset, larger bandwidths are needed for the receive path which has implications on the analog-to-digital converter (ADC), which digitizes the incoming signals. Furthermore, the desire to remove analog automatic gain control (AGC) and prefiltering as far as possible, also increases the dynamic range requirement of the ADC. There is a tradeoff to be made between the provision of prefiltering/AGC and the ADC dynamic range which must be made as part of the receiver design process, but the pressure for increased bandwidth and dynamic range is considerable, making the design of the ADC a difficult challenge.

The $\Sigma\Delta$ modulator ADC described in this paper is for use in a highly digitized dual-mode receiver designed for both GSM and UMTS operation. However, only the UMTS aspects of its design and performance will be presented. Sections II–IV will introduce the zero-IF receiver architecture, the most relevant attributes of the UMTS physical layer, and the impact these have on the dynamic range requirement of the ADC. The behavioral aspects of the continuous-time $\Sigma\Delta$ modulator will be discussed in Section V whilst Section VI will describe the circuit implementations. The remaining sections of the paper will present the experimental results and some final conclusions.

II. ZERO-IF UMTS RECEIVER ARCHITECTURE

In Fig. 1, the zero-IF receiver architecture for UMTS is shown. The architecture comprises an RF front-end, an ADC, and a digital baseband processor. The front-end uses a quadrature down-converter to convert the RF channel to the zero IF. Both $I$ (in-phase) and $Q$ (quadrature-phase) components with a 2-MHz bandwidth are converted into the digital domain by a pair of $\Sigma\Delta$ modulators. The baseband processor subsequently provides all the necessary filtering of quantization noise and most of the receiver selectivity.

In a zero-IF architecture, the input signal is translated in frequency such that its spectrum becomes symmetrical around dc. Fig. 2 illustrates this process and the generation of an unwanted image component. In the upper part of the figure [i.e., Fig. 2(a)], the double-sided amplitude spectrum of the real UMTS RF signal is depicted. This is mixed with a complex local oscillator (LO) signal whose spectral Dirac component in the case of a perfect circuit would be located at the center of the band of the UMTS signal at the negative side. Without circuit imperfections, this LO signal would cause perfect translation of the UMTS band on the right of the spectrum down to dc.
as shown in Fig. 2(b). However, as shown in Fig. 2(c), phase and/or amplitude imbalances either in the LO signal or the I and Q components after the mixer can produce a frequency translation of the RF spectrum in the wrong direction and create an unwanted, cochannel image of the UMTS signal at dc. The magnitude of this internally generated image is dependent upon the actual amplitude and phase imbalances.

Given typical process spreads, it is relatively easy to achieve a rejection of the cochannel image by 25 dB since this corresponds to an amplitude mismatch of approximately 1 dB or a phase mismatch of $6^\circ$. This is not difficult to maintain throughout the IF signal chain and therefore within the circuits of the two ADCs. In any case, the spread-spectrum characteristic of the UMTS signal makes it comparatively tolerant to any cochannel image, and even if the cochannel image were strongly correlated with the wanted signal, adequate performance could be obtained with only a 10-dB image rejection ratio.

A well-known generic problem with the zero-IF architecture is the generation of dc offsets and $1/f$ noise in the mixers which fall directly into the wanted signal band. A zero-IF architecture is also prone to large amplitude-modulated interferers which cause distortion in the mixers and which, due to even-order components in the distortion, can fall inside the wanted signal band. These effects have been difficult to overcome for narrow-band systems such as GSM, but for UMTS they are not a serious problem. Once again this is because of the spread-spectrum nature of the signal, which allows a highpass filter to be inserted after the mixer and remove the dc offset and other low-frequency interfering products. The bandwidth of the wanted signal is such that it is relatively undamaged by the presence of a notch at its center. Any remaining $1/f$ noise or intermodulation products are further attenuated (spread) as part of the de-spreading and chip recovery processes. This is also true of any dc offsets and $1/f$ noise generated later in the receiver chain by the ADCs.

In short, the zero-IF receiver architecture is ideal for spread-spectrum communication systems such as UMTS.

### III. UMTS Fundamentals

The UMTS RF receive band extends from 2110 to 2170 MHz and the channel spacing is 5 MHz. As shown in Fig. 3, multiple users occupy the same frequency slot by virtue of being spread to the chip rate of 3.84 MHz by a set of pseudorandom codes, otherwise known as channelization codes. These codes are carefully chosen to be orthogonal to each other so that, on correlation with the correct code during the despreading process at the end of the receiver chain, the spectral density of only the wanted user signal rises by the relevant despreading gain. After integration over the chip period, the energy in all the other co-channel user signals substantially reduces.

### IV. ADC Dynamic Range Specification

The dynamic range of the ADC is the difference (in decibels) between the maximum signal power at the input of the ADC and its integrated equivalent input noise floor. The maximum signal at the input of the ADC is determined by the amount of analog prefiltering, the AGC range, and the power level of the interferers/blocking signals as defined in the UMTS specifications [1]. The required noise floor of the ADC is determined by the receiver sensitivity and the required signal-to-noise ratio (SNR) which on its turn depends on the amount by which the ADC is allowed to contribute to the overall noise figure.

Dealing with the large-signal requirement first, the maximum input to the ADC is chosen to be equal to $-44$ dBm, which is the maximum level of a modulated blocking signal at a 15-MHz offset (at RF) from the wanted signal. There are larger blocking signals at larger frequency offsets but it is assumed that these will be attenuated by prefiltering to a level equal to or lower than $-44$ dBm. To avoid loss in sensitivity, the ADC must remain linear at this power level. According to the UMTS specification, the total power level of the wanted signal plus all the orthogonal noise associated with other users can reach as high as $-25$ dBm, which would imply a considerable increase in dynamic range. However, by applying $19$ dB of AGC (in a single step), this cochannel power can also be reduced to a maximum of $-44$ dBm. For UMTS, the reference sensitivity level of the receiver must be at or below $-117$ dBm. To give some performance margin in this design, the target sensitivity level is taken to be $2.5$ dB lower than that called for in the specification, at a value of $-119.5$ dBm. For the 12.2-kb/s data-rate service, it can be shown by system simulation that the required SNR after
despreading at the input of the demodulator is approximately 1 dB for a bit error rate (BER) of 0.1%. This accounts for the use of convolutional channel coding. Hence, if the $-119.5$ dBm is raised by the despreading gain of 21 dB and then reduced by the SNR of 1 dB, the total effective noise at the input to the receiver must be $-99.5$ dBm. Attributing 0.5 dB of this to the noise of the ADC, the effective noise power of the front-end alone must be $-100$ dBm and that of the ADC noise itself $-110$ dBm. In conclusion, the dynamic range for the ADC must be at least $(-44$ dBm) $(-110$ dBm) $66$ dB. Adding a margin of 4 dB finally results in a dynamic range of 70 dB.

Part of this overhead in dynamic range is annulled by the spread spectrum input signal. Peak amplitudes larger than the full-scale input level of the ADC would cause a temporarily but dramatic increase of the quantization noise floor and/or (depending on the design) instability of the modulator. However, it must be understood that despite the dramatic rise in noise from the ADC, that can be caused by peaks in drive, the peaks themselves will last for a very short time in comparison to the symbol period. After integration over the symbol period, the effect on the BER is not assumed to be serious.

V. CONTINUOUS-TIME $\Sigma\Delta$ MODULATOR

Sigma-delta modulator ADCs are noted for their high dynamic range and conversion efficiency. A continuous-time $\Sigma\Delta$ modulator is chosen because the loop filter provides additional anti-alias filtering [3] which is of considerable benefit when having to handle large offset interferers. Operating together, the two $\Sigma\Delta$ modulators quantize the total signal bandwidth of 4 MHz while individually they deal with only 2 MHz.

The functional block diagram of one $\Sigma\Delta$ modulator is given in Fig. 4 showing the use of a feed-forward, fourth-order loop filter with a single, nonzero transmission pole, and a 1.5-b quantizer and feedback digital-to-analog converter (DAC) combination.

The input signal is converted into a current by $P_{in1,2}$ which flows into the virtual ground node of the first integrator. The data-dependent DAC output voltage is also converted into a current by resistors $R_{DAC1,2}$ and subtracted from the input current. The error signal is integrated on the capacitors of the first integrator and filtered by the rest of the loop filter, which is implemented with gm-C integrators. The feed-forward transconductors ensure stability of the loop by making the loop filter first order at high frequencies.

The clock speed of both the $\Sigma\Delta$ modulators is chosen to be a multiple of the chip rate to avoid fractional decimation. Because in UMTS the chip rate is 3.84 MHz and a zero-IF architecture is used, the conversion bandwidth is $\pm 1.92$ MHz. So the 153.6-MHz clock generated by a PLL represents an oversampling ratio of 40 for both modulators.

The dynamic range of the modulator depends on the following sources of noise: circuit noise ($1/f$ and thermal) emanating mainly from the input resistors, first integrator, and feedback DAC, quantization noise generated by the quantizer, and jitter noise originating in the clock.

To minimize power consumption, the circuit noise is made dominant so the combination of quantization and jitter noise is designed 10 dB below the circuit noise.

To reduce the noise induced by clock jitter, a three-level rather than the more usual two-level quantizer/DAC combination is used. In [2] and [3], the performance degradation due to clock jitter in a 1-b continuous-time $\Sigma\Delta$ modulator is calculated. With two quantization levels (1-b modulator), a return-to-zero (RTZ) ratio of 0.5, an oversampling ratio of 40, a signal bandwidth of 2 MHz, and a Gaussian-shaped clock jitter of 2.5 ps rms, the maximum dynamic range achievable is 75 dB in a 2-MHz bandwidth. This value is too low to meet the target design criteria. Increasing the number of quantization levels $N$, the maximum modulator input signal can increase by a factor of

$$\frac{V_{in,\text{max}, N=n}}{V_{in,\text{max}, N=2}} = \frac{(0.5\sqrt{2} + n - 2)}{n-1} \frac{1}{0.5\sqrt{2}}$$

which for a three-level (1.5-b) modulator yields an extra dynamic range of 1.6 dB with respect to the situation where $\eta = 2$. Simulations show that, with a full-scale sinusoid input, 35% of all output symbols are zero. If the DAC output is zero, the jitter has no contribution to the noise. This results in a further dynamic range improvement of 3.7 dB. Hence, the calculated dynamic range of the 1.5-b modulator due to quantization and jitter noise is 80.3 dB, which is roughly 10 dB more than the 70 dB required by the application. This 10-dB overhead in dynamic range is used to make circuit noise dominant compared to quantization and jitter noise. A simulation (without circuit noise) of the modulator with 2.5 ps white-noise jitter yields an 80.1-dB dynamic range, which is in close agreement with the calculated performance. In this simulation, jitter noise is dominant. The figure 2.5 ps of the time jitter is derived from the measurements on an existing PLL, which was available before the ADC was designed.

Fig. 5 shows the ideal spectrum of the quantization noise at the digital $\Sigma\Delta$ modulator output with and without the 2.5-ps rms Gaussian-shaped clock jitter. Also, the level of the thermal and $1/f$ noise is indicated with the same resolution bandwidth of 1.25 kHz. Taking into account all the noise sources, the theoretical SNR is 70 dB in 2 MHz in which the thermal noise is dominant.
VI. CIRCUIT IMPLEMENTATIONS

The IC has been designed in a 1-poly 5-metal 0.18-μm CMOS process. All critical circuits have been designed differential to have sufficient rejection of power supply noise and substrate bounce.

A. Circuit Implementations of the Loop Filter

In Fig. 6 the input stage of the loop filter is shown in detail. Input transistor M4 has a minimum channel length because of speed, and due to this small channel length its output resistance is very low. To obtain enough dc gain in the integrator stage, a gain boosting technique is used. The supply to the gate of cascode transistor M1 is regulated via the level-shift transistor M2 and amplifying transistor M3. The resulting dc gain is 80 dB and the output swing is 0.8 $V_{pp}$ differential. Fig. 7 also shows the schematic of the circuit used for the second, third, and fourth integrator stages, which also have regulated cascodes to achieve 60 dB dc gain with minimum channel length input transistors. Their output swing is 0.8 $V_{pp}$ differential. The transconductor, which creates the offset transmission pole in the frequency response, is a scaled version of those used in the integrators to ensure good matching. In [4] a fifth-order continuous-time loop filter with two nonzero transmission poles has been described in more detail.

The feed-forward transconductor (Fig. 8) is also a scaled version of those in the integrators; its gm is modified accordingly. The output currents of the feedforward coefficients are summed in the middle of the cascode arrangement and converted to voltages by the two resistors at the comparators. The current $I_{DC}$ determines the separation of the comparator decision levels. The output bits D0 and D1 are fed to the DAC.

B. Feedback D/A Converter

The 1.5-b DAC has an RTZ output to reduce intersymbol interference [5]. The schematic of the DAC is shown in Fig. 9. The input signal $V_{in}$ is converted into a current by the input resistors $R_{in1,2}$. Depending on the output data of the comparators, nodes n1 and n2 are switched to ground or to a reference voltage, $V_{ref1,2}$, through switches M1–M4. The data-dependent DAC output voltage is converted into a current by $R_{DAC1,2}$ resulting in a positive or negative feedback current, $I_{DAC}$. This feedback current is subtracted from the input current and the error signal is integrated on the capacitors of the input stage. By closing switch M5 and opening switches M1–M4 the return to zero level as well as the zero reference level for the 1.5-b DAC is set. In this DAC state, the current $I_{DAC}$ is zero in ideal circumstances.

In [3], the distortion due to the limited gain of the input stage is calculated. Suppose the gain of the first integrator is infinite: the two inputs of the first integrator will be at the same voltage and will not have any signal on them. The DAC linearity is independent of dc offset ($V_o$) in the input stage and process spread $R_{DAC} \times (1 \pm \Delta)$ in the input and feedback resistors. If the common-mode input voltage at both inputs is taken to be $V_{cm}$, three states for the feedback DAC can be distinguished. When
the on-resistances of the switches are assumed to be 0 ohm, the equivalent circuits of the three states can be drawn as illustrated in Fig. 10. The current $I_{DAC,1}$ is implicitly described by the following formulas:

$$V_{x,1} = -\frac{V_o}{2} + I_{DAC,1} \cdot R_{DAC} \cdot (1 + \Delta)$$

$$V_{x,1} = -\frac{V_o}{2} + I_{DAC,1} \cdot R_{DAC} \cdot (1 + \Delta) - \frac{V_{ref}}{2}$$

When the formulas (2a) and (2b) are subtracted, $I_{DAC,1}$ can be obtained as follows:

$$I_{DAC,1} = \frac{V_{ref}}{2 \cdot R_{DAC}} + \frac{V_o}{2 \cdot R_{DAC}}$$

Similarly, formulas for $I_{DAC,0}$ and $I_{DAC,-1}$ can be derived which yield

$$I_{DAC,0} = 0 + \frac{V_o}{2 \cdot R_{DAC}}$$

$$I_{DAC,-1} = -\frac{V_{ref}}{2 \cdot R_{DAC}} + \frac{V_o}{2 \cdot R_{DAC}}$$

As can be seen from the formulas above the DAC is perfectly linear and is only shifted over an offset of $V_o/(2 \cdot R_{DAC})$.

The DAC linearity is dependent on the matching of the switches. In the DAC described above, all the switches are ideal, and every switch has an on resistance of 0 Ω. Because in practice a different pair of switches is active in every state, there is an impedance difference that must be accounted for.

In the design of this particular DAC, the absolute value of the feedback resistors is 37.5 kΩ. The 4σ-value for the mismatch of the on resistance of the different states is in the order of 150 ohms. This gives an impedance mismatch of 0.2%. In Fig. 11, the output spectrum of an ideal fourth-order 1.5-b converter is shown, for the assumption that in the “1” state the impedance differs 0.2% from the “−1” state. The nonlinearity degrades the signal-to-quantization-noise ratio (SQNR) of the converter from 81 to 72 dB. From the spectrum, it is also possible to deduce that the total harmonic distortion due to this mismatch is about −70 dB.

When $\Delta \neq 0$ and $V_o \neq 0$, there will be a dc shift in the common-mode input voltage $V_i$ of the input stage. This can be seen when looking at the average voltage of $V_x$ as function of the $\Sigma\Delta$ modulator output bit stream. If (2a) and (2b) are added, $V_{x,1}$ can be rewritten as

$$V_{x,1} = \frac{V_o}{2} + \frac{V_{ref}}{2} \cdot R_{DAC} \cdot \Delta$$

and similarly $V_{x,-1}$ is given by

$$V_{x,-1} = \frac{V_o - V_{ref}}{2} \cdot \Delta$$

When the $\Sigma\Delta$ modulator produces a “0” output state, the average value of $V_x$ does not change.

Suppose $N_{\text{symbols}}$ is the total number of symbols at the digital output of the $\Sigma\Delta$ modulator. So $N_{\text{symbols}} = N_1 + N_0 + N_{-1}$ with duration $N_{\text{symbols}} \cdot T_s$ in time. The following formulas can now be defined:

$$P_1 = \frac{N_1}{N_{\text{symbols}}}$$

$$P_0 = \frac{N_0}{N_{\text{symbols}}}$$

$$P_{-1} = \frac{N_{-1}}{N_{\text{symbols}}}$$

where $N_x$ is the number of symbols of symbol $x$ with $x = [1, 0, -1]$ and $P_x =$ probability of symbol $x$ in a bit stream with
Furthermore, it can be calculated that \( P_1 + P_0 + P_{-1} = 1 \). Now the average value of \( V_x \), \( \overline{V_x} \), can be derived as

\[
\overline{V_x} = P_1 \cdot V_{x,1} + P_{-1} \cdot V_{x,-1} + P_0 \cdot \overline{V_x}
\]

which can be reduced to

\[
\overline{V_x} = \frac{P_1 \cdot V_{x,1} + P_{-1} \cdot V_{x,-1}}{1 - P_0}.
\]

With (4a) and (4b), this reduces to

\[
\overline{V_x} = \frac{P_1 \cdot \frac{V_a + V_m}{2} \Delta + P_{-1} \cdot \frac{V_a - V_m}{2} \Delta}{1 - P_0}
= \left[ V_o \cdot (P_1 + P_{-1}) + V_{ref} \cdot (P_1 - P_{-1}) \right] \cdot \frac{\Delta}{1 - P_0}.
\]

Intuitively, it can be seen that if \( V_o = 0 \), the dc shift in \( V_x \) is also zero. This is also clear from (7), because in this case \( P_1 = P_{-1} \).

If the two feedback resistors are perfectly matched, the dc shift in \( V_x \) will be zero because \( \Delta \) is zero. As calculated earlier [see (3a)-(3c)], a dc shift in \( V_x \) has no influence on the linearity of the feedback DAC.

**C. Clocking Scheme of the Two ΣΔ Modulators**

The clocking scheme of the two \( \Sigma \Delta \) modulators is illustrated in Fig. 12. The comparators are clocked on the rising edges of the 153.6-MHz PLL output clock. The clock of the DAC is delayed a quarter of the sampling time to compensate for the delay between the comparator latch and its output flipflop. When the comparators give a zero output the feedback current will also be zero. In this way the extra level is implemented.

**VII. EXPERIMENTAL RESULTS**

The test setup shown in Fig. 13 consists of a prototype chip mounted on a printed circuit board. The prototype chip comprises two ADCs (I and Q), a reference oscillator, and a PLL. The oscillator frequency was 30.72 MHz and the PLL output frequency 307.2 MHz, which is frequency-divided by two to produce the required sample clock. An on-chip bandgap circuit provides all the necessary reference voltages and currents. The test signal generator is fed to the ADC via a highly selective lowpass filter which removes the harmonic distortion of the generator. The I and Q ADC output bits are fed to a logic analyzer for data acquisition. The bit stream then is fed to a computer on which an FFT is calculated.

Fig. 12. Clocking scheme and 1.5-b RTZ DAC currents.

![Clocking scheme and 1.5-b RTZ DAC currents.](image)

Fig. 13. Test setup with or without the harmonic distortion prefilter.

![Test setup with or without the harmonic distortion prefilter.](image)

Fig. 14. Measurement at full scale (FS) input.

![Measurement at full scale (FS) input.](image)

Fig. 15. Intermodulation measurement with −6 dBFS input signals at 1.003 and 1.11 MHz.

![Intermodulation measurement with −6 dBFS input signals at 1.003 and 1.11 MHz.](image)

Fig. 16 shows the measured output spectrum of a single \( \Sigma \Delta \) modulator if a 1-MHz tone at full scale is applied to the input. The measured dynamic range in a 2-MHz bandwidth is 70 dB, which is in good agreement with the earlier presented simulations and calculations. Second-harmonic distortion is at −74 dB.

In Fig. 15, an intermodulation measurement is shown. The input frequencies applied to the input of a single \( \Sigma \Delta \) modulator are 1.003 and 1.11 MHz at −6 dBFS. The IM2 and IM3 distances are 76 and 74 dB, respectively.

Fig. 16 shows the SNR and SNDR of the ADC as a function of the input power level of a 400-kHz tone. At high input powers, the second and third harmonics dominate the maximum SNDR figure of 68 dB. Fig. 17 illustrates a blocking interferer test for which the modulator input is an in-band tone at 1 MHz@−41 dBFS.
dBFS together with a sinusoidal blocking signal at 5 MHz@-6 dBFS. This gives a good indication of the linearity of the ADC in circumstances highly relevant to the receiver performance. The degradation in SNR due to the interferer is negligible.

In the test setup for measuring the complex output spectrum from both modulators (i.e., I and Q ADCs active), the harmonic distortion filter was not connected. This was to avoid the effects of gain and phase mismatches in the two pre-filters, which would otherwise introduce a false image of the input tone and confuse the measured image rejection ratio of the two ADCs. Hence, the I and Q generator output signals were connected directly to the I and Q ADCs. The rest of the measurement setup has not changed. In Fig. 18 a measurement of the complex output spectrum from the pair of ADCs is shown for an input tone of 500 kHz at full-scale drive. There is considerable distortion visible in the spectrum but investigations have shown that this originates mainly in the signal generator. Typical of nonlinearities in complex networks of this kind, the third harmonic distortion appears only on the left side of the spectrum. The measurement shows an image rejection of 53 dB while the dynamic range (excluding the power in the distortion products) is 70 dB in 4 MHz. Table I summarizes performance and main design characteristics of the modulator.

Fig. 19 shows the die photograph of one modulator. The prototype IC was fabricated in a 5-metal, 1-poly, 0.18-μm, digital CMOS process. The input resistors, first integrator, second–fourth integrators, feed-forward coefficients, summing node, comparators, and feedback resistors $R_{DAC1,2}$ are indicated.

**TABLE I**

<table>
<thead>
<tr>
<th>Conversion system</th>
<th>Zero-IF</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Sigma\Delta$ modulator</td>
<td>Continuous-Time, 4th order, 1.5 bit</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>153.8 MHz</td>
</tr>
<tr>
<td>Signal bandwidth</td>
<td>2 MHz (single modulator)</td>
</tr>
<tr>
<td>Oversampling ratio</td>
<td>40</td>
</tr>
<tr>
<td>Input voltage range</td>
<td>0.5 V, differential for a sinoid</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>70 dB</td>
</tr>
<tr>
<td>Total Harmonic Distortion</td>
<td>-74 dB</td>
</tr>
<tr>
<td>Image Rejection</td>
<td>&gt;53 dB (only 8 samples measured)</td>
</tr>
<tr>
<td>Process</td>
<td>1.8 V, 1P, 5M, 0.18 μm CMOS</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Area and power consumption</th>
<th>Area [mm²]</th>
<th>Power [1.8 V [mW]]</th>
</tr>
</thead>
<tbody>
<tr>
<td>I&amp;Q $\Sigma\Delta$ modulator</td>
<td>2.012</td>
<td>2.33</td>
</tr>
<tr>
<td>PLL</td>
<td>0.14</td>
<td>3.6</td>
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<tr>
<td>Oscillator</td>
<td>0.029</td>
<td>0.72</td>
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<tr>
<td>Bandgap</td>
<td>0.52</td>
<td>0.54</td>
</tr>
<tr>
<td>Total</td>
<td>0.43 mm²</td>
<td>11.5 mW</td>
</tr>
</tbody>
</table>

**VIII. CONCLUSION**

The design of a fourth-order, 1.5-b, continuous-time $\Sigma\Delta$ modulator has been presented. Two of the modulators operating as a complex pair achieve a dynamic range of 70 dB in a 4-MHz bandwidth and an SNDR of 68 dB at full-scale input. All measurements where done clocked with the integrated PLL and oscillator. All reference voltages and currents are coming from the bandgap circuit. The modulators are able to operate in the presence of large out-of-band interference, thereby reducing the need for anti-alias filtering in a receiver. In these modulators, a 1.5-b DAC is used to reduce the influence of clock jitter on the achievable dynamic range. When used in a zero-IF UMTS receiver, the modulators provide enough dynamic range to substantially reduce the need for analog prefilters and AGC.
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REFERENCES


In 1996–, he joined the Mixed-Signal Circuits and Systems group at Philips Research Laboratories, Eindhoven, where he worked on the design of high-resolution A/D and D/A converters and associated circuits for instrumentation, audio, and radio applications.

Brian J. Minnis (M’00–SM’00) was born in Sheffield, U.K., in 1953. He received the B.Sc. (Honors) degree and the Ph.D. degree from the University of Kent at Canterbury, U.K., in 1973 and 1976, respectively.

He joined Philips Research Laboratories in 1978 to work on the design of microwave systems and components. During the following 18 years, he published approximately 30 papers covering various aspects of his work and a book on the subject of exact network synthesis applied to microwave circuit design. In 1996, he moved into the field of wireless communications and now, as a Research Fellow, leads a team of scientists studying the design of integrated transceivers for cellular and cordless radio applications. The team has successfully transferred several new architectural concepts into handset products for DECT and GSM.

Dr. Minnis is a Fellow of the Institution of Electrical Engineers, U.K.

Johannes A. (Hans) Hegt (M’01–SM’01) was born on June 30, 1952, in Amsterdam, The Netherlands. He studied electrical engineering at the Eindhoven University of Technology (TU/e), where he graduated with honors in 1982. He received the Ph.D. degree on synthesis of switched-capacitor filters in 1988 from the same university.

From 1983 until 1986, he was an Assistant at the TU/e. Since 1987, he has been a lecturer at this University, where he gives courses in the areas of switched-capacitor filter engineering, switched current filters, digital electronics, microprocessors, digital signal processing, neural networks, nonlinear systems, and mixed-signal systems. Since 1994, he has been an Associate Professor on mixed analog/digital circuit design. He is currently especially involved in the hardware realization of ADCs and DACs.

Arthur H. M. van Roermund (M’85–SM’95) was born in Delft, The Netherlands, in 1951. He received the M.Sc. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 1975 and the Ph.D. degree in applied sciences from the K. U. Leuven, Belgium, in 1987.

From 1975 to 1992, he was with Philips Research Laboratories, Eindhoven, The Netherlands. From 1992 to 1999 he was a full Professor with the Electrical Engineering Department of Delft University of Technology, where he was Chairman of the Electronics Research Group and Member of the management team of DIMES. From 1992 to 1999, he was Chairman of a two-year post-graduate school for “chartered designers.” From 1992 to 1997, he was a consultant for Philips.

In October 1999, he joined Eindhoven University of Technology as a full Professor, chairing the Mixed-Signal Microelectronics Group. He is chairman of the board of ProRISC, a nation-wide microelectronics platform.