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Mercha, A.; Vandamme, L.K.J.; Pichon, L.; Carin, R.; Bonnaud, O.

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Current crowding and 1/f noise in polycrystalline silicon thin film transistors

A. Mercha
Université de Caen Groupe de Recherches en Informatique, Image, Instrumentation de Caen, CNRS–UMR 6072, ISMRA, Boulevard du Maréchal Juin, 14050 Caen Cedex, France

L. K. J. Vandamme
Department of Electrical Engineering, Technische Universiteit Eindhoven, Postbus 513, 5600 MB Eindhoven, The Netherlands

L. Pichon and R. Carin
Université de Caen Groupe de Recherches en Informatique, Image, Instrumentation de Caen, CNRS–UMR 6072, Institute des Sciences de la Matière et du Rayonnement, Boulevard du Maréchal Juin, 14050 Caen Cedex, France

O. Bonnaud
Université de Rennes Groupe de Microélectronique et Visualisation, CNRS–UMR 6076, I, Campus de Beaulieu bât 11B, 35042 Rennes Cedex, France

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Here we investigate dc characteristics, impedance versus frequency, and low frequency noise. The effect of current distribution on 1/f noise in polycrystalline silicon thin film transistors (TFTs) is discussed. We show that the channel impedance versus frequency roll induces spectra that could be misinterpreted above a corner frequency in terms of a frequency index $\gamma$ in $1/f^\gamma$ with $\gamma$ higher than 2. Moreover, ignoring the inhomogeneous current distribution leads to overestimation of the noise parameter. Whereas it seemed evident that the noise in TFTs can be interpreted in terms of carrier number fluctuation, the noise parameter variation versus the gate bias can be also understood in terms of mobility fluctuations by including the potential barrier evolution. © 2001 American Institute of Physics. [DOI: 10.1063/1.1404418]

I. INTRODUCTION

Low temperature polysilicon thin film transistors (TFTs) are of a great interest for active matrix liquid crystal displays (AMLCDs), imaging systems, and static random access memories (SRAMs). For these latter applications good electrical properties, in particular low noise levels, are required. However, few investigations of polycrystalline silicon layers can be found in the literature. Recently Michelutti$^2$ reported that 1/f noise in a highly boron-doped polysilicon layer could be attributed to dielectric losses in the grain boundaries. For low or moderately doped polysilicon layers, two different interpretations are generally proposed as the source of 1/f noise: carrier mobility fluctuations or carrier density fluctuations.

In 1982, de Graaff and Huybers$^3$ reported, for samples of different doping levels, that the 1/f noise could be attributed to mobility fluctuations and that the noise parameter $\alpha$ decreases according to the law, $\alpha = (\mu/\mu_{\text{sat}})^g \alpha_{\text{sat}}$. In 1990, Luo and Bosman$^3$ proposed a correction to the previous model that included a position dependent weight function that couples the local fluctuation sources to the terminals through Langevin formalism. In the same year, Jang$^6$ added to the Luo and Bosman model a term for the contribution of built-in potential fluctuations due to mobility fluctuations. In 1999, Chen et al.$^7$ included the scattering at grain boundaries in the Luo and Bosman model to interpret the unusual apparent noise parameter reduction with an increase in the Hall mobility. However ignoring the current crowding effect at grain boundaries often results in too low an apparent mobility and too high an apparent $\alpha$ value.$^8$ Others$^7$ attribute low mobility to grain boundary scattering only.

The second model for noise in polysilicon was proposed in 1988 by Madenach and Werner$^9$ who attributed the 1/f noise to a sum of Lorentzians resulting from trapping of carriers at the grain boundaries. Poly-Si TFTs exhibit large 1/f noise that is always attributed to carrier density fluctuations due to carrier trapping in oxide and/or grains boundary states.$^{10,11}$

Up to now, the noise in poly-Si TFTs has been interpreted only through the carrier number fluctuation with the correlated mobility fluctuation model proposed by Ghibaudo et al. for crystalline-metal–oxide–semiconductor field effect-transistors (C-MOSFETs).$^{12}$ The model of correlated mobility fluctuations with carrier number fluctuation was criticized by Vandamme and Vandamme$^{13}$ Agreement between experimental results and the unified 1/f noise model can only be obtained by using nonphysical fitting parameters.$^{13}$ In this article the influence of the grain boundary potential barrier on the current distribution and the device channel impedance versus frequency and consecutively on noise versus gate bias are investigated.

$^a$Corresponding author; electronic mail: kmercha@greyc.ismra.fr
II. DEVICE DESCRIPTION

The devices under investigation were made by a four-mask process with an aluminum gate. Since each fabrication step of the devices remains at a temperature below 600 °C, it is a so-called low temperature process. In principle the process is compatible with a glass substrate in AMLCD applications. First a low pressure chemically vapor deposited (LPCVD) amorphous layer is deposited on an oxidized monosilicon substrate with two different doped regions: the region adjacent to the oxide is undoped and the upper half is heavily doped in situ. Thermal annealing ensures crystallization of this amorphous silicon layer. The top layer is then plasma etched to define the channel, source, and drain regions. A rf oxygen plasma plus a RCA-type cleaning are performed before an APCVD silicon dioxide is deposited to insulate the gate electrode. The source, drain, and gate electrodes are made of thermally evaporated aluminum. Finally thermal annealing is performed in N2/H2 ambient forming gas to ensure good contact. More details about TFT fabrication (Fig. 1) can be found in Ref. 14. We investigate samples in various geometries W/L = 200/170, 100/38, 100/15, and 60/25 in microns with a gate oxide thickness of \( t_{ox} = 600-1000 \) Å.

III. ELECTRICAL CONDUCTION IN POLY-Si TFTs

The TFT channel can be considered a succession of more of less homogeneous grains separated by highly resistive regions [Fig. 2(a)]. These grain boundaries contain dangling bonds that constitute capture sites for charge carriers. When they are electrically charged, they constitute a potential barrier. An opposite charge in the depletion region surrounding the grain boundaries compensates for the charge trapped at the grain boundaries and impedes the current flow [Fig. 2(b)]. The injected carriers, which are not trapped, induce a reduction of the potential barrier height \( V_B \) according to the charge neutrality relation

\[
V_B = \frac{qN_T^2}{8en},
\]

where \( N_T \) is the density of traps per unit area at the grain boundaries, \( q \) the elementary electrical charge, \( e = \epsilon_0 \epsilon_r \) with \( \epsilon_r \) the relative poly-silicon dielectric constant, and \( n \) the density of free carriers in the channel. For high enough free charge concentration the barrier no longer limits the current flow. The current in these devices, as long as the potential barrier remains non-negligible, is described by thermionic emission of carriers over the potential barrier. In this case, the drain current is given by

\[
I = C_{ox} W \frac{V_G}{L} \mu_0 \exp \left( \frac{-qV_B}{kT} \right) (V_{GS} - V_T) V_{DS}, \quad \text{for } V_{DS} \ll V_G - V_T. \tag{2}
\]

The presence of grain boundaries in the channel has important consequences for the electrical conduction and explains the difference in electrical properties between polycrystalline and single-crystal silicon. The current at low effective gate bias is not only determined by thermionic emission of carriers over the potential barrier, but also by diffusion of the carriers in the crystallite-depleted region. Moreover, the active layer can be represented by the schematic of an equivalent circuit shown in Fig. 2(c). The resistance \( R_n \) and the parallel association of the capacitance \( C_d \) with the resistance \( R_d \) describe, respectively, the nondepleted region of the grain and the depleted zone of the grain including the grain boundary.

The threshold voltage \( V_T \) does not have the same meaning as it does in the (C-MOSFET). Here an on voltage denotation would be more suitable. There is still a contribution of diffusion current for gate biases near the threshold voltage. But at high gate biases, when \( V_B \ll kT \), the current equation is similar to the current relation for C-MOSFET in the ohmic regime. The effective mobility \( \mu_{eff} \) and threshold voltage \( V_T \) are extracted according to the simplified electrical model for C-MOSFET using the procedure described in Ref. 18, and illustrated in Fig. 3. The plot of the ratio \( C_i \)
old voltage $V_T$ is then lower due to hydrogen passivation of defects at the poly-Si/SiO$_2$ interface and at the grain boundaries. Current voltage characteristics at different temperatures [Fig. 4(a)] are also performed to extract the activation energy $E_A = qV_B$ [Fig. 4(b)]. Next we will discuss the role of these potential barriers on channel impedance and also on noise.

**IV. 1/f NOISE EXPERIMENTAL RESULTS**

**A. Measurement setup**

Noise measurements were performed on the wafer level and on encapsulated devices in a shielded environment. A low noise voltage Brookdeal 5004 or current preamplifier Brookdeal 5002 is used followed by a dynamic signal analyzer (HP 35665A) with frequency range from 1 Hz to 100 kHz. Batteries supply all power in order to reduce any external electrical perturbations. Impedance measurements were carried out with an HP4274 multifrequency low capacitance (LCR) meter.

The noise measured at device terminals is always an indirect picture of the microscopic noise source. 1/f noise depends on the current distribution in the device, the number of electrons in the system, and the quality of the material. A physical noise source investigation requires a study of the dc and ac characterization of the devices. The effect of the impedance on the slope of the noise spectrum will be examined.

**B. Cutoff frequency in 1/f noise spectra and impedance measurements**

For low mobility devices, the noise spectra show large 1/f noise, but in the frequency range over 1 kHz pure 1/f noise turns into 1/f$^\gamma$ noise with an exponent $\gamma$ higher than 2 [Fig. 5(a)]. For these devices the impedance versus frequency was investigated by impedance measurements carried out in the frequency range of 100 Hz–100 kHz. A cutoff frequency $F_C$ in the modulus of the impedance is found to be the same as that for the 1/f noise spectrum [Fig. 5(b)]. $F_C$ increases with the gate bias [see Fig. 5(b)]. This behavior can be explained by the depletion region width $W_D$ reduction since the free carrier density in the channel increases and the potential barrier decreases accordingly $^{17}$

$$W_D = \left( \frac{2eV_B}{qn} \right)^{1/2} = \frac{1}{2n} N_T . \quad (4)$$

The cutoff frequency is due to the capacitance and resistance in parallel at the depleted region around the grain boundary (Fig. 2) and is expected to be proportional to $n$, because $F_C = 1/(2\pi RC)$ with $R \approx W_D/n^2$ and $C \approx W_D/n$. The different dependence of $R$ and $C$ on $n$ is also experimentally observed in Fig. 6.

The impedance evolution versus gate bias is attributed to variation of the depletion width with gate bias. The noise source propagates in an impedance network, shown in Fig. (2c). Impedance measurements show that the channel impedance is frequency dependent (Fig. 6). The resistive part rapidly decreasing with gate bias can explain the increase of the cutoff frequency [Fig. 5(a)]. These experiments show that
ignoring the corner frequency of the impedance in Fig. 5(b) can be misinterpreted and the 1/f noise spectra can be misinterpreted beyond that frequency.

C. Apparent noise parameter

The 1/f noise in MOSFETs stems from contributions by the contact and channel. The contribution by the channel is often dominant in good quality devices. This so-called intrinsic 1/f noise is attributed to channel conductivity fluctuations, due to fluctuations of the charge carrier number or the mobility. In the ohmic region of the current–voltage characteristic it is obvious that the open circuit voltage noise $S_V(f)$ is proportional to $I^2$ and that the short circuit current fluctuation $S_I(f)$ is proportional to $V^2$. In order to get rid of obvious bias dependencies 1/f noise is often presented and compared in relative values as $S_V(f)/V^2$. The relative noise is inversely proportional to the size of the system and to the number of independent noise sources. For further comparison between devices we investigate the noise here per carrier in terms of $\alpha$ values. An empirical relation often can describe the 1/f noise in a homogeneous semiconductor:

$$S_R(f) \sim f^{\alpha}$$

where $\alpha$ often is between $10^{-6}$ and $10^{-3}$ but the volume and device length are independent. $N$ is the total number of free charge carriers. For inhomogeneous materials $N_{\text{eff}}$ must be used. The use of an empirical relation, Eq. (5), to calculate $\alpha$ values from experimental results by ignoring the nonuniform current density on a microscopic scale always leads to overestimation of apparent $\alpha$ values. The 1/f noise parameter $\alpha$ is used here as a figure of merit and not to suggest a mobility fluctuation $\Delta \mu$ origin for 1/f noise. In both cases, $\Delta \mu$ or $\Delta N$ models, an apparent parameter $\alpha_{\text{app}}$ can be introduced by analogy with the Hooge empirical relation for homogeneous semiconductors to normalize the measured noise to the number of carriers $N$. 

**FIG. 4.** (a) Current–voltage characteristic at different temperatures from 20 to 50 °C (in 5 °C steps) and (b) Arrhenius diagrams for different gate biases used to extract the current activation energy (C) for process B. $W/L = 100 \mu \text{m}/38 \mu \text{m}$ and $V_{DS} = 50 \text{ mV}$. 

\[\frac{S_R(f)}{R^2} = \frac{\alpha}{Nf^\alpha}\]
It should be noted that in the present case $\alpha_{\text{app}}$ is not a constant and strongly depends on microscopic nonuniformity in the current. Here we do not presume at any time one or the other fluctuation model. In the homogeneous situation the evolution of $\alpha_{\text{app}}$ with the effective gate bias should help to discriminate between both models.\(^{20}\)

For a polycrystalline semiconductor the case is more complex due to

1. inhomogeneous current density between grain boundaries,
2. gate voltage dependent depletion layers between grains boundaries, and
3. inhomogeneous free charge carrier densities and mobilities in the sample.

In Sec. IV D we will illustrate this difficulty. One way to estimate the carrier number $N$ involved and overlooking the problems mentioned is use of the carrier injection method where

$$N = \frac{C_{\text{ox}}WL}{q} v_{G};$$  \hspace{1cm} (7)

the other is with the resistance method where in principle a uniform current density is assumed:

$$N = \frac{L^2}{q \mu R}. $$  \hspace{1cm} (8)

In a homogeneous volume of a semiconductor, the $1/f$ noise can be characterized by an $\alpha$ value obtained indifferently from one or another expression. Here a difference is observed between the apparent noise parameter calculated from experimental results and that from Eqs. (6) and (7) or (6) and (8). This difference decreases at higher gate biases [Figs. 7 and 8(b)] because the channel becomes more uniform. At high gate voltages the grain boundary potential barrier is reduced and the current density can become more uniform. The following simple experiment can explain this trend.\(^{21}\)
The current flows preferentially through the lowest barriers at grain boundaries. These restricted contact regions at the grain boundaries are where the current flows in multicontact zones in the boundary plane. If one contact is considered to be a circular conduction spot, then the resistance of this spot is

\[ R_{\text{spot}} = \frac{\rho}{\pi a}, \tag{9} \]

where \( a \) is the radius of the spot contact, \( \rho \) the resistivity of silicon, and the effective volume \( \Omega_{\text{eff}} \) is

\[ \Omega_{\text{eff}} = 20\pi a^3. \tag{10} \]

This effective volume should be used in the Hooge empirical relation for nonuniform current density situations:

\[ \frac{S_I}{I^2} = \frac{S_{V_{DS}}}{V_{DS}^2} = \frac{\alpha}{n\Omega_{\text{eff}}} = \frac{\alpha}{n20\pi a^3}. \tag{11} \]

If one were to calculate \( \alpha_{\text{app}} \), ignoring current crowding from relation (5) by using \( N = n\Omega \), Eq. (12), with \( \Omega \) the volume of the conducting material, one will find another apparent \( \alpha \) value given by

\[ \alpha_{\text{app}} = \frac{fS_I(f)}{I^2}N = \frac{\alpha}{n20\pi a^3}nL^3 = \frac{\alpha L^3}{20\pi a^3}. \tag{12} \]

Relation (12) is applicable in this experiment for \( a/L < 1/20 \). Hence we find apparent \( \alpha \) values of at least a factor of 15 higher than the real values describing the material properties.

**FIG. 7.** Apparent noise parameter vs the effective gate bias \( V_G^{\ast} \) for two different channel lengths. The difference in the \( \alpha \) value for these two different lengths, 38 and 15 \( \mu \text{m} \), respectively, is attributed to dispersion in the noise, actually observed on the same wafer for the same process.

**FIG. 8.** Relative noise and noise parameter for a high mobility device \( \mu_{\text{eff}} = 190 \text{cm}^2/\text{V s} \) at constant drain voltage \( V_{DS} = 60 \text{mV} \) and with geometry of \( W/L = 60 \mu \text{m}/25 \mu \text{m} \).
The other point that could hide the intrinsic channel noise contribution and that will now be developed is related to the contribution by series resistance noise.

D. Contributions by access resistance

For high gate bias, the normalized noise spectral density increases with effective gate bias \( V_G^* = V_G - V_T \) with power of 2 [Fig. 8(a)] and the apparent noise parameter increases with a power of 3 [Fig. 8(b)]. This phenomenon occurs only in technology with the highest mobility and lowest channel 1/f noise. This behavior is characteristic of the access resistance noise contribution that dominates channel noise, whereas the resistance of the channel \( R_c \) is still higher than the value of series resistance \( R_s \) : 

\[
R = R_c + R_s = R_c \frac{1}{V_G^*},
\]

the total resistance is

\[
S_R = S_{R_c} + S_{R_s} = S_{R_c} = \lambda V_G^*,
\]

the resistance power spectral density is

\[
S_R = S_{R_c} \frac{S_{R_s}}{R_c} \approx V_G^{2},
\]

the normalized noise is

\[
\alpha_{app} = f \frac{S_R}{R^2} \frac{L^2}{q \mu_m R} \approx \frac{V_G^{2}}{R} \approx V_G^{3},
\]

the noise parameter dependence with the gate bias is

\[
\alpha_{app} = f \frac{S_R}{R^2} \frac{L^2}{q \mu_m R} \approx \frac{V_G^{2}}{R} \approx V_G^{3},
\]

from

\[
\frac{1}{N} = \frac{q \mu R}{L^2},
\]

\[
\alpha_{app} = f \frac{S_R}{R^2} \frac{L^2}{q \mu_m R} \approx \frac{V_G^{2}}{R} \approx V_G^{3},
\]

An apparent \( \alpha \) proportional to \( V_G^{3} \) is observed in Fig. 8(b) for \( V_G^* > 15 \) V. The series resistance noise contribution is particularly marked for this device and this geometry due to a lower noise contribution by the channel and a smaller channel width.

The highest mobility reported for this fabrication process can be attributed to the better quality of the grain boundaries due to a plasma hydrogenation process. So the noise contribution by the channel is lower than for the other processes (C versus A and B in Fig. 9). However the access resistance is also present in low mobility devices; this contribution is not seen in the current range investigated \( I < 10 \) \( \mu A \) at \( V_{DS} = 60 \) mV (Fig. 9) since the channel noise is higher and it can hide contact noise. The differences observed in the noise parameter with both methods for carrier number extraction indicate that in low mobility devices the current flow is not uniform. The constriction on the current increases the channel noise contribution. This point in now developed for the different mobility devices.

E. Noise parameter evolution for different effective mobilities

The different mobilities are attributed to improvement in the grain boundaries. The grain boundaries contain a lower
density of states $N_T$, so the potential barrier is lower [see Eq. (1)] and the effective mobility is also improved [Eq. (3)]. The apparent noise parameter can be approximated by power law $\alpha_{\text{app}} \propto V_G^\delta$ with $0.2 < \delta < 1$ in Fig. 9. This dependence is related to the height of potential barrier $V_B$. For high $V_B$ current crowding at grain boundaries increases the noise parameter $\alpha_{\text{app}}$. Current crowding is reduced as the potential barrier decreases. Thus a decrease of the potential barriers at grain boundaries induces a reduction in the noise parameter $\alpha_{\text{app}}$. This interpretation corresponds to the so-called Swiss cheese model. In that model a constant noise parameter $\alpha_H$ is considered for the whole semiconductor, but a few cavities do not participate to the conductivity due to higher potential barriers. The number of these spots remains constant but their dimensions decrease with the gate bias (Fig. 10). The current density is higher near these nonconducting spots than in the homogeneous situation, leading to a higher $1/f$ noise parameter.

For $k$ nonconducting spots of diameter $2a$ (Fig. 11) the resistance and noise ratio between the constricted current path at low effective gate bias $[R, S_R(f)]$ and the channel with uniform current density at high gate bias $[R_0, S_{R_0}(f)]$ are, respectively:27

$$\frac{R}{R_0} = 1 + \frac{kW}{L} \left( \frac{W}{W - 2a} - 1 \right)$$

and

$$\frac{S_R(f)}{S_{R_0}(f)} = 1 + \frac{kW}{L} \left( \frac{W}{W - 2a} \right)^3 - 1 \right).$$

The nonconduction spot area becomes smaller with increasing gate bias according to relation (4). The current can be considered uniform when the activation energy due to potential barriers at grains boundaries becomes lower than thermal energy $kT$ [Fig. 4(b)].

V. CONCLUSION

In this experimental analysis of $1/f$ noise we emphasized the dominating role of the barrier potential at grain boundaries. We showed how the potential barrier and its dependence on gate bias could modify the amplitude and the shape of the $1/f$ noise spectrum.

The parameter $\alpha$ measured in polysilicon thin film transistors is not the Hooge parameter because it does not reflect the intrinsic noise properties of the channel. The contribution by series resistance must be separated out. The role of the potential barrier on current crowding should be introduced to model the $1/f$ noise in poly-Si TFTs and to determine the true noise parameter. Only under these conditions can one investigate the microscopic mechanisms responsible for $1/f$ noise.

Therefore lattice scattering and potential barrier reduction also can explain the $1/f$ noise in poly-Si TFTs.