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Load Current Corrected Capacitor Voltage Control in Eight-Level DC-AC Converter using Extended Commutation Cells

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Abstract—The extended commutation cell is a four-port, four-switch cell that allows for bidirectional energy transport in two orthogonal directions throughout the cell. By cascading multiple cells a multilevel converter can be constructed with a high number of levels. The voltage across each cell capacitor can be adjusted independently of the load, resulting in high flexibility in output levels. This paper presents an improved method for capacitor voltage control, based on a system model and the measured output current. The proposed method is analyzed and verified on a 4.4 kW eight-level dc-ac converter. The obtained reduction in capacitor voltage ripple is more than 75%.

Index Terms—Buck-boost, current control, ECC, multicell, multilevel, switched capacitor.

I. INTRODUCTION

POWER converters have a large range of applications, from low power in mobile devices to high power in grid applications. In all these applications the electric power converters work as an interface between a source and load, allowing microprocessors to operate, electric motors to be controlled, and electric cars to charge. In the search for an increasing power density, the switching frequency in power processing converters is typically being increased [1], and multilevel converters are being used to reduce the size of passive filtering components.

Filtering devices often occupy a significant proportion of the volume of a power converter. To further reduce the size, noticeable development is made for new multicell converter topologies [2]–[5] and modular converter structures [6]–[9]. A higher number of switching levels (more than two) reduces the ripple, and consequently the volume of filtering components. Most popular examples of such multilevel/multicell converters are the flying capacitor, neutral-point clamped, cascaded cell and modular multilevel converters [10]–[12]. However, current multilevel topologies have poor (linear) scaling of levels with respect to the number of switches [11], [13]. Topologies exist that scale the levels exponentially with the number of switches, but these require isolated voltage sources [4], [14] or can not supply active power from each level [15], [16]. In converters based on the extended commutation cell (ECC) [17], shown in Fig. 1, the number of levels scales exponentially with the amount of switches. From each level, active power can be supplied without the use of isolated voltage sources.

One point of concern is the reliability of power electronics, where in most cost-driven applications, a single component failure immediately results in a defective product. To ensure

Fig. 1. Basic circuit diagram of the extended commutation cell implemented with MOSFETs. Connection terminals are indicated with *a*, *b*, *c* and *d*.

sufficient reliability, power semiconductors are not used to their full potential [18]. A basic circuit that is applied in most power converter topologies is the commutation cell [19], which consists of two switches, an inductor, and a capacitor. The switches can be stressed more when making the circuit failsafe to single-fault. However, this comes at a high cost: i.e. adding another six switches and drivers, and replacing each switch with two parallel branches of two series switches [20]. The high cost for single-fault failsafe operation, also applies to the known multilevel converters such as the flying capacitor and neutral-point clamped converter, making it generally undesirable to implement fail-safety, except for special applications such as in aerospace. Each cell of an ECC based converter can isolate a fault if only a single switch is added, and fault tolerance can then be implemented by simply placing cells in parallel.

The ECC is an advanced power electronics switching structure that allows for more flexibility in power converter design. Adding multiple cells in series results in a rapid increase in the number of levels, and adding cells in parallel enables single-fault safe operation. The switching cell is modular and can be cascaded, doubling the amount of levels with each cell. Within the converter, the voltage rating of all switches is only determined by the capacitor voltages of the neighboring cells.

This paper describes the analysis, design and verification of an ECC-based, 230 V_{rms}, 4.4 kW, eight-level dc-ac converter, where the capacitor voltage is controlled with load current correction to obtain high output quality. In the next section the basic operation of the ECC is explained and the analysis

of a two-cell converter is given. The analysis is extended for current-mode control in an ECC-based converter using load current based current estimation and feedback control to obtain a constant capacitor voltage. For comparison, experimental results for both load current corrected control and classical feedback control are given at full load.

II. EXTENDED COMMUTATION CELL

The basic ECC is shown in Fig. 1 where the connection terminals are indicated with letters *a*, *b*, *c*, and *d*. This basic cell is a voltage-to-voltage converter where terminals *a* and *b* are supposed to operate as a pair, and, so are terminals *c* and *d*.

Operation of the ECC consists of two separate modes; the first mode is input-to-output direct connection, when switches $S_{4\eta-3}$ and $S_{4\eta-1}$ are turned on simultaneously, or when switches $S_{4\eta-2}$ and $S_{4\eta}$ are turned on. With the first pair of switches, terminal *a* is connected to *c*, with the second pair, terminal *b* is connected to *d*. The second mode is buck-boost operation, where energy can be transferred between a voltage source connected to terminals *a* and *b* and the capacitor C_η . Assuming continuous conduction mode for the buck-boost operation, the capacitor voltage is given by

$$U_{C_\eta} = U_{ab} \frac{D_\eta^\perp}{1 - D_\eta^\perp} \quad (1)$$

where $D_\eta^\perp$ is the buck-boost duty ratio for $S_{4\eta-3}$ and $S_{4\eta-2}$, with $S_{4\eta-1}$ and $S_{4\eta}$ being complementary. The peak voltage across all switches in the switching cell is $U_{C_\eta} + U_{ab}$.

The operation of the ECC, with both input-to-output direct connection and buck-boost combined, is shown in Fig. 2. With ideal components, these operating modes are fully decoupled.

N-Level converter

By using series connection of multiple ECCs, an *N*-level converter can be constructed, where *N* is exponentially related to the number of switches. As an example a four-level converter is presented in Fig. 3. This four-level converter consists of a single ECC followed by a half-bridge. The idealized piece-wise steady-state switching waveforms for this four-level converter are presented in Fig. 4.

Adding a second ECC introduces an additional four output levels. The resulting two-ECC converter with eight output levels is shown in Fig. 5. In an *N*-level converter, each additional cell multiplies the number of available output voltage levels by a factor of two. Therefore, the number of levels as a function of the number of ECCs, together with the two level introduced by the output half-bridge, is given by

$$N = 2^\sigma \cdot 2 = 2^{\sigma+1} \quad (2)$$

where σ is the number of cells cascaded in series. For a given number of cells the required number of switches, denoted by n_S , is found to be

$$n_S = 4\sigma + 2 \quad (3)$$

Fig. 2. Combined ECC operation of input-to-output direct connection and buck-boost operation. Dashed line: input-to-output direct connection path. Continuous line: buck-boost path. Direct connection between *a* and *c* with buck-boost inductor connected to the input (a) and to the cell capacitor in (b). The other direct connection, between *b* and *d* is shown in (c) with inductor connected to the input and to the capacitor in (d).

Fig. 3. Circuit diagram of an ECC based four-level converter, employing a single ECC and half bridge.

Substituting (3) into (2), after some manipulations gives the number of switches n_S required for the number of levels *N* as

$$n_S = 2^{\frac{2 \ln(N) - \ln(2)}{\ln(2)}} \quad (4)$$

For comparison, n_S for a flying capacitor converter [11], [13] is given by

$$n_S = 2(N - 1) \quad (5)$$

which is also valid for the neutral-point clamped and cascaded cell multilevel converter.

The resulting number of switches for both the ECC and flying capacitor converter, for an arbitrary number of levels is shown in Fig. 6. Note that for ease of visualization a continuous line is plotted despite the fact that (4) and (5) only hold for specific values of *N*. At two or four levels, the

Fig. 5. Circuit diagram of an ECC based eight-level converter, employing two ECCs and a half-bridge.

Fig. 4. Ideal piece-wise steady-state switching waveforms of the four-level converter from Fig. 3. A purely resistive load is assumed and the capacitor voltage U_{C1} is equal to the input voltage U_{dc} .

number of switches for the flying capacitor and ECC multilevel converter are equal; for a higher number of levels, the number of switches in the flying capacitor converter dramatically increases.

A. Output levels

The output levels that can be achieved with the eight-level converter ($\sigma = 2$) from Fig. 5 are listed in Table I. Depending on the capacitor voltages U_{C1} and U_{C2} (assumed to be constant), a set of output voltage levels can be defined, indexed with

$$\ell \in \{N/2, \dots, 1, -1, \dots, -N/2\} \quad (6)$$

In case a zero output level is required ($u_{out} = 0$ V), two switch states will result in 0 V output and a maximum of seven unique active output levels will be available. As shown

Fig. 6. Required number of switches n_S versus number of levels N for an ECC based converter and flying capacitor converter.

TABLE I
8-LEVEL CONVERTER OUTPUT VOLTAGE PER STATE

ℓ	u_{out}
4	$\frac{1}{2}U_{dc} + u_{C1} + u_{C2}$
3	$\frac{1}{2}U_{dc} + u_{C1}$
2	$\frac{1}{2}U_{dc}$
1	$\frac{1}{2}U_{dc} - u_{C2}$
-1	$-\frac{1}{2}U_{dc} + u_{C2}$
-2	$-\frac{1}{2}U_{dc}$
-3	$-\frac{1}{2}U_{dc} - u_{C1}$
-4	$-\frac{1}{2}U_{dc} - u_{C1} - u_{C2}$

in [17], for a set of equidistant output levels, the capacitor voltage for C_η is given by

$$\frac{U_{C_\eta}(\sigma)}{U_{dc}} = \frac{(-1)^{\sigma-\eta} + 2^{\sigma+1-\eta}}{(-1)^\sigma + 2^{\sigma+1}} \quad (7)$$

An example of a capacitor voltage choice for the 1, 2, 3, 4 and 5-cell converter is shown in Table II together with the resulting output range and step size between adjacent levels, all these values being shown with respect to U_{dc} . For each case in Table II there is no zero-level.

B. Voltage control

In Table I the set of output levels for a two-cell converter are presented. Each output level is constructed as a combination

TABLE II
N-LEVEL CONVERTER CAPACITOR VOLTAGE WITH RESPECT TO U_{dc} TO OBTAIN EQUIDISTANT OUTPUT LEVELS.

σ	U_{C_1}	U_{C_2}	U_{C_3}	U_{C_4}	U_{C_5}	$\hat{u}_{out}$	Δu_{out}
1	1	-	-	-	-	$\pm 3/2 U_{dc}$	U_{dc}
2	1/3	1/3	-	-	-	$\pm 7/6 U_{dc}$	$1/3 U_{dc}$
3	3/5	1/5	1/5	-	-	$\pm 3/2 U_{dc}$	$1/5 U_{dc}$
4	5/11	3/11	1/11	1/11	-	$\pm 31/22 U_{dc}$	$1/11 U_{dc}$
5	11/21	5/21	3/21	1/21	1/21	$\pm 3/2 U_{dc}$	$1/21 U_{dc}$

Fig. 7. Basic buck-boost topology.

of the input voltage and the cell capacitor voltages. The levels are formed by directly connecting these capacitors in (anti-) series, stepping between levels results in significant load-steps for the buck-boost operation of the cell. For example, when stepping from $\ell = 3$ to $\ell = 4$ the buck-boost output current of cell two goes from 0 to i_{out} . Therefore, a highly dynamic controller is required to obtain a small ripple in the capacitor voltage of each cell.

III. CAPACITOR VOLTAGE CONTROL

The buck-boost operation in the extended commutation cell is ideally decoupled from the output operation of the converter, therefore the control can also be investigated separately from the output operation. For the buck-boost operations all equations apply that are also suitable for a normal inverting buck-boost that operates in continuous conduction mode. The linearized transfer function of the buck-boost contains a non minimum-phase zero (right hand plane zero). As a result of this zero the initial output voltage response to a change in duty-cycle is inverse to the final direction making the system difficult to control using only voltage control. To overcome this, current mode control can be added [21].

The basic buck-boost circuit with a current-source load is shown in Fig. 7. In the case $g^perp = 1$ the left switch is conducting, if $g^perp = 0$ the right switch is conducting. By applying current-mode control, such as peak current control, the current in the inductor is controlled cycle-by-cycle. As a result of this, the switches, voltage source, and inductor from Fig. 7 can be replaced by a current source. The resulting equivalent circuit of the buck-boost operation of the converter is shown in Fig. 8. As a rule of thumb, due to the delay of the current controller, this equivalent circuit is valid up to approximately $1/4^{th}$ of the switching frequency.

Depending on the momentary output level of the converter, the relation between the cell capacitor voltage u_{C_η} and the cell output current $i_{out,\eta}^perp$ varies greatly, e.g. the load impedance as seen by the converter varies depending on the output level. Therefore, the load will be modeled as a current source and

Fig. 8. Buck-boost equivalent circuit under current-mode control.

Fig. 9. Waveforms of a buck-boost under peak current-mode control.

will be included as a disturbance in the current-mode control models.

A. Peak current-mode control

In peak current-mode control the induct current is compared to a reference current. If the current surpasses the reference value the switch is turned off. At the beginning of the next cycle, the switch is turned on. To prevent any subharmonic oscillations [22] the reference of the inductor current has a slope. The overview of the waveforms of a buck-boost converter under peak current-mode control is shown in Fig. 9. The S and R signals indicate the “set” and “reset” inputs of an SR-latch used to generate the g^perp control signal. An implementation of such a peak current-mode controller is given in Fig. 10. Since the switch is turned-on each time the SR-latch is set, the switching frequency is determined by the pulse generator.

To obtain stable operation of the current-mode controller without any subharmonic oscillations (limit cycles), the slope of the reference current should be equal to the negative slope of the inductor current [22]. This negative slope in the current reference is referred to as “slope compensation” and is implemented by subtracting a sawtooth waveform from the reference current. The required peak value of this sawtooth waveform is calculated by

$$i_{slope,\eta} = \frac{U_{C_\eta} T_\eta^perp}{L_\eta} \quad (8)$$

To obtain an average inductor current $\langle i_{L_\eta} \rangle$ equal to the reference $\langle i_{L_\eta} \rangle^*$, an offset current must be added, as shown

Fig. 10. Implementation of peak current-mode controller.

Fig. 11. Buck-boost voltage control loop. The output current of the cell is modeled as a disturbance of the control signal.

in Fig. 9. This offset current is given by

$$i_{offset,\eta} = \frac{1}{2} \left(1 + \frac{U_{C_{\eta-1}}}{U_{C_{\eta-1}} + U_{C_\eta}} \right) i_{slope,\eta} \quad (9)$$

where $U_{C_{\eta-1}}$ is the input voltage of the corresponding cell.

B. Voltage control loop

The peak current-mode controller is used as an inner loop to reduce the order of the system. To control the capacitor voltage, a voltage controller must be added. Since the buck-boost converter can now be modeled as an integrator, a first-order controller is sufficient to control the capacitor voltage. An overview of the control system is shown in Fig. 11. The linear voltage controller $C_{BB,\eta}$ responds to the error in the capacitor voltage and outputs a reference output current $\langle i_{src,\eta}^\perp \rangle$ for the peak current-mode controller. It is assumed that the peak current controller acts as an ideal current source within the bandwidth of the voltage controller. Therefore the total current into the capacitor is equal to the reference output current $\langle i_{src,\eta}^\perp \rangle$ minus the buck-boost output current $i_{out,\eta}^\perp$.

C. Cell current estimator

With the peak current controller and the feedback voltage controller the capacitor voltage can be stabilized. However, when stepping between levels, severe load-steps occur for each cell. The voltage feedback controller responds to the change in capacitor voltage, but because of the limited bandwidth, the response is slow and a large voltage ripple across the cell capacitor will occur. When the cell buck-boost output current is known, the current reference can be corrected to improve the performance of the voltage controller. However, measuring $i_{out,\eta}^\perp$ is not possible with a single sensor due to the two operating modes of the cell. Therefore an estimation method is proposed in this paper. By measuring the total load current i_{out} , an individual cell current $i_{out,\eta}^\perp$ can be estimated based

on the momentary output level ℓ and a steady-state model of the converter.

From [17] it is apparent that, in steady-state, the buck-boost input current for each cell and level is given by

$$\langle \mathbf{i}_{in}^\perp \rangle = \mathbf{P} \begin{bmatrix} 0 & \mathbf{I} \end{bmatrix}^T \mathbf{A} \mathbf{I}_{out} \quad (10)$$

with $\mathbf{A}$ being an ancillary matrix describing the inter-cell buck-boost gain as

$$\mathbf{A}_{p,q} = \prod_{\eta=q}^p k_\eta \quad \text{if } p \geq q \text{ else } \mathbf{A}_{p,q} = 0 \quad (11)$$

The resulting ancillary matrix has the following structure

$$\mathbf{A} = \begin{bmatrix} k_1 & 0 & 0 & \dots & 0 \\ k_1 k_2 & k_2 & 0 & \dots & 0 \\ k_1 k_2 k_3 & k_2 k_3 & k_3 & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ k_1 k_2 \dots k_\sigma & k_2 \dots k_\sigma & k_3 \dots k_\sigma & \dots & k_\sigma \end{bmatrix} \quad (12)$$

The obtained matrix $\langle \mathbf{i}_{in}^\perp \rangle$ from (10) contains the average buck-boost input current value of each of the cells for each level as

$$\langle \mathbf{i}_{in}^\perp \rangle = \begin{bmatrix} \langle i_{in,1}^\perp(N/2) \rangle & \dots & \langle i_{in,\sigma}^\perp(N/2) \rangle \\ \vdots & \ddots & \vdots \\ \langle i_{in,1}^\perp(1) \rangle & \dots & \langle i_{in,\sigma}^\perp(1) \rangle \\ \langle i_{in,1}^\perp(-1) \rangle & \dots & \langle i_{in,\sigma}^\perp(-1) \rangle \\ \vdots & \ddots & \vdots \\ \langle i_{in,1}^\perp(-N/2) \rangle & \dots & \langle i_{in,\sigma}^\perp(-N/2) \rangle \end{bmatrix} \quad (13)$$

The inductor current is given by

$$\langle \mathbf{i}_L \rangle = \langle \mathbf{i}_{in}^\perp \rangle (\mathbf{I} + \mathbf{K}^{-1}) \quad (14)$$

where $\mathbf{K}$ is a square matrix with the buck-boost gains on the diagonal as

$$\mathbf{K} = \begin{bmatrix} k_1 & 0 & \dots & 0 \\ 0 & k_2 & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & k_\sigma \end{bmatrix} \quad (15)$$

and $\langle \mathbf{i}_L \rangle$ is a matrix containing the average inductor current value for all cells and levels.

In steady state, the buck-boost output current is given by

$$\langle \mathbf{i}_{out}^\perp \rangle = \langle \mathbf{i}_L \rangle - \langle \mathbf{i}_{in}^\perp \rangle \quad (16)$$

Fig. 12. Control system overview for two-cell converter. Additional to the conventional control system with voltage feedback control only, the proposed load current corrected control system is added with dashed lines.

Rewriting (16) in a direct form, using (14) and (10), gives

$$\langle \mathbf{i}_{\text{out}}^{\perp} \rangle = \mathbf{P} \begin{bmatrix} 0 & \mathbf{I} \end{bmatrix}^T \mathbf{A} \mathbf{K}^{-1} I_{\text{out}} \quad (17)$$

Ideally, when the cell capacitor voltage is constant and the switching periodic average inductor current is at the correct value, the buck-boost operation is in steady-state. Therefore (17) can be rewritten as a reference for the buck-boost output current by

$$\langle \mathbf{i}_{\text{src}}^{\perp} \rangle^* = \mathbf{P} \begin{bmatrix} 0 & \mathbf{I} \end{bmatrix}^T \mathbf{A} \mathbf{K}^{-1} \langle i_{\text{out}} \rangle \quad (18)$$

where $\langle \mathbf{i}_{\text{src}}^{\perp} \rangle^*$ contains the switching periodic buck-boost output current reference for each cell and level. The reference for each cell is given as a function of the momentary level by

$$\langle \mathbf{i}_{\text{src},\eta}^{\perp} \rangle^* = \langle \mathbf{i}_{\text{src}}^{\perp} \rangle_{\ell,\eta}^* \quad (19)$$

D. Load current corrected capacitor voltage control

Since the estimated buck-boost output current is not exact, an error will be present when using only the estimated output current, resulting in a non-constant capacitor voltage. Therefore a feedback controller is used to compensate for the remaining error. An overview of the complete control system, including reference correction with the estimated buck-boost output current, is shown in Fig. 12. The load is represented by Z_{load} and the direct input-to-output operation of the converter is represented by the switch block, which combines the bus and capacitor voltages to an output voltage depending on the level signal (ℓ). As the output is also modulated by the switching periodic average output current and level are used, the function blocks $\langle i_{\text{out}} \rangle$ and $\langle \ell \rangle$ take the switching periodic average over the output switching period ($T^+ = \frac{1}{f_{\text{sw}}}$).

The eight-level dc-ac converter is simulated with the proposed load current corrected capacitor voltage control. Ideally a proportional feedback controller is sufficient to stabilize the

capacitor voltage. However, due to possible offset errors in the estimated buck-boost output current an integrating action is desired to eliminate a steady-state error. Therefore a hand-tuned integrating controller with a gain of 2, and a pole at 0 Hz is used. A zero is placed at 100 Hz to provide sufficient phase-margin.

Simulated waveforms of the converter operating with feedback control only are presented in Fig. 13. In this case the capacitor voltage is controlled locally with a peak current controller and a linear voltage controller based on the measured cell capacitor voltage. For the first 15 ms the converter output current is 0 A_{rms}, and after that the load is increased to 19.2 A_{rms}. In Fig. 14 the same simulation is performed but with the proposed load current corrected voltage control. Here the reference for the current controller is the sum of the voltage feedback controller output and the estimated buck-boost output current of each cell. The voltage feedback controller is identical in both cases. It is clear from the simulation that the load current corrected capacitor voltage control reduces the variation of the capacitor voltage significantly, resulting in a more accurate output voltage waveform.

By using the proposed load current corrected capacitor voltage control technique, the voltage ripple the cell capacitors is reduced from 21 V and 11 V peak-to-valley to approximately 3 V peak-to-valley for both capacitors, which is in the same order of magnitude as the buck-boost switching ripple.

IV. EXPERIMENTAL RESULTS

The proposed control scheme has also been experimentally verified on an eight-level dc-ac converter. The test prototype represents a single leg of a three-phase inverter, intended as a proof-of-concept for the extended commutation cell. This first proof-of-concept was designed for the sake of experimental validation, therefore minimum size or maximum efficiency were not a main design objective. The specifications of the

Fig. 13. Simulation result: Output voltage u_{out} , output current i_{out} , cell output current set-points $\langle i_{src}^{\perp} \rangle^*$, cell inductor currents and cell capacitor voltages without load current corrected capacitor voltage control.

converter are listed in Table III. The maximum output power is approximately 4.4 kW.

A. Power stage

The two-cell prototype converter, with circuit diagram as shown in Fig. 15, comprises of five Semikron SKM100GB12T4 half-bridge IGBT modules with isolated

Fig. 14. Simulation result: Output voltage u_{out} , output current i_{out} , cell output current set-points $\langle i_{src}^{\perp} \rangle^*$, cell inductor currents and cell capacitor voltages with load current corrected capacitor voltage control.

drivers. The values of the inductors were dimensioned such that the nominal current ripple is the same for both inductors. The inductors are constructed around a core of four Magnetics K133TC026 sections each. Electrolytic capacitors were selected as cell capacitors and are chosen for their rms current rating. Parallel to the cell capacitor, film snubber capacitors were placed close to the power modules. The current through

Fig. 15. Circuit diagram proof-of-concept eight-level converter, employing two ECCs. The dashed boxes indicate the position of the half-bridge IGBT modules.

TABLE III
TWO-CELL, EIGHT-LEVEL DC-AC CONVERTER EXPERIMENTAL SETUP
SPECIFICATIONS

Parameter	Value
U_{dc}	300 V
U_{out}	230 V _{rms}
f_{sine}	50 Hz
R_l	11.7 Ω
L_l	150 μ H
$\hat{u}_{out}$	± 350 V
L_1, L_2	210 μ H, 140 μ H
C_1, C_2	1000 μ F
U_{C1}^*, U_{C2}^*	100 V
f_{sw}^+, f_{sw}^-	10 kHz

the inductors was measured with high-frequency current transducers, the capacitor voltages were measured using isolated voltage transducers.

B. Controller implementation

The control system was implemented in a dSPACE system comprising of a DSP and FPGA subsystem. The output reference signal u_{out}^* was generated in the DSP and the phase-disposition PWM modulator for the multilevel output signal was implemented in the FPGA. The output was operated in open-loop and works as a variable voltage source. The cell buck-boost current controllers were implemented in the FPGA using high frequency ADCs (10 MHz) to sample the inductor current. The voltage controllers for the cell capacitors were implemented in the DSP together with the buck-boost output current estimator. The implemented voltage controllers are identical to the feedback controllers as applied in the simulations of Fig. 13 and Fig. 14.

C. Measurement results

The completed experimental prototype is shown in Fig. 16. A symmetric supply of 150 V is used to power the converter and the load is formed by a 11.7 Ω power resistor R_l with a parasitic inductance L_l . Due to the switching delay of the

Fig. 16. Experimental setup.

IGBTs, a blanking time is added to the gating signals. This blanking time is 1 μ s and was implemented as a delayed-on for each switch. The output reference is a sine wave of 50 Hz with a modulation depth of 0.9.

The obtained measurement results, where the prototype converter was operated with a load current of 19.2 A_{rms}, are shown in Fig. 18. The operating conditions are identical to the simulations of Fig. 13 and Fig. 14. In Fig. 17 the results are shown with only feedback control. In Fig. 17 (a) the capacitor voltages show a shape similar to simulation with a ripple of 27 V and 14 V peak-to-valley, a detailed view of the inductor currents is provided in Fig. 17 (b). With the load current corrected voltage control the ripples are reduced to approximately 5 V and 3 V peak-to-valley. This is shown in Fig. 18 (a) with a close-up view of the inductor currents is given in Fig. 18 (b). The remaining ripple has a frequency of twice the load current as active power is delivered in both the positive and negative half of the sine wave.

The improved capacitor voltage control is also visible in the output voltage waveform of Fig. 18, where each level is now virtually a flat line. This is emphasized in Fig. 19 where the

Fig. 17. Experimental results of two-cell, eight-level converter with 11.7 Ω load. Capacitor voltage controlled by feedback only. Output voltage u_{out} (200 V/div), output current i_{out} (20 A/div), capacitor voltage ripples (10 V/div offset by 100 V) and inductor currents (100 A/div). (a) Capacitor voltage ripples. (b) Inductor currents.

signals are plotted on a shorter time-base. Due to the blanking time and high voltage slew rates small spikes can be observed between the level transitions, during blanking time the output level is determined by the output current. Since the blanking time is quite short, the resulting error in the output current, also shown in Fig. 19, is small.

At full load a drop in the output voltage is visible. This is because of the forward voltage drop of the IGBTs that are used for the direct input-to-output connection. As the direct input-to-output operation of the converter is operated in open-loop, there is no compensation for this drop. The resulting output voltage at full load is therefore approximately 220 V_{rms}. With the high capacitor voltage ripple under capacitor voltage feedback only, the output voltage is reduced to approximately 215 V_{rms}.

The start-up of the converter under full-load is shown in Fig. 20. The converter is enabled at the zero-crossing of the 50 Hz reference signal. The measurements show a robust start, even while the input-to-output operation is stepping through the levels. Approximately 4 ms after enabling the converter both capacitor voltages are at their nominal levels.

Fig. 18. Experimental results of two-cell, eight-level converter with 11.7 Ω load. Capacitor voltage controlled with the proposed load current corrected capacitor voltage control. Output voltage u_{out} (200 V/div), output current i_{out} (20 A/div), capacitor voltages (10 V/div offset by 100 V) and inductor currents (100 A/div). (a) Capacitor voltage ripples. (b) Inductor currents.

Fig. 19. Experimental results of two-cell, eight-level converter with 11.7 Ω load under load current corrected capacitor voltage control. Output voltage u_{out} (200 V/div), output current i_{out} (20 A/div), and capacitor voltage ripples (10 V/div offset by 100 V).

Fig. 20. Experimental results of the startup of a two-cell, eight-level converter with 11.7 Ω load under load current corrected capacitor voltage control. Output voltage u_{out} (200 V/div), output current i_{out} (20 A/div), and capacitor voltages (100 V/div).

V. CONCLUSION

The control strategy proposed in this paper provides a significant reduction in capacitor voltage ripple in extended commutation cell based converters. A complete control system has been analyzed for an extended commutation cell based converter to stabilize the voltage across the cell capacitors. With the use of peak current controllers and linear feedback control on the capacitor voltage, the capacitor voltage can be stabilized. By applying the proposed cell current estimation the load current was used to determine the required cell current reference. This allows for a faster response to changes in output level and load current.

A comparison was made in simulation between a control system with capacitor voltage feedback control only, and with the proposed load current correction. The resulting capacitor voltage ripple was reduced by about 85% and 73% for capacitor C_1 and C_2 . Also a very fast response to large load changes has been achieved. Experimental verification of both control strategies on a two-cell, eight-level dc-ac converter of 4.4 kW, shows similar results to the simulation. A reduction of 76% and 78% has been obtained for the voltage ripple in capacitors C_1 and C_2 , where in both cases the same voltage controller is used. The response to large load changes is fast and without any oscillatory behavior.

Additionally the startup behavior of the converter is experimentally verified. The start from 0 V across both cell capacitors, with the full load connected to the output of the converter, shows stable and robust behavior. Both cell capacitors reach their nominal value within 4 ms.

The extended commutation cell has potential in applications where a multilevel voltage is required that can supply a load from dc to a high frequency. Since no or only a minimum of filtering is required on the output, a very high output bandwidth can be obtained. By using smart control, as shown in this paper, the voltage ripple across the cell capacitors can be kept to a minimum.

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verter structures.

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