A 10.7MHz IF-to-baseband sigma delta A/D conversion system for AM/FM radio receivers

A 10.7-MHz IF-to-Baseband $\Sigma\Delta$ A/D Conversion System for AM/FM Radio Receivers

Eric J. van der Zwan, Kathleen Philips, and Corné A. A. Bastiaansen

***Abstract*—$\Sigma\Delta$ modulation with integrated quadrature mixing is used for analog-to-digital (A/D) conversion of a 10.7-MHz IF input signal in an AM/FM radio receiver. After near-zero IF mixing to a 165 kHz offset frequency, the I and Q signals are digitized by two fifth-order, 32 times oversampling continuous-time $\Sigma\Delta$ modulators. A prototype IC includes digital filters for decimation and the shift of the near-zero-IF to dc. The baseband output signal has maximum carrier-to-noise ratios of 94 dB in 9 kHz (AM) and 79 dB in 200 kHz (FM), with 97 and 82 dB dynamic range, respectively. The IM3 distance is 84 dB at full-scale A/D converter input signal. Including downconversion and decimation filtering, the IF A/D conversion system occupies 1.3 mm^2 in 0.25-μm standard digital CMOS. The $\Sigma\Delta$ modulators consume 8 mW from a 2.5-V supply voltage, and the digital filters consume 11 mW.**

***Index Terms*—Analog-to-digital conversion, continuous time circuits, IF systems, passive mixers, radio receivers, sigma–delta modulation.**

I. Introduction

THE AIM FOR highly integrated low-power wireless communication devices for use in cellular phones or wireless LANs, for example, has resulted in a clear digitization trend in radio receiver technology. Newly developed technologies can also be applied to traditional receivers, for example, in car radios. Already a lot of digital signal processing is applied in car radios, but usually the receiver is still analog. Fig. 1 shows a block diagram of an AM/FM radio receiver using digital audio signal processing. Depending on the continent, the FM input signal may be between 65–108 MHz. AM signals, including LW, MW, and SW frequency bands, range from 145 kHz to 10 MHz. The radio front-end converts the FM or AM antenna signal to an intermediate frequency (IF) of 10.7 MHz. FM demodulation takes place after 200-kHz channel selection at the IF, resulting in the FM multiplex signal (FMMPX). AM signals are processed by a double conversion receiver using the same 10.7-MHz frequency as first IF. After mixing to a second IF (for example 450 kHz), 9-kHz channel filtering, and amplification by an automatic gain control (AGC) amplifier, AM detection takes place. The FMMPX or AM audio signal is digitized in the audio signal processor IC. This signal processor may provide functions like interference absorption, stereo decoding, radio data system (RDS) decoding and audio controls such as volume, balance, tone control, and dynamics compression. At the output, the digital signals are converted to analog signals, which connect to the audio power amplifiers.

An AM/FM receiver with a higher level of integration is shown in Fig. 2 [1], [2]. In this solution, the analog-to-digital (A/D) conversion takes place at the 10.7-MHz IF, both for FM and for AM input signals. Demodulation of the radio signal is performed digitally, which simplifies the analog radio front-end. An FM channel filter, usually about 200 kHz wide, is still required to protect the AGC and the A/D converter (ADC) from strong interfering signals. Its specification may however be relaxed, because it does not necessarily have to provide full channel selectivity: final channel filtering takes place in the digital domain. This configuration enables a software-controlled variable bandwidth of the digital channel selection filter. This bandwidth can be chosen such that an optimum tradeoff between selectivity and adjacent channel suppression is achieved. Since AM channels are only 9 kHz wide, no selectivity is provided in front of the ADC. About twenty AM channels will pass through the 200-kHz FM channel filter. If the IF ADC provides sufficient dynamic range and linearity, the AM channel filter can be omitted and AM channel selection is shifted to the digital domain completely. Again, the bandwidth may be configurable by software depending on the strength of neighboring channels.

The key element in the system of Fig. 2 is the IF ADC. In FM mode, a single 200-kHz channel must be converted to digital [Fig. 3(a)]. Neighboring channels are attenuated by the FM channel filter by some 40 dB. However, because of the large dynamic range of the radio signals, the neighboring channels are not completely removed by the channel filter, and may even still be stronger than the wanted channel. Depending on the gain range of the AGC amplifier, the dynamic range at the ADC input is about 70 dB. Further filtering providing the required channel selectivity is performed digitally. In AM mode, neighboring channels are not attenuated by the FM channel filter [Fig. 3(b)]. Again depending on the amount of AGC, the required dynamic range at the ADC input may be larger than 90 dB. The presence of very strong unwanted channels complicates the reception of weak radio channels, and makes this AM/FM ADC more difficult to realize in AM mode than in FM mode in terms of linearity. Nonlinearity introduces intermodulation distortion or other spurious frequency components into the wanted channel, or the noise level may be increased by the presence of large interference. Hence, the multichannel aspect for AM puts severe requirements on the AGC amplifier and ADC in terms of noise, linearity, and spurious-free dynamic range.

The digitization in Fig. 2 may be performed by a wide-band ADC [1]. A resolution of 10 bits in 11-MHz bandwidth may

Manuscript received April 10, 2000; revised July 17, 2000.

E. J. van der Zwan, deceased, was with Philips Research Laboratories, 5656 AA Eindhoven, The Netherlands.

K. Philips and C. A. A. Bastiaansen are with Philips Research Laboratories, 5656 AA Eindhoven, The Netherlands (e-mail: Kathleen.Philips@philips.com).

Publisher Item Identifier S 0018-9200(00)10047-2.

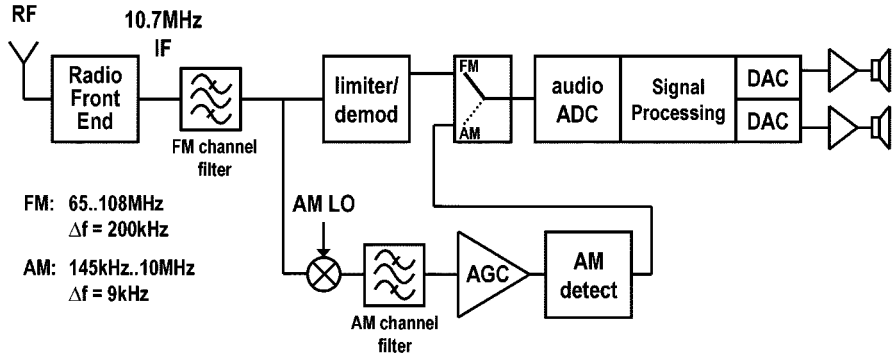


Fig. 1. Simplified block diagram of an AM/FM radio with digital audio signal processing.

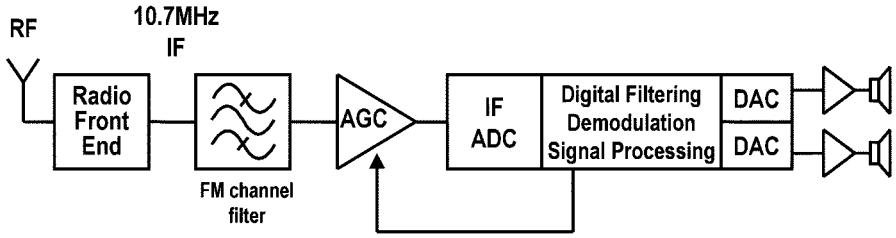
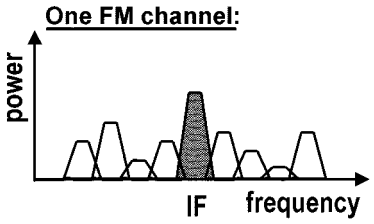
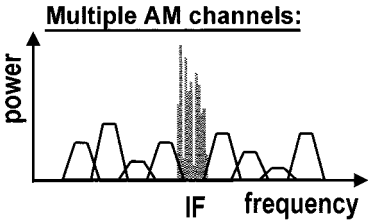


Fig. 2. IF A/D conversion in an AM/FM radio receiver.



(a)



(b)

Fig. 3. IF ADC input spectrum in FM (a) and AM (b) mode.

be sufficient to achieve the noise specifications. However, the linearity requirements for AM are difficult to meet at the 10.7-MHz input frequency. Therefore, an analog AM channel filter is still necessary, which is applied after mixing to a second IF of 450 kHz. Alternatively, bandpass $\Sigma\Delta$ modulation may be used [2]–[7], providing the required resolution in the bandwidth of interest only. Solutions for AM [3] and FM [4], [5] have been shown, but with limited performance and relatively high power consumption. Further development resulted in combined solutions for AM and FM [2], [6]. Again, the input stage has to be very linear at the 10.7-MHz IF to prevent intermodulation of neighboring channels in AM mode, which is difficult to achieve. A different approach uses a $\Sigma\Delta$ phase-locked loop (PLL) to digitize and demodulate FM radio signals directly after the limiter in [8, Fig. 1]. Because of the high dynamic range of the radio signal and the intermodulation distortion requirements, none of these techniques eliminates the need for a high-Q channel filter.

The ADC described in this paper mixes the 10.7-MHz input signal to a second low intermediate frequency, and uses continuous-time $\Sigma\Delta$ modulation to digitize the resulting signal. In Section II advantages and disadvantages of A/D conversion at near-zero-IF are discussed. Section III deals with the continuous-time $\Sigma\Delta$ modulators with integrated mixers that are used for the A/D conversion of the 10.7-MHz IF signal. Section IV discusses the implementation of some relevant parts of the ADC, and in Section V measurement results on a prototype IC are shown. Finally, in Section VI, conclusions are drawn.

II. A/D Conversion at Near-Zero-IF

The fact that at lower frequencies high linearity is easier to achieve than at higher frequencies justifies further frequency downconversion of the IF signal by a second mixer stage, as depicted in Fig. 4. The A/D conversion is performed at a much lower frequency compared to the 10.7-MHz IF in this case. The second mixer may convert the wanted signal band to dc ("zero-IF") or to an offset frequency ("near-zero-IF" or "low-IF"). Both methods have advantages and disadvantages [9]. Using zero-IF, the required ADC bandwidth is as low as possible. The main disadvantage is the sensitivity to dc offset, which may be introduced by circuit mismatch, local oscillator crosstalk or second-order distortion in the mixer. Fig. 5(a) shows an example of a complex frequency spectrum of the quadrature mixer outputs ($I+jQ$) in Fig. 4.

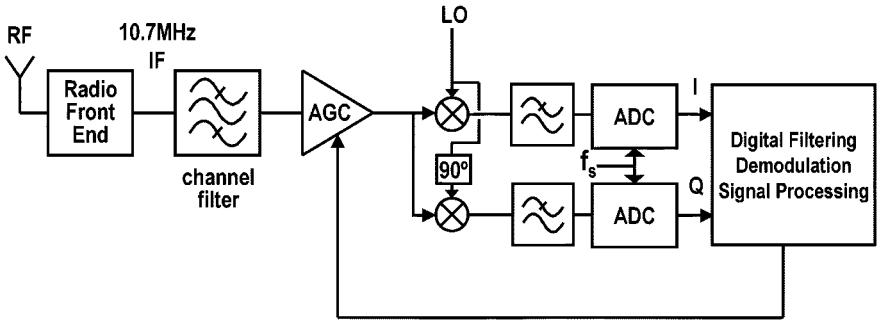


Fig. 4. Conventional dual-conversion receiver.

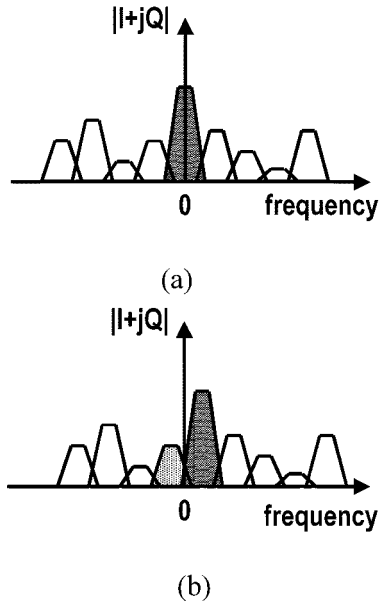


Fig. 5. Quadrature mixer complex frequency spectrum ($I + jQ$) for zero-IF (a) and near-zero-IF (b).

Since dc offset as well as flicker noise is located in the middle of the wanted channel, it cannot be removed without loss of part of the input signal. This is the main reason why mixing to a near-zero-IF is preferred. The wanted signal is not mixed to dc, but to an offset frequency equal to at least half the channel bandwidth. In this case, the dc offset and flicker noise are still outside the wanted channel after the frequency conversion [Fig. 5(b)]. Although a quadrature signal path is needed for suppression of signals at the image frequency, this topology is still favorable for performance and efficient in terms of power consumption.

Mismatch in the quadrature paths leads to leakage of signals around the image frequency into the wanted signal band. Using zero-IF the signal at the image frequency is the mirror of the wanted signal, and therefore the requirements for image rejection are relatively relaxed. However, when near-zero-IF is used, the signal at the image frequency of the wanted channel is its adjacent channel. Since the adjacent channel may be significantly stronger than the wanted channel, the image rejection requirements are much more severe for near-zero-IF than for zero-IF [9]. This implies that accurate gain matching and 90° phase difference between the I and Q paths is required. The image rejection can approximately be expressed as

$$IR = 10\log\frac{4}{\left(\frac{\Delta A}{A}\right)^2 + (\Delta\phi)^2}$$

where $\Delta A/A$ represents the relative gain mismatch between I and Q, and $\Delta\phi$ is the phase error in radians [10]. The AM/FM application requires about 80 dB of image rejection. The channel filter at the 10.7-MHz IF (see Fig. 4) attenuates the adjacent channel by some 40 dB, so another 40 dB of rejection must be provided by matching of I and Q. Assuming equal contributions from gain and phase error, a gain error below 1.4% is required, and the phase error must be less than 0.8°.

III. Continuous-Time ΣΔ Modulators With Integrated Mixers

In [11], a continuous-time ΣΔ modulator with an integrated passive mixer was presented. It was shown that with this technique a high-resolution high-linearity IF ADC can be implemented with very low power consumption. The shaded area in Fig. 6 shows how this technique is applied for A/D conversion of the 10.7-MHz IF in an AM/FM receiver. The quadrature near-zero-IF mixer outputs are digitized by continuous-time single-bit low-pass ΣΔ modulators. A complex digital filter decimates the I and Q output bitstreams and also performs the final frequency shift to dc. Thus, an ADC is implemented with 10.7-MHz IF input and filtered digital baseband output. Comparing Fig. 6 to Fig. 1, the AM channel filter is not required anymore, provided that the IF AGC and ADC have sufficient dynamic range and linearity to cope with large interfering neighbors of the wanted channel. The complete path from 10.7-MHz IF to analog audio can be integrated in a single CMOS IC. In terms of power consumption, the IF AGC in Fig. 6 is most critical, since compared to the ADC it has to deal with even higher dynamic range with the same linearity constraints at its input. Although the IF AGC implementation is beyond the scope of this paper, it is expected that its power consumption is higher than the AGC in Fig. 1, because the lack of AM channel filtering poses heavier demands on linearity and dynamic range.

Fig. 7 shows a more detailed block diagram of the IF ADC. The input voltage is converted to currents by input resistors

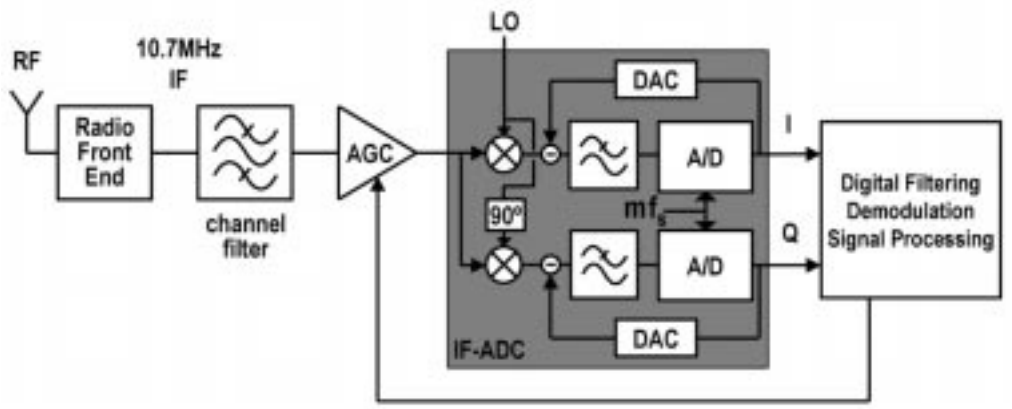


Fig. 6. IF ADC implementation by $\Sigma\Delta$ modulators with integrated mixers in a dual-conversion receiver.

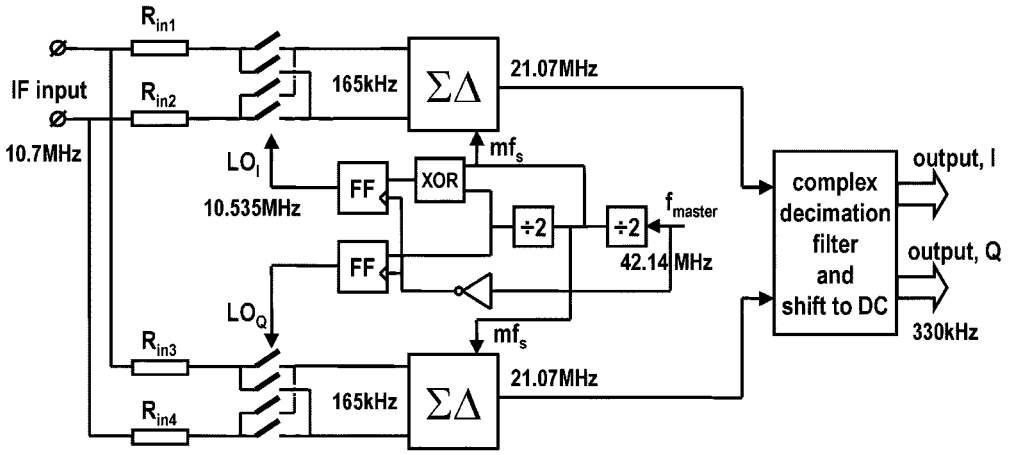


Fig. 7. 10.7-MHz IF ADC block diagram.

$R_{\mathrm{in}1}$ and $R_{\mathrm{in}2}$. Passive mixers are implemented by switches at the inputs of the $\Sigma\Delta$ modulators, which are low-ohmic (virtual ground) in this case. The on-resistances of the mixer switches are much smaller than the input resistors. Thus, high linearity is achieved because these on-resistances are only weakly modulated. Power consumption of the passive mixers is negligible. Using continuous-time $\Sigma\Delta$ modulators has several advantages. Continuous-time $\Sigma\Delta$ modulators tend to use less power than switched-capacitor implementations [13]. Also, the high-frequency components generated by the mixers are removed by the inherent low-pass filtering characteristic of continuous-time $\Sigma\Delta$ modulators. A switched-capacitor implementation would require anti-aliasing filters between the mixers and the $\Sigma\Delta$ modulator inputs. Alternatively, the input switches of switched-capacitor $\Sigma\Delta$ modulators might be used as subsampling mixers for the IF input signal [14]. However, in that case flexibility is lost because the mixing frequency is equal to the sampling frequency. Moreover, since in a switched-capacitor implementation the switches are connected to the input signal, their gate–source voltages show large variations. Therefore, the linearity of the switches is more critical than in the continuous-time case as shown in Fig. 7, where the switches are at virtual ground. The most important disadvantage of continuous-time $\Sigma\Delta$ modulators is their higher sensitivity to clock jitter, which has to be included during evaluation of the noise budget of the system.

Both the sampling frequency and the mixer local oscillator frequency require high accuracy and low jitter. These frequencies were chosen such that they can be derived from a single master clock frequency of 42.14 MHz generated by an on-chip crystal oscillator. The wanted channel is mixed to 165 kHz by the mixer local oscillator (LO) frequency of 10.535 MHz, which is obtained by dividing the master clock by 4. An exclusive-or function of this LO with half the master clock frequency (21.07 MHz) provides 90° phase shift between the local oscillator signals for I and Q (see Fig. 7). High phase accuracy is achieved by re-clocking both LO_I and LO_Q with the master clock. A Nyquist sampling rate of 658 kHz is used for the digitization of the input signal band centered at 165 kHz. Thus, a maximum frequency deviation of about $\pm$150 kHz is allowed in FM mode. The $\Sigma\Delta$ modulators operate at an oversampling ratio of 32, so the sampling rate is 21.07 MHz, which is half the master clock rate.

The $\Sigma\Delta$ modulators are based on [12], [11], but have fifth-order loop filters with complex conjugate poles (Fig. 8). These poles provide additional filter gain within the signal bandwidth and appear as notches in the shaped quantization noise spectra of the $\Sigma\Delta$ modulators. One of the notches is located at the 165-kHz

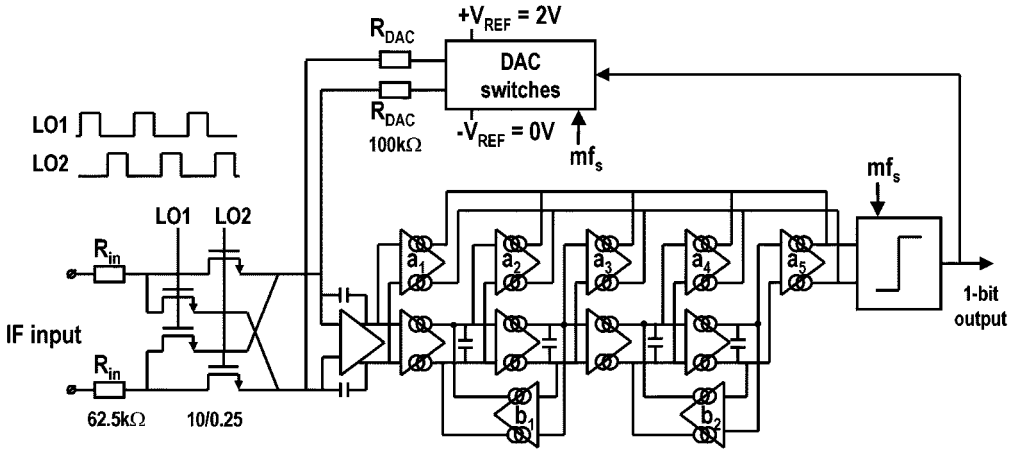


Fig. 8. Fifth-order IF $\Sigma\Delta$ modulator implementation with complex conjugate loop filter poles.

offset frequency, the other one at the edge of the signal band. The near-zero-IF mixer is implemented by nMOS switches at the virtual ground nodes of the first integrator input. At these nodes, the 1-bit feedback DAC current is also subtracted from the input signal. The mixer switches are driven by local oscillator signals LO1 and LO2, which are nonoverlapping in order to prevent a short-circuit between the input nodes during switching. Such a short-circuit would give rise to distortion of the feedback DAC pulses, and cause leakage of the high-frequency quantization noise into the signal band [11].

The loop filter is implemented by means of simple transconductor-C integrators with feed-forward coefficients a_i. These feed-forward coefficients provide first-order roll-off at unity open-loop gain for stability reasons. Large signal stability is guaranteed by clipping the integrator outputs, starting at the fifth integrator (graceful degradation) [13]. The resonators introducing the complex conjugate poles are implemented using local feedback transconductors b_1 and b_2. The 1-bit feedback DAC current is made by switching resistors between positive and negative reference voltages generated by an on-chip bandgap reference circuit. Return-to-zero coding is used in order to minimize intersymbol interference. The resulting shaped quantization noise frequency spectrum assuming ideal circuit elements is shown in Fig. 9. In practice, the quality factors of the resonators will be limited, and component spread causes deviation of the position of the notches. However, the impact of these nonidealities is small since the overall noise in the band of interest is dominated by the circuit noise as also shown in Fig. 9. Assuming 20% error in the time constants, the signal-to-quantization noise ratio (SNQR) is 86 dB in 200 kHz (FM) and 102 dB in 9 kHz (AM), which are still significantly better than the target values of 70 dB for FM and 90 dB for AM. The main contribution to the circuit noise is the thermal noise of the input and the feedback DAC resistors of the $\Sigma\Delta$ modulator. Another limiting factor for signal-to-noise ratio (SNR) may be clock jitter. Approximation [13] and simulations have shown that the RMS clock jitter must be below 7 ps, which can be achieved with an on-chip crystal oscillator.

If a near-zero-IF topology with separate quadrature paths is chosen, effectively the required ADC bandwidth is doubled compared to the zero-IF solution, because both the wanted and

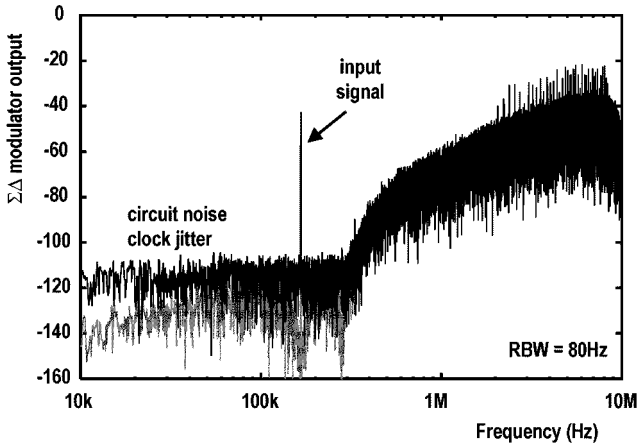


Fig. 9. Simulated $\Sigma\Delta$ modulator quantization noise and circuit noise.

the image channel are converted to digital. Theoretically, a complex or quadrature $\Sigma\Delta$ modulator would be more efficient, since it provides the required resolution in the bandwidth of interest only. Such a modulator can be made by implementing a complex loop filter in the $\Sigma\Delta$ modulators [15]. This would result in lower quantization noise in the wanted signal band, or the same noise level at a lower sampling rate. However, limited image rejection caused by circuit mismatch would cause leakage of the shaped quantization noise from the image band into the signal band. For that reason, some shaping of the noise in the image band is still necessary, which makes the noise shaping in the wanted signal band less effective [15], [16]. In the ADC described in this paper, the possible reduction of the sampling rate by using complex $\Sigma\Delta$ modulation was not very significant, and also impractical in terms of frequency planning. Therefore, straightforward implementation of separate real I and Q paths was chosen.

IV. Circuit Implementations

The input stage of the $\Sigma\Delta$ modulator of Fig. 8 is implemented as an active *RC* integrator (Fig. 10) [12]. The amplifier is a simple single-stage operational transconductance amplifier (OTA), with large input transistors operating in weak inversion

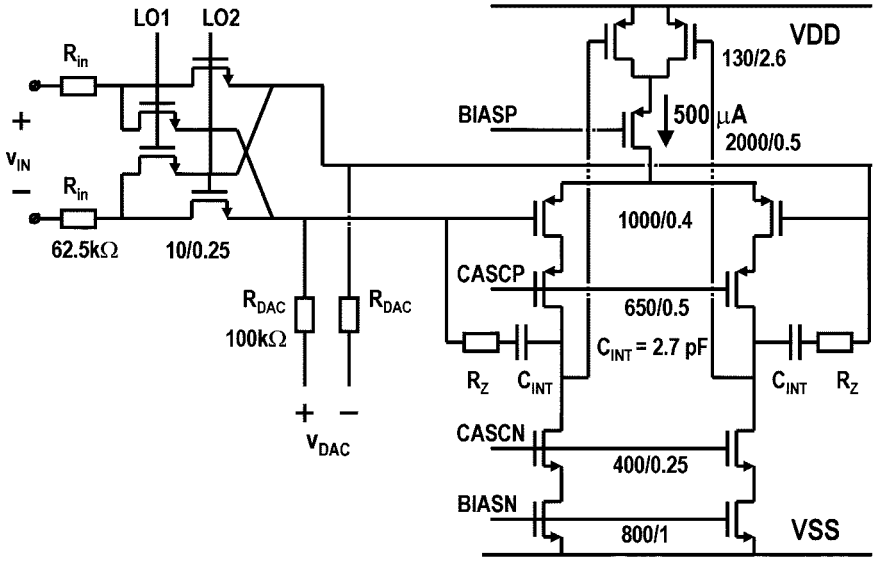


Fig. 10. IF $\Sigma\Delta$ modulator input stage.

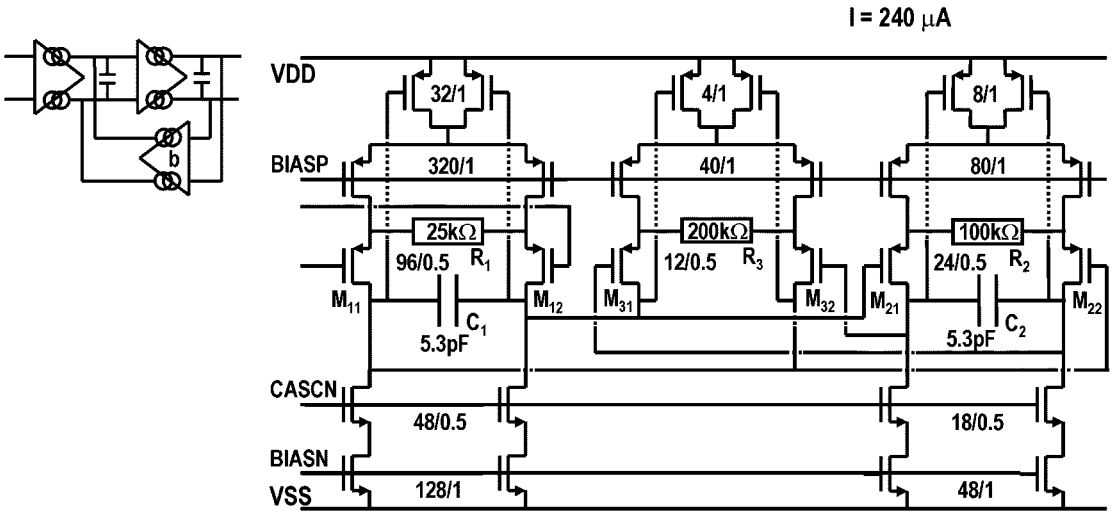


Fig. 11. Resonator implementation.

with $g_m = 4.3$ mA/V. It provides the virtual ground input nodes where the mixer can be conveniently implemented using nMOS switches, and where the DAC feedback current is subtracted from the input signal. Polysilicon resistors and gate-oxide capacitors are used. Nulling resistors in series with the integration capacitors compensate for the right-half plane zero that is introduced by this structure. The current consumption of the input stage, which is determined mainly by the noise and distortion requirements, is 500 μA. The resonator stages consist of two transconductor-C integrators and a feedback transconductor. The implementation is shown in Fig. 11. A first transconductor-C integrator is constructed by degenerated differential pair $M_{11}/M_{12}/R_1$, loaded by capacitor C_1. The second integrator is similar, consisting of M_{21}, M_{22}, R_2, and C_2. Feedback b is made by a third degenerated differential pair $M_{31}/M_{32}/R_3$. Its input is connected to the second integrator output, and its output current is subtracted from the output current of the first transconductor. The current consumption of a complete resonator is 240 μA. The feed-forward coefficients in Fig. 8 are implemented as degenerated differential pairs as well. Their outputs are added by simply connecting them. The quantizer is implemented by a cross-coupled latch with a folded cascode current-mode input stage [13]. The loop filter frequency characteristics are plotted in Fig. 12. Although the quality factors of the resonators are limited by the finite output impedance of the transconductors, still the resonances at 165 and 285 kHz are very useful to suppress the quantization noise in the signal band.

The maximum input signal of the ADC is 1.4 V_{pp} (differential). The input and feedback DAC resistors, which are 62.5 and 100 kΩ, respectively, dominate the circuit noise of the $\Sigma\Delta$ modulator. Some noise is added by the input amplifier and the rest of the loop filter, and also by the DAC reference voltage source. The total simulated equivalent input thermal noise floor

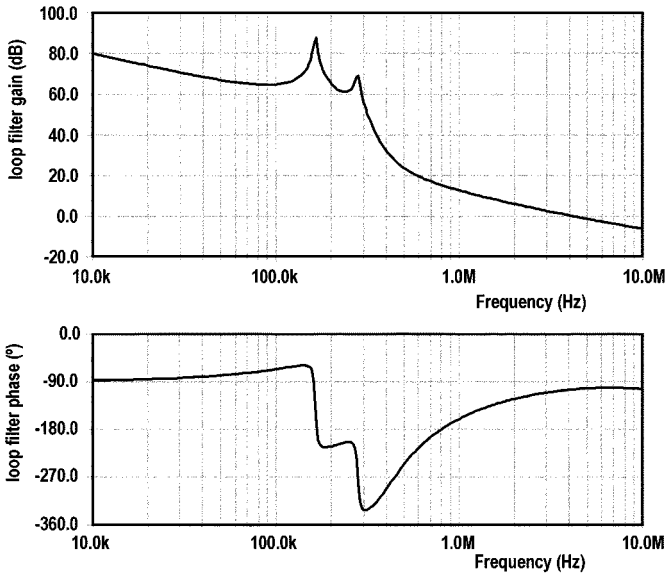


Fig. 12. Simulated fifth-order loop filter frequency characteristics.

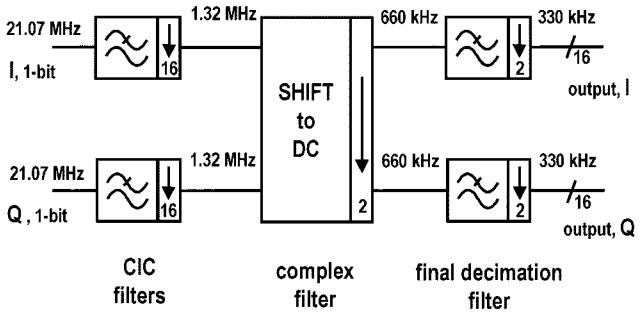


Fig. 13. Complex decimation filter block diagram.

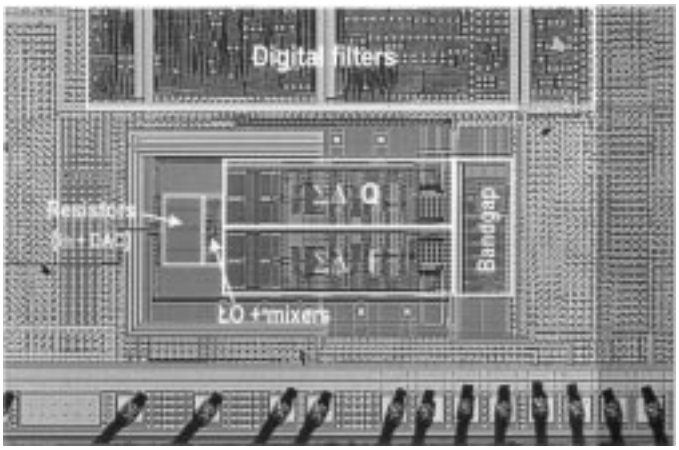


Fig. 14. 10.7 MHz IF ADC 0.25-μm CMOS prototype IC micrograph.

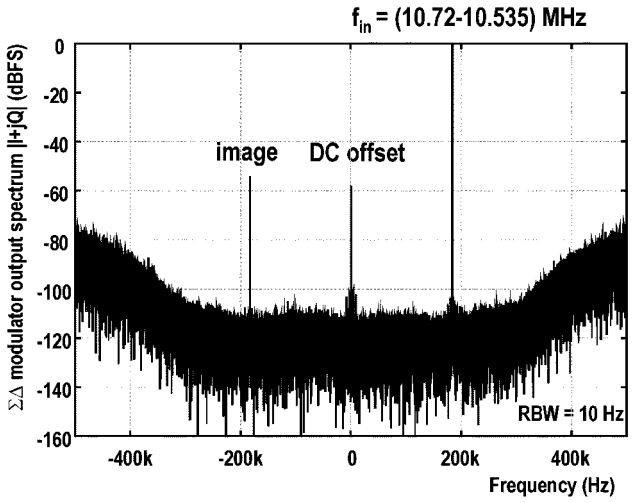


Fig. 15. Measured complex $\Sigma\Delta$ modulator output bitstream frequency spectrum ($I + jQ$).

is 99 dB in AM mode (9 kHz) or 85 dB in FM mode (200 kHz) below the maximum ADC input signal. Flicker noise is negligible in the signal band around the 165-kHz near-zero-IF. Fig. 13 shows the block diagram of the complex decimation filter. The 21.07 MHz I and Q $\Sigma\Delta$ modulator output bitstreams are first filtered by cascaded integrated comb (CIC) filters and decimated by a factor of 16. The output rate of these filters is 1.32 MHz. Then the signal band of interest around 165 kHz is mixed to dc and further decimated to 660 kHz. After that, final filtering and decimation to 330 kHz takes place.

V. Experimental Results

An IF ADC prototype IC was initially fabricated in a 0.35-μm standard digital CMOS process, including I and Q $\Sigma\Delta$ modulators with IF mixers, complex decimation filtering of the 200-kHz signal band around 165 kHz and the final shift to dc [17]. The circuit has been successfully scaled to a 0.25-μm CMOS process, which resulted in a smaller chip area of 1.35 mm^2 and lower power consumption. Fig. 14 shows a micrograph of the IF-ADC and part of the digital filters on the 0.25-μm CMOS prototype IC. The measurement results of this latest silicon are presented here. The output of the IC is 16 bits wide and contains the filtered baseband decimated to 330 kHz. The digital filters measure 0.75 mm^2 and the analog part, including bandgap reference, is 0.55 mm^2. The crystal oscillator is 0.04 mm^2. Careful layout of DAC, mixer and input stage is indispensable. Crosstalk from the large amount of quantization noise around half the sampling frequency toward the IF input must be minimized. Layout symmetry is essential to reduce gain and phase mismatch between the quadrature paths for best image rejection.

Both the 16-bit baseband outputs and the single-bit $\Sigma\Delta$ modulator outputs were measured. Differential current-mode output buffers were used for the bitstream outputs in order to minimize crosstalk. Fig. 15 shows a complex fast Fourier transform (FFT) of the output bitstreams ($I + jQ$) for a full-scale 10.72-MHz input signal. The input signal is mixed to 185 kHz, 20 kHz above the offset frequency. As expected, thermal noise dominates in the signal band of interest. Spurious frequency components are more than 100 dB below full-scale. Measured dynamic range is 97 dB in 9 kHz (AM) and 82 dB in 200-kHz (FM) bandwidths. Especially in AM mode, the maximum carrier-to-noise ratio (CNR) is important, since a rise of the noise floor caused by a large neighboring channel decreases the sensitivity for the wanted channel. Measured CNR is 94 dB in 9 kHz at the maximum differential input signal of 1.4 V_{pp}. The 3-dB

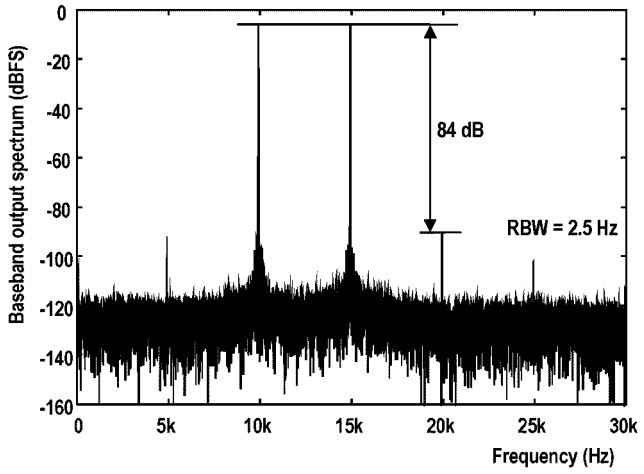


Fig. 16. Measured intermodulation distortion at baseband with −6 dBFS input signals at 10.710 and 10.715 MHz.

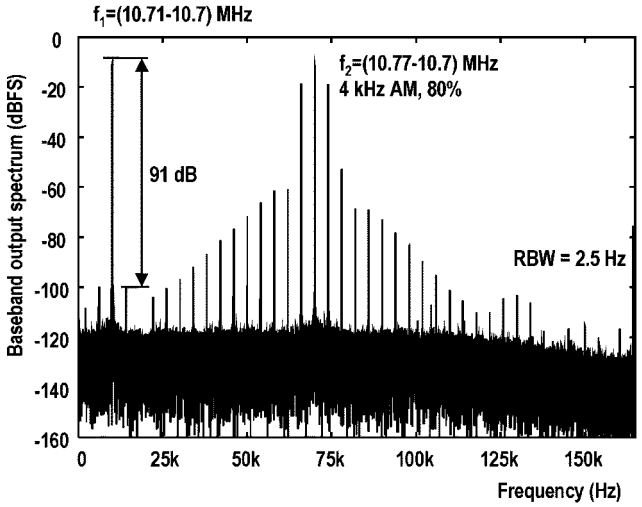


Fig. 17. Cross-modulation distortion measured at baseband with full-scale input signal.

increase of the in-band noise at maximum input is probably caused by distortion of the high-frequency quantization noise in the $\Sigma\Delta$ modulator loop filters. Fig. 15 also shows the offset at dc and the image frequency component at -185 kHz. The test ICs showed offsets with 0.7-mV standard deviation. Because of the near-zero IF mixing, this offset is outside the band of interest and removed by the complex digital decimation filter. Image rejection was measured over 20 samples from different batches. The gain mismatch between the I and Q paths is 0.7% or less, and is mainly caused by mismatch between the input and feedback DAC resistors of the $\Sigma\Delta$ modulators. Due to the re-clocking of the quadrature local oscillator signals LO_I and LO_Q with the master clock (see Fig. 7), the 90° phase difference between the I and Q paths appears to be very accurate. The phase error is 0.07° or less, so the gain mismatch is much more significant than the phase mismatch. Over the samples measured, the image rejection varies between 49 dB (corresponding to the worst-case gain mismatch of 0.7%) and 70 dB (apparently a sample with less than 0.06% gain mismatch and less than 0.04° phase mismatch). In the near-zero-IF AM/FM application, including the FM channel filter which is assumed to provide an additional image rejection of 40 dB, the image rejection is at least 89 dB, which is better than the target value of 80 dB.

Intermodulation distortion is especially important for AM input signals, since the input signal frequency band contains multiple AM channels. Distortion components of strong unwanted channels may deteriorate reception of the wanted channel. Intermodulation was measured by applying a full-scale IF input signal consisting of two 0.7 V_{pp} tones of 10.710 and 10.715 MHz, so that the ADC input signal is maximum. This measurement was performed at the baseband outputs of the prototype IC (see Fig. 16). The IM3 distance is 84 dB, and decreases rapidly for smaller input signals. Nonlinearity also leads to cross-modulation: modulation in the wanted signal band caused by a strong unwanted channel. This effect is well-known in AM receivers: when listening to a wanted channel that is not or weakly modulated, the modulation of a strong unwanted channel may be heard, and thus disturbs the reception of the wanted channel. It was measured with a full-scale input signal consisting of a 10.71-MHz unmodulated carrier (wanted), and a 10.77-MHz carrier modulated with 80%, 4 kHz AM (unwanted), both at -9 dB relative to full-scale. Again, the ADC input signal is maximum. Fig. 17 shows the output spectrum measured at baseband. Only the frequency components at 4-kHz distance of the unwanted carrier are of interest; the other frequency components are spurious of the signal generator and can be neglected. The cross-modulation distortion components are 91 dB below the carrier of the wanted signal. The cross-modulation also rapidly decreases for smaller input signals.

The total power consumption of the prototype IC is 36 mW from a 2.5-V supply voltage. A considerable amount of power, 15 mW, is consumed by the current-mode bitstream output buffers, which are only present for evaluation purposes, and do not contribute to the power consumption during normal operation. 8 mW is consumed by the IF ADC (two $\Sigma\Delta$ modulators), and 11 mW by the complex digital decimation filters, so the complete IF-to-baseband A/D conversion takes 19 mW. The crystal oscillator consumes 1.6 mW. Table I summarizes the performance of the IF ADC.

VI. Conclusion

A 10.7-MHz IF ADC with filtered digital baseband output for use in AM/FM radio receivers has been demonstrated. Instead of direct A/D conversion by a wide-band ADC or a bandpass $\Sigma\Delta$ modulator, the IF input signal is converted down to a low 165-kHz second IF frequency first, and then digitized by two fifth-order continuous-time $\Sigma\Delta$ modulators in quadrature. Thus, the A/D conversion takes place on a relatively low frequency, which is favorable for low power consumption. By implementing the downconversion passively at the $\Sigma\Delta$ modulator input virtual ground nodes, a very linear IF ADC is constructed. This technique was verified by a 0.25-μm prototype IC realization. The test IC includes digital filters for decimation and the final shift from near-zero-IF to dc, so it has 10.7-MHz IF input and filtered digital baseband output. Power consumption

TABLE I
IF A/D CONVERTER PERFORMANCE SUMMARY

Input IF	10.7 MHz	
Sampling rate	21.07 MHz	
Baseband output rate	330 kHz	
Full-Scale input voltage	1.4 V_{pp} (diff.)	
Input impedance	125 kΩ	
	AM (9 kHz)	**FM (200 kHz)**
Dynamic Range	97 dB	82 dB
Carrier-to-Noise (Full-Scale input)	94 dB	79 dB
IM3 distance (Full-Scale input)	84 dBc	
Cross-modulation (Full-Scale input)	-91 dBc	
Image rejection (20 samples)	> 49 dB	
I/Q gain error (20 samples)	< 0.7%	
I/Q phase error (20 samples)	< 0.07°	
Process	0.25μm, 1PS, 5AL, CMOS	
Supply voltage	2.5 V	
	ΣΔ ADC	**Dig. filters**
Power consumption	8 mW	11 mW
Chip Area	0.55 mm^2	0.75 mm^2

of the IF-to-baseband A/D conversion system is 19 mW. Dynamic range, carrier-to-noise ratio and linearity (see Table I) are sufficient for application of the IF ADC in AM/FM radios. Compared to a traditional AM/FM receiver, the number of analog components is reduced, and no specific analog AM channel filtering is necessary. This work has shown that less analog filtering in a radio receiver front-end may boost the ADC requirements considerably. Due to the AM multichannel aspect, the noise and linearity requirements for the AM/FM IF ADC were more difficult to meet in AM mode than in FM mode.

Further increase of the integration level of radio receivers, for example in mobile communication devices, enables cheaper solutions with lower component count. On the other hand, this implies less filtering in the radio front-end. On system level less filtering is even desirable, because it permits more flexibility for channel selection in the digital domain. This means that there will be a need for low-power multichannel ADCs for mobile communication applications. The bandwidth of such systems is usually wider than the bandwidth of the AM/FM receiver described in this paper. Therefore, the design of such multichannel ADCs with low power consumption will be a major challenge.

ACKNOWLEDGMENT

The authors would like to thank E. C. Dijkmans, L. J. Breems, F. Sessink, R. Ahn, J. van Valburg, and P. Rutten for many fruitful discussions on A/D conversion in radio receivers and assisting with system definitions and measurements. The digital filter design at ITCL, Leuven, Belgium, and the layout work at the Digital Audio Group of Philips Semiconductors, Nijmegen, The Netherlands, is also greatly appreciated.

REFERENCES

[1] J. W. Whikehart, "DSP-based radio with IF processing," presented at the SAE World Cong., Mar. 2000.
[2] L. Vogt, D. Brookshire, S. Lottholz, and G. Zwiehoff, "A two-chip digital car radio," in *ISSCC Dig. Tech. Papers*, Feb. 1996, pp. 350–351.
[3] S. A. Jantzi, W. M. Snelgrove, and P. F. Ferguson, "A fourth-order bandpass sigma–delta modulator," *IEEE J. Solid-State Circuits*, vol. 28, pp. 282–291, Mar. 1993.
[4] F. W. Singor and W. M. Snelgrove, "Switched-capacitor bandpass delta–sigma A/D modulation at 10.7 MHz," *IEEE J. Solid-State Circuits*, vol. 30, pp. 184–192, Mar. 1995.
[5] J. Park, E. Joe, M.-J. Choe, and B.-S. Song, "A 5-MHz IF digital FM demodulator," *IEEE J. Solid-State Circuits*, vol. 34, pp. 3–11, Jan. 1999.
[6] J. A. E. P. van Engelen, R. J. van de Plassche, E. Stikvoort, and A. G. Venes, "A sixth-order continuous-time bandpass sigma–delta modulator for digital radio IF," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1753–1764, Dec. 1999.
[7] A. K. Ong and B. A. Wooley, "A two-path bandpass sigma–delta modulator for digital IF extraction at 20 MHz," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1920–1934, Dec. 1997.
[8] I. Galton, W. Huff, P. Carbone, and E. Siragusa, "A delta–sigma PLL for 14-b 50-kSample/s frequency-to-digital conversion of a 10-MHz FM signal," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2042–2052, Dec. 1998.
[9] J. Crols and M. S. J. Steyaert, "Low-IF topologies for high-performance analog front-ends of fully integrated receivers," *IEEE Trans. Circuits Syst. II*, vol. 45, pp. 269–282, Mar. 1998.
[10] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 1998, pp. 558–559.
[11] L. J. Breems, E. J. van der Zwan, E. C. Dijkmans, and J. H. Huijsing, "A 1.8-mW CMOS ΣΔ modulator with integrated mixer for A/D conversion of IF signals," *IEEE J. Solid-State Circuits*, vol. 35, pp. 468–475, Apr. 2000.
[12] E. J. van der Zwan, "A 2.3-mW CMOS ΣΔ modulator for audio applications," in *ISSCC Dig. Tech. Papers*, Feb. 1997, pp. 220–221.
[13] E. J. van der Zwan and E. C. Dijkmans, "A 0.2-mW CMOS ΣΔ modulator for speech coding with 80-dB dynamic range," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1873–1880, Dec. 1996.
[14] F. Chen and B. Leung, "A 0.25-mW low-pass passive sigma–delta modulator with built-in mixer for a 10-MHz IF input," *IEEE J. Solid-State Circuits*, vol. 32, pp. 774–782, June 1997.
[15] S. A. Jantzi, K. W. Martin, and A. S. Sedra, "Quadrature bandpass ΔΣ modulation for digital radio," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1935–1950, Dec. 1997.
[16] ——, "Mismatch effects in complex bandpass ΔΣ modulators," in *Proc. 1996 IEEE ISCAS*, vol. 1, May 1996, pp. 227–230.
[17] E. J. van der Zwan, K. Philips, and C. A. A. Bastiaansen, "A 10.7-MHz IF-to-baseband ΣΔ A/D conversion system for AM/AM radio receivers," in *ISSCC Dig. Tech. Papers*, Feb. 2000, pp. 340–341.

Eric J. van der Zwan was born in Leiderdorp, The Netherlands, on March 22, 1965. He received the M.S. degree in electrical engineering from Twente University of Technology, Enschede, The Netherlands, in 1988.

In 1989, he joined the TNO Physics and Electronics Laboratory, Den Haag, The Netherlands, where he worked on radar signal processing. In 1990, he joined the Mixed-Signal Circuits and Systems Circuits Group, Philips Research Laboratories, Eindhoven, The Netherlands, where he worked on the design of high-resolution A/D and D/A converters and associated circuits for speech, audio, instrumentation, and radio applications.

He died in a traffic accident on August 1, 2000.

Kathleen Philips received the M.Sc. degree in electrical engineering from the Katholieke Universiteit van Leuven, Belgium, in 1995.

She then joined the Mixed-Signal Circuits and Systems Group of the Philips Research Laboratories, Eindhoven, The Netherlands. Her research interests include IF circuits, A/D and D/A conversion for audio systems, and radio receivers.

Corné A. A. Bastiaansen was born in Breda, The Netherlands, on August 4, 1962. He received the B.Sc. degree in electrical engineering from the Technical College, Breda, The Netherlands, in 1985.

He joined Philips Research Laboratories, Eindhoven, The Netherlands, in 1985. After working for two years in the field of photolithography, he joined the Analog Integrated Electronics Group, where he worked on the design of A/D and D/A converters for digital audio applications. In 1994, he joined the Digital Audio Group, Philips Semiconductors, Nijmegen, The Netherlands, where he continued his work on data converters. In 1997, he joined the Analog Module Service Group, Philips Semiconductors, Eindhoven, The Netherlands, where he is currently working on the design of CMOS analog circuits such as operational amplifiers, reference sources, A/D and D/A converters for digital audio, modem and radio receiver applications.