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Citation for published version (APA):

Bezooijen, van, A., Mahmoudi, R., & Roermund, van, A. H. M. (2005). Adaptive Methods to Preserve Power Amplifier Linearity under Antenna Mismatch Conditions. *IEEE Transactions on Circuits and Systems. I, Fundamental Theory and Applications*, 52(10), 2101-2108. <https://doi.org/10.1109/TCSI.2005.853254>

DOI:

[10.1109/TCSI.2005.853254](https://doi.org/10.1109/TCSI.2005.853254)

Document status and date:

Published: 01/01/2005

Document Version:

Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
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- The final published version features the final layout of the paper including the volume, issue and page numbers.

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Adaptive Methods to Preserve Power Amplifier Linearity Under Antenna Mismatch Conditions

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Abstract—Under antenna mismatch conditions at high output power, voltage clipping (due to collector voltage saturation) is the main cause of power amplifier linearity degradation. To preserve linearity under mismatch three adaptive methods are presented that make use of the detected minimum collector peak voltage. This detected signal controls either the amplifier output power, load-line, or supply voltage. These concepts are generalized analytically, and calculated results compare well to simulations. Measurements demonstrate an error vector magnitude reduction of 5% and an adjacent channel power ratio improvement of 10 dB at a voltage standing wave ratio of 4 for an EDGE amplifier with adaptively controlled output power. These adaptive methods offer a cost and size effective alternative to the use of an isolator.

Index Terms—Adaptive control, distortion, isolators, power amplifiers (PA).

I. INTRODUCTION

BANDWIDTH efficient modulation schemes are used for a rapidly increasing number of wireless applications. These modulation schemes impose, due to their nonconstant envelope, severe requirements on the linearity of power amplifiers (PAs) in mobile phones [1]. At high output power the amplifier linearity is strongly affected by the antenna environment and the battery supply, as is visualized in Fig. 1. Distortion, due to collector voltage saturation, is predominantly determined by the three quantities.

- A) *Output power*: When link budget is marginal, the base station requests for the phone to transmit more power (up to a maximum level). Consequently, the RF envelope of the collector voltage tends to become large.
- B) *Load-line*: Nearby objects that mutually couple with the antenna detune its resonant frequency and cause a change in load-line [2]. For a certain range of antenna mismatch phases the collector load impedance increases causing a RF collector voltage enhancement.
- C) *Supply voltage*: Collector voltage saturation is more severe when the PA supply voltage is low due to battery discharge.

Saturation of bipolar transistors causes hard clipping of the collector voltage. Consequently, strong deterioration of the

Fig. 1. Chain of causes and effects on PA distortion under antenna mismatch conditions showing that output power, load-line and supply voltage determine distortion due to collector voltage saturation.

error vector magnitude (EVM) and adjacent channel power ratio (ACPR) occur when no precautions are taken.

To preserve PA linearity under these extremes an isolator is commonly applied between the PA and antenna. It prevents the transistor from saturating by dissipating the reflected power in a load resistor that terminates the isolator third port [3]. However, to achieve cost and size reduction, “isolator-less” PA and transceiver concepts are of great interest to handset manufacturers.

In this paper, we present three adaptive methods to preserve PA linearity under mismatch. These methods are based on a control loop, embedding the PA, that is activated once collector voltage saturation of the bipolar RF power transistor tends to occur. We make use of the strong correlation between the detected minimum peak collector voltage and PA nonlinearity as described in a companion paper [4]. Because of their high level of integration, these concepts are low cost and small in size.

II. ADAPTIVE CONCEPTS

The adaptive concepts presented preserve linearity under mismatch by avoiding collector voltage saturation. Basic load-line calculations give the relationship between maximum output power, load impedance, and supply voltage.

The maximum power $P_{\text{col_max}}$ that can be delivered to the real part of the collector load impedance Z_{col} can be expressed as a function of the maximum collector signal voltage at which

Manuscript received August 31, 2004; revised February 2, 2005. This paper was recommended by Associate Editor W. A. Serdijn.

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Digital Object Identifier 10.1109/TCSI.2005.853254

clipping just occurs. This is determined by the supply voltage U_{sup} and the transistor saturation voltage U_{sat} according to

$$P_{\text{col_max}} = \frac{(U_{\text{sup}} - U_{\text{sat}})^2}{2 \cdot \Re\{Z_{\text{col}}\}}. \quad (1)$$

The collector load impedance is a function of the nominal collector load resistance R_{nom} and the collector reflection coefficient Γ_{col} , with magnitude $|\Gamma_{\text{col}}|$ and phase θ as follows:

$$Z_{\text{col}} = R_{\text{nom}} \cdot \frac{1 + |\Gamma_{\text{col}}| \cdot e^{j\theta}}{1 - |\Gamma_{\text{col}}| \cdot e^{j\theta}}. \quad (2)$$

The real part of the collector load impedance can now be worked out by rewriting Γ_{col} in its polar form $|\Gamma_{\text{col}}|(\cos(\theta) + j \sin(\theta))$, which yields

$$\Re\{Z_{\text{col}}\} = R_{\text{nom}} \cdot \frac{1 - |\Gamma_{\text{col}}|^2}{1 + |\Gamma|^2 - 2 \cdot |\Gamma| \cdot \cos(\theta)}. \quad (3)$$

By taking the derivative of the real part of Z_{col} to θ ,

$$\frac{\partial(\Re\{Z_{\text{col}}\})}{\partial\theta} = -R_{\text{nom}} \cdot \frac{2 \cdot |\Gamma_{\text{col}}| \cdot (1 - |\Gamma_{\text{col}}|^2) \cdot \sin(\theta)}{(1 + |\Gamma|^2 - 2 \cdot |\Gamma| \cdot \cos(\theta))^2} \quad (4)$$

and equating this to zero we find a minimum when θ equals $\pm\pi$ and a maximum when θ is zero. Thus, for a given power delivered to the load, the collector signal voltage will be largest when θ is zero. Consequently, this is the worst-case mismatch phase with respect to linearity. For this phase, the real part of the collector load impedance becomes proportional to the voltage standing wave ratio at the collector voltage standing wave ratio (VSWR) VSWR_{col}

$$\Re\{Z_{\text{col}}\}|_{\theta=0} = R_{\text{nom}} \cdot \text{VSWR}_{\text{col}}. \quad (5)$$

Substitution of (5) in (1) gives

$$P_{\text{col_max}} = \frac{(U_{\text{sup}} - U_{\text{sat}})^2}{2 \cdot R_{\text{nom}} \cdot \text{VSWR}_{\text{col}}}. \quad (6)$$

According to (6) the linearity under mismatch can be preserved by adapting the nominal maximum output power $P_{\text{col_nom}}$ (which corresponds to the maximum output power for a VSWR of one) by a factor proportional to the inverse of the VSWR at the collector

$$P_{\text{col_max_ad}} = \frac{P_{\text{col_nom}}}{\text{VSWR}_{\text{col}}}. \quad (7)$$

Alternatively, the nominal supply voltage $U_{\text{sup_nom}}$ (which corresponds to the minimum supply voltage for a VSWR of one) can be adaptively enhanced to $U_{\text{sup_ad}}$, given by

$$U_{\text{sup_ad}} = \sqrt{\text{VSWR}_{\text{col}}} \cdot (U_{\text{sup_nom}} - U_{\text{sat}}) + U_{\text{sat}} \quad (8)$$

to avoid collector saturation. In case of load-line adaptation the load-line will be adapted to its nominal value, $R_{\text{ad_to_nom}}$, and the collector VSWR_{col} will, of course, be reduced to one. Obviously, (6) can now be rewritten as

$$P_{\text{col_max}} = \frac{(U_{\text{sup}} - U_{\text{sat}})^2}{2 \cdot R_{\text{ad_to_nom}}}. \quad (9)$$

It is common practice to express output power as an average power delivered to the PA load. This average PA output

Fig. 2. PA transistor using an output power adaptation loop that avoids collector voltage saturation.

power $P_{\text{load_av}}$ is related to the maximum collector load power $P_{\text{col_max}}$, the modulation Crest Factor (CF), and the output matching network insertion losses IL_{match} according to

$$P_{\text{col_max}} = P_{\text{load_av}} \cdot 10^{(CF+IL_{\text{match}}/10)}. \quad (10)$$

Similarly, the magnitude of the collector reflection coefficient can be related to that at the load by

$$|\Gamma_{\text{col}}| = |\Gamma_{\text{load}}| \cdot 10^{-IL_{\text{match}}/10} = \frac{\text{VSWR}_{\text{load}} - 1}{\text{VSWR}_{\text{load}} + 1} \cdot 10^{-IL_{\text{match}}/10}. \quad (11)$$

When the antenna is mismatched and the output power is high, the relationships between output power, load-line, and supply voltage on one hand, and EVM and ACPR, on the other, are not straightforward. However, the strong correlation between the detected minimum peak collector voltage and nonlinearity [4] can be used as control criterion for an adaptive loop. This criterion can be expressed as

$$v_{\text{col_min}} > U_{\text{sat_NPN}} \quad (12)$$

in which $v_{\text{col_min}}$ is the minimum allowable instantaneous voltage at the collector of the NPN power transistor and $U_{\text{sat_NPN}}$ is its saturation voltage (typically 0.3 V). This criterion is used to adaptively correct either (A) the output power, (B) the load-line, or (C) the supply voltage of the PA.

A. Output Power Adaptation

Collector voltage saturation can be avoided by reducing the power, P_{load} , that is delivered to the load as illustrated in Fig. 2. The minimum collector peak voltage is monitored by a diode peak detector (that is weakly coupled to avoid introduction of distortion). When this detected minimum voltage falls below the threshold voltage V_{ref} , the track-and-hold circuit is triggered to increase its output voltage. Consequently, the gain of the variable gain preamplifier, located at the input to control the amplifier output power, is slightly reduced. This gain reduction limits the amplitude of the collector RF voltage and thus prevents saturation of the power transistor.

B. Load-Line Adaptation

The second method to preserve linearity is based on load-line adaptation as shown in Fig. 3. When the detected minimum collector peak voltage falls below the threshold voltage V_{ref} , the PA output match is adjusted to reduce the effective load impedance

Fig. 3. PA transistor using an output match adaptation loop that avoids collector voltage saturation.

Fig. 4. PA transistor using a supply voltage adaptation loop that avoids collector voltage saturation.

of the collector, which consequently reduces the magnitude of the collector voltage RF envelope.

C. Supply Voltage Adaptation

For the third method, based on supply voltage adaptation, a dc–dc converter is required that allows upconversion of the battery voltage to keep the RF-transistor out of saturation. As depicted in Fig. 4, the minimum collector voltage is again monitored by a diode peak detector and compared to a threshold voltage V_{ref} . Once the minimum collector voltage trips this reference voltage the dc–dc converter is actuated to increase the PA supply voltage.

III. SIMULATION RESULTS

To verify the adaptive methods, illustrated in Figs. 2–4 simulations are performed on these control loops using behavioral models. The RF-transistor is modeled as a voltage controlled current source according to the exponential behavior of a bipolar transistor. The model includes the base-collector junction behavior to represent collector voltage saturation.

Time-domain analysis results are presented showing the adaptation of the magnitude of the lower side envelope of an EDGE modulated collector voltage [5] that can be expressed as

$$v_{col}(t) = V_{Supply} + \sqrt{I^2(t) + Q^2(t)} \cdot \cos\left(\omega_0 \cdot t + \arctan\left(\frac{Q(t)}{I(t)}\right)\right) \quad (13)$$

for time moments t at which $\cos(\dots)$ equals -1 . $I(t)$ and $Q(t)$ represent the complex base-band signals modulating the carrier frequency ω_0 . Frequency spectra of the EDGE modulated carrier are given to illustrate differences in spectral regrowth.

A. Output Power Adaptation

Using envelope simulations, we initially determined the input power required to obtain a nominal output power of 28.6 dBm

Fig. 5. Simulated difference in the lower side collector voltage envelope for open loop and a closed loop adapting the output power. The corresponding VGA gain reduction is on the RHS Y axis. VSWR = 4, phase of Γ_{col} = 0 degrees.

in a 50- Ω load. The load impedance Z_{load} was changed to represent a VSWR of 4 at the output of the matching network. The worst-case phase of the mismatch was chosen such that a maximum collector load impedance occurs, corresponding to a reflection coefficient phase of zero degrees at the collector, as derived in (4). Fig. 5 depicts the resulting lower side envelope of the EDGE modulated collector voltage for an open, as well as closed, adaptive loop. The hard clipping that occurs in open loop is avoided once the loop is closed. The supply voltage is 3.5 V. On the right-hand side (RHS) Y axis, the gain reduction of the variable gain amplifier (VGA) is shown. We can clearly see the fast attack of the loop during the first 20 μ s, as well as the ripple that is caused by peaks in the envelope reactivating the track-and-hold circuit. The corresponding spectra, given in Fig. 6, show an impressive improvement in spectral regrowth.

With a harmonic balance simulation the behavior of the adaptive loop has been studied as a function of the phase of the mismatch as depicted in Fig. 7. The VGA control voltage $V_{control}$ -VGA reduces the gain by 4 dB/V. Obviously, the larger the

Fig. 6. Simulated difference in spectral regrowth between open loop and a closed loop adapting the output power. VSWR = 4, phase of Γ_{col} = 0 degrees.

Fig. 7. Simulated VGA control voltage as function of the load mismatch phase shows that the loop is activated over a limited range of mismatch phases. VSWR = 1, 2, 3, and 4.

Fig. 8. Simulated envelope of the collector voltage for open and closed loop while the load-line is being adapted. VSWR = 4, phase of Γ_{col} = 0 degrees. The load impedance at the collector is on the RHS Y axis, V_{supply} = 3.5 V.

VSWR the wider the range of phases over which the loop is activated to prevent the RF-transistor from saturating.

B. Load-Line Adaptation

In a very similar manner to the aforementioned, a control loop based on adaptation of the load-line has been described with behavioral models and verified, for the same conditions, with envelope simulations. The lower side envelope of the EDGE modulated collector voltage is shown in Fig. 8 for the open and closed-loop conditions. The hard clipping that occurs in the open loop is avoided once the loop is closed. The RHS Y axis shows that during the first 20 μ s the effective collector load

Fig. 9. Simulated difference in spectral regrowth between open loop and a closed loop adapting the load-line. VSWR = 4, phase of Γ_{col} = 0 degrees.

Fig. 10. Simulated envelope of the collector voltage showing clipping in case of open loop and supply voltage enhancement in case of closed loop condition. VSWR = 4, phase of Γ_{col} = 0 degrees.

Fig. 11. Simulated difference in spectral regrowth between open and a closed loop adapting the supply voltage. VSWR = 4, phase of Γ_{col} = 0 degrees.

resistance adapts from approximately 7.7 to 2.8 Ω . The corresponding spectra, given in Fig. 9, show an impressive improvement in spectral regrowth that is similar to that of the adapted output power case.

C. Supply Voltage Adaptation

In the same manner as described in the preceding sections, envelope simulations are performed to verify the effectiveness of supply voltage adaptation. The hard clipping that occurs in the open loop once again disappears when the loop is closed due to an increase in the supply voltage from 3.5 V to approximately 6.1 V (as is illustrated on the RHS Y axis of Fig. 10). The corresponding spectra, given in Fig. 11, show a similar improvement in spectral regrowth to the cases with power and load-line adaptation.

TABLE I
MAIN DIFFERENCES BETWEEN METHODS OF PRESERVING PA LINEARITY

	Method of preserving linearity	Load condition	Figures Obtained by	P _{out} [dBm]	V _{supply} [V]	Col. load [Ω]	ACPR [dBc]	EVM [%]
R-1	none	50 Ω	simulations	28.6	3.5	2.5	-59	2.5
R-2	none	4:1, $\arg(\Gamma_{\text{col}})=0$	simulations	27.3	3.5	7.7	-43	22
R-3	isolator	4:1, $\arg(\Gamma_{\text{col}})=0$	simulations	26.7	3.5	2.5	-59	2.5
A-1	output power adaptation	4:1, $\arg(\Gamma_{\text{col}})=0$	calculations	23.7	3.5	7.7	-	-
A-2	output power adaptation	4:1, $\arg(\Gamma_{\text{col}})=0$	simulations	24.1	3.5	7.7	-59	3.1
B-1	load-line adaptation	4:1, $\arg(\Gamma_{\text{col}})=0$	calculations	28.6	3.5	2.5	-	-
B-2	load-line adaptation	4:1, $\arg(\Gamma_{\text{col}})=0$	simulations	29.0	3.5	2.8	-58	2.5
C-1	supply voltage adaptation	4:1, $\arg(\Gamma_{\text{col}})=0$	calculations	28.6	5.9	7.7	-	-
C-2	supply voltage adaptation	4:1, $\arg(\Gamma_{\text{col}})=0$	simulations	28.6	6.1	7.7	-59	2.5

$IL_{\text{match}} = 0.7$ dB; $IL_{\text{isolator}} = 0$ dB.

IV. DISCUSSION

The main differences in calculated and simulation results between three reference cases R-1, R-2, and R-3 and the three presented adaptive methods will now be discussed and are summarized in Table I.

- R-1) For a nominal load condition of 50 Ω and an output power of 28.6 dBm an ACPR of -59 dBc and EVM of 2.5% are simulated at ± 400 kHz. These results are close to typical EDGE PA ACPR and EVM specifications of -57 dBc and 4% respectively.
- R-2) For a load VSWR of 4 and a phase of the reflection coefficient at the collector of zero degrees an ACPR of -43 dBc and an EVM of 22% is obtained when no precautions are taken. This severe distortion is due to the rather high output power in combination with the relatively high collector load impedance that is simulated at 7.7 Ω .
- R-3) When a loss-less isolator is placed between the PA and its load, the output power becomes 1.9 dB lower than under nominal load conditions and the collector load impedance remains approximately 2.5 Ω because the reflected power is now absorbed. The distortion remains as low as under nominal load conditions.
- A-1) For a load VSWR of 4 and a modeled matching network insertion loss of 0.7 dB the calculated VSWR at the collector equals, according to (11), 3.08. Consequently, the collector load resistance is $2.5 \cdot \sqrt{3.08} = 7.7 \Omega$. In case of output power adaptation the output power has to be reduced, according to (7) by $10 \cdot \log(3.08) = 4.9$ dB, to 23.7 dBm.
- A-2) In simulations the output power is adapted to 24.1 dBm. This is the net result of gain enhancement due to an increase in load-line on one hand, and gain reduction of the VGA on the other hand. ACPR and EVM are both rather similar to the values obtained under nominal load conditions, which indicates that the RF transistor is kept well out of saturation. The reduction in output power is a major disadvantage of this concept because the corresponding reduction in field strength might cause call drops. The dynamic range requirement on the preamplifier is rather small. Therefore, the IF or RF VGAs that are commonly used in a mobile phone to adjust its output power

over a wide dynamic range can be used as part of the adaptive loop. By reusing these circuit blocks a highly integrated low cost solution is obtained.

- B-1) When the load-line is adapted the VSWR at the collector reduces to 1 according to (6). It results in a nominal load impedance of 2.5 Ω and a nominal output power of 28.6 dBm.
- B-2) In simulations adaptation of the load-line gives an output power of 29.0 dBm. The loop corrects the collector load to approximately 2.8 Ω . It results in an output power that is $10 \cdot \log(2.8/2.5) = 0.5$ dB higher than for nominal load conditions. The simulated ACPR is -58 dBc and EVM is 2.5%. Thus, unlike protection by means of an isolator, load-line adaptation allows for linear operation up to the nominal output power.
- C-1) In the case of supply voltage adaptation linearity can be preserved, according to (8), by increasing the nominal supply voltage from 3.5 to 5.9 V for a collector VSWR of 3.08 (see A-1) and a saturation voltage of 0.3 V.
- C-2) The simulated loop corrects the nominal 3.5-V supply voltage to approximately 6.1 V. It results in linear operation at an average output power of 28.6 dBm. The increased power dissipation at enhanced supply voltage is a major drawback of this concept in comparison to load-line adaptation. To preserve the linearity under rapidly changing output power conditions, the response time of the base-band controller and dc-dc converter has to be sufficiently short. This poses severe requirements, especially on the speed of the dc-dc converter, which commonly use rather large inductors and capacitors to smooth the output voltage ripple and to suppress spurious signals. The use of supply voltage adaptation becomes more attractive once it is combined with PA efficiency enhancement methods that need downconversion of the supply voltage [7].

The small differences between calculated and simulated values are likely to be due to harmonic content in the collector voltage, differences in effective loop gain, parasitic emitter inductance and resistance, and other second-order effects.

Obviously, load-line adaptation is the best solution to preserve linearity under mismatch because it directly compensates

Fig. 12. PAM embedded in a control loop to adaptively preserve PA linearity under mismatch.

the mismatch. For cellular phone applications the severe requirements on insertion loss and linearity as well as on cost and size hamper the implementation of variable matching networks with technologies that are available today. However, emerging RF-MEMS technologies are expected to provide variable capacitors with relatively large tuning ranges, high Q-factors, and low distortion, which will allow for realization of low-cost miniaturized adaptive matching networks.

V. HARDWARE REALIZATION

To verify the effectiveness of an adaptively controlled PA hardware has been realized. The circuit diagram in Fig. 12 depicts a three-stage PA module (PAM) using a control loop that adaptively adjusts the output power of the amplifier. The detector output voltage, $V_{detector}$, representing the envelope of the minimum collector voltage of the last RF-stage, is fed to a voltage follower and comparator amplifier with a manually adjustable threshold voltage V_{ref} . This comparator controls the resistance of a MOS-transistor, used to rapidly charge the capacitor $Chold$ once the threshold level is crossed. A buffer amplifier controls the gain of the variable gain preamplifier BGA2031, to reduce its gain when the loop is activated.

The potentiometers P1 and P2 set the total variable gain range to approximately 10 dB, of which approximately 5 dB is actually used. The component values are chosen such that acquisition of the loop occurs well within one symbol period, whereas the decay time is made large to prevent the loop from reintroducing any amplitude distortion.

The PAM consists of two, fully independent, RF line-ups. For these experiments it has been populated for the 900-MHz band only, as is shown in Fig. 13. The first and second RF-stage are integrated into a 0.5- μm silicon bipolar driver IC that is visible

on the RHS. The power transistor and the minimum collector voltage peak detector are integrated into a second silicon die. On the left-hand side of the module the output matching network and the feeding choke with supply decoupling capacitors are visible. The module uses a 5-layer LTCC as substrate and its size is 11 mm $\times$ 13.75 mm [6].

VI. EXPERIMENTAL VERIFICATION

To verify the relationship between distortion and collector voltage saturation, load pull measurements have been performed on the PAM in open loop. The measured EVM and the detected voltage contours of $V_{detector}$ are depicted in Fig. 14.

The dotted circle, centered around the nominal load impedance of 50 Ω , represents a VSWR of 4. The closed contours near the center of the Smith chart show an optimum EVM of approximately 4%, whereas the dense EVM contours at the lower right part of the chart indicate significant distortion. The EVM contours are displayed with a step size of 1%. The voltage detector contours are approximately equally spaced over the entire Smith chart with maximum values in the upper left corner and minimum values in the lower right corner. Their spacing is 0.1 V. There is a strong correlation between maximum EVM and minimum detected collector voltage, as expected.

Open-loop as well as closed-loop EVM and ACPR measurements are carried out for an EDGE modulated signal. Initially, the output power is set at 28.5 dBm in a 50- Ω load by choosing the input power appropriately. A load mismatch is then applied with a VSWR of 4 while the phase of the mismatch is varied over 360 degrees. The measured EVM, depicted in Fig. 15, has a maximum at 180 degrees. By closing the adaptive control loop the maximum EVM is reduced from approximately 15% to 10%.

Fig. 13. Hardware demonstrator of the adaptively controlled PAM.

Fig. 14. Measured EVM and minimum collector peak voltage show a strong correlation. $P_{load} = 28.5$ dBm, Freq. = 900 MHz, and $V_{SWR} = 4$.

Fig. 15. EVM measured as a function of the phase of mismatch for open and closed loop. $V_{SWR} = 4$. P_{out} is set at 28.5 dBm at 50 Ω .

Fig. 16. ACPR measured as a function of the phase of mismatch for the same conditions.

Fig. 16 shows the measured ACPR for the same conditions. At 180 degrees the ACPR improves from approximately -43 dBc to -55 dBc by closing the loop. The loop reference voltage was set at approximately 0.9 V. For this chosen value, the loop activates the BGA2031 for mismatch phases between approximately 135 and 270 degrees. It reduces the VGA gain with a maximum of approximately 4.5 dB at 180 degrees mismatch, which is just sufficient to keep the PA out of strong saturation.

VII. CONCLUSION

In this paper, we proposed three methods to adaptively preserve PA linearity under antenna mismatch conditions. They make use of information derived from a minimum collector voltage peak detector to dynamically adjust either the output power, the collector load-line, or the supply voltage, to prevent a bipolar RF-transistor from saturating.

The three concepts are treated analytically, and calculated values compare very well to values obtained from simulations with behavioral models.

From these results, we conclude that all three adaptive methods preserve linearity equally well and, from a linearity point of view, there is no preference for one above the other. Moreover, there is no advantage in combining two or three loops because the required dynamic range of adaptation is small.

Output power adaptation is most attractive for application in the short term because it can easily be implemented with IC technologies that are commonly available. It requires only a small extension of the mobile phone power control function. A major drawback of this method, however, is the relatively low maximum output power that can be obtained for worst case mismatch phases.

Load-line adaptation is likely to provide the best overall compromise. An advantage of this method is that the maximum obtainable linear output power is larger than with the use of an isolator. However, linear, high- Q microelectromechanical systems devices must become available to allow the implementation of small size and low-cost adjustable output matching networks.

To make supply voltage adaptation economically more attractive than the use of an isolator, small size and low cost dc-dc converters first have to become available. Then they can probably be combined most advantageously with PA efficiency enhancement methods that need down-conversion of the supply voltage.

We have proven, by means of hardware, that the method of adaptively controlled output power is effective. Measurements on a three-stage EDGE PA demonstrate an EVM improvement from 15% to 10% and an ACPR improvement from -43 to -55 dBc at maximum power and an VSWR of 4 at worst-case mismatch phases.

ACKNOWLEDGMENT

The authors would like to thank all colleagues who contributed to the work covered in this paper. The enthusiastic support from F. van Straten is very much appreciated.

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