

A 3.5-mW, 2.5-GHz diversity receiver and a 1.2-mW, 3.6-GHz VCO in silicon on anything

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A 3.5-mW, 2.5-GHz Diversity Receiver and a 1.2-mW, 3.6-GHz VCO in Silicon on Anything

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Abstract—In this paper, first results of radio-frequency (RF) circuits processed in a novel silicon bipolar technology called silicon on anything (SOA) are presented. This technology was developed with the application of low-power, high-frequency circuits in mind. Three test IC's are discussed: A fully integrated 3.6-GHz voltage-controlled oscillator, a fully integrated 2.5-GHz diversity receiver front end, and an intermediate-frequency IC containing channel selectivity and demodulation circuits. Measurement results show that using this technology, significant power savings are possible for RF circuits.

Index Terms—Frequency divider, IF circuits, LNA, mixer, RF front ends, silicon on anything.

I. INTRODUCTION

THIS PAPER describes the first radio-frequency (RF) circuits designed in a novel silicon technology called silicon on anything (SOA) [1]. In this process, both active and passive devices are processed on a silicon-on-insulator (SOI) wafer. After processing, the wafer is glued to a new carrier. Now the original silicon substrate is removed by means of potassium hydroxide (KOH) etching down to the buried oxide layer of the SOI wafer. This transfer by glueing has been successful for a number of materials such as glass, alumina, ferroxcube, and Alsimag (which is an alloy of AlO₂, Ti and carbide), hence the reference to “anything” in SOA. These materials can be used to design on-chip passives with distinctive properties. Fig. 1 gives a schematic representation of the transfer process. Note that we are not growing Si onto another material but simply bonding it with a glue. The inverted bondpads shown in this figure can be protected from KOH attack by a thin layer of silicon nitride that is deposited before the back-end metallization.

The substitution of the substrate not only reduces substrate capacitances by a factor of five to ten but also allows the construction of a low-power, high-performance lateral bipolar device with standard lithography, as shown in Table I.

In Sections II and III, subcircuits of a fully integrated diversity transceiver designed in the SOA process will be described. To facilitate testing, this transceiver has been split up into a number of subblocks. Some conclusions regarding the technology and the circuits designed in it will be drawn in Section IV.

II. A FULLY INTEGRATED 3.6-GHz VCO AND TRAVELING WAVE DIVIDER

Using the technology described in Section I, we have fabricated several test IC's. The first contains an oscillator and

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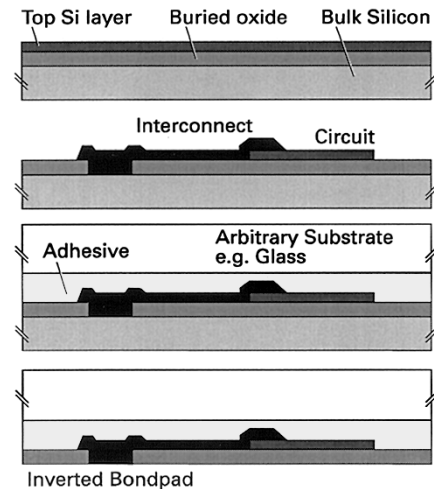


Fig. 1. Transfer process of circuits to glass.

TABLE I
KEY TRANSISTOR PARAMETERS FOR TWO COLLECTOR LENGTHS

Collector length	1.5 μm	1 μm	Unit
F _t	6.6	9.2	GHz
R _b	7.6	12.4	k Ω
C _{jc}	354	563	aF
C _{js}	550	550	aF
R _e	295	360	Ω
I _{Ft}	14	63	μA
V _{early}	24	24	V
β	80	85	

programmable divider chain for use in a synthesizer loop. A block diagram of the IC is drawn in Fig. 2. The divider chain consists of one traveling wave divider, three divide-by-two master-slave flip-flop prescalers, and 11 programmable divide-by-2/3 current-routing-logic dividers. With this chain, frequency division ratios between 32 768 and 65 520 can be programmed. The programmable dividers can be set with an 11-bit serial to parallel shift register. The outputs of the traveling wave divider are buffered and provide quadrature outputs at 1.8 GHz. A dummy divider cell is added after the second 1.8-GHz output to balance the circuit load on-chip, which improves I and Q matching. All circuits are biased by NPN bandgap references, and the total nominal current consumption for the IC is 800 μA , excluding the RF output buffers. The oscillator circuit topology is drawn in Fig. 3. It is a basic balanced oscillator that uses a cross-coupled differential pair and two emitter followers as a feedback amplifier. Each tail current equals 100 μA that feeds transistors with an area

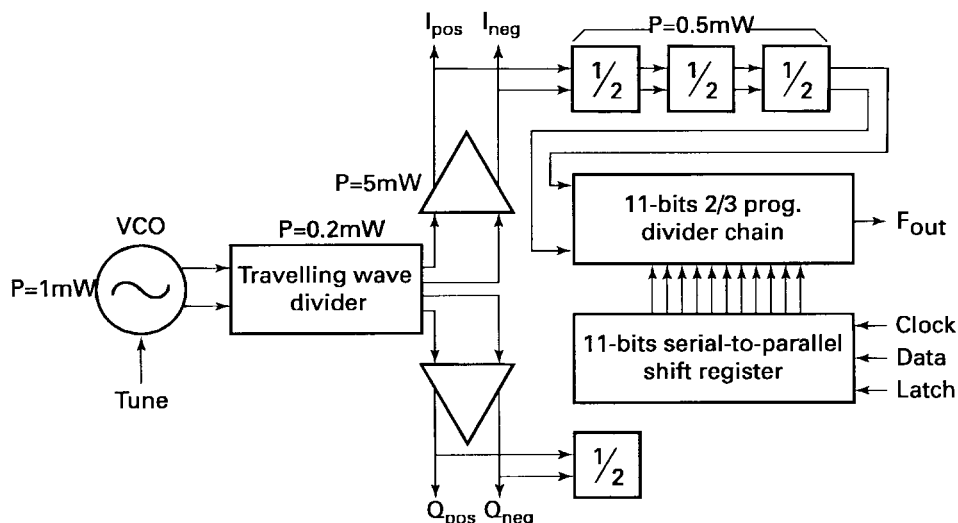


Fig. 2. Block schematic voltage-controlled oscillator/divider chain test IC.

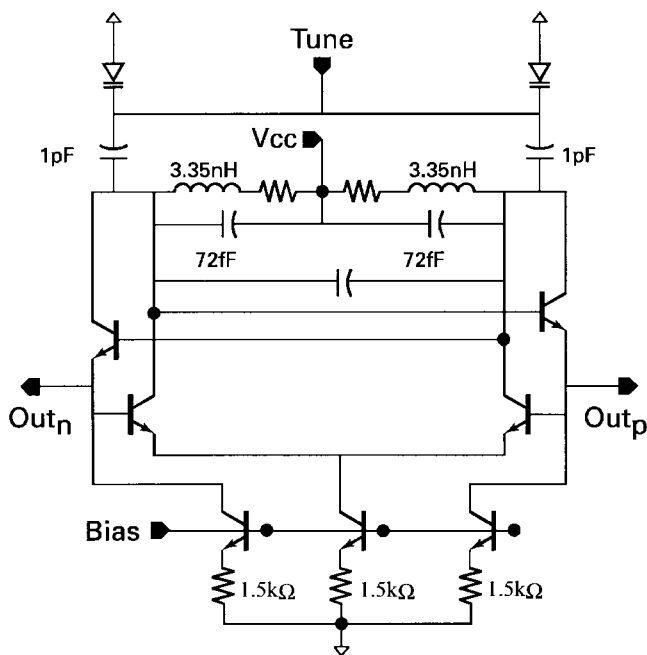


Fig. 3. Voltage-controlled-oscillator circuit topology.

factor of ten. The transistors with a collector length of $1.5 \mu\text{m}$ were chosen because they exhibit a higher input bandwidth at lower current levels. Two on-chip PIN diodes with a quality factor of 25 at 3.6 GHz are used as varactors. These diodes are capacitively tapped into the oscillator tank circuit. The diodes have a capacitance of 22–36 fF for 0–3.6-V reverse bias and allow the oscillator to be tuned over 25 MHz. If the diodes are coupled directly to the resonant circuit, oscillator frequency ratios of more than 20% should be possible. The inductors used in the resonant circuit have two turns, a track width of $40 \mu\text{m}$, spacing of $5 \mu\text{m}$, and a diameter of $600 \mu\text{m}$. The inductors are built up of a two-layer aluminum stack with a total thickness of $3.5 \mu\text{m}$. Before the RF circuits described in this paper were designed, a test mask containing many inductor geometries was processed and characterized. These measurements were then used to generate simple one-port models for use in ensuing

circuit simulations. For all these inductors, a clear resonance frequency could be observed. Fig. 4 shows the measured tank inductance and quality factor versus frequency. The resonance frequency of this inductor equals 10.5 GHz and is mainly set by the turn-to-turn capacitance now that the substrate has been removed. For simulation purposes, a simple one-port level crossing rate model has been fitted to the data, using fixed L and C values and a frequency-dependent resistance to account for skin effect. The fitted model showed a good agreement with the measurements at the frequency of interest. The derived model parameters are: $R(3.6 \text{ GHz}) = 2.3 \Omega$, $L = 3.35 \text{ nH}$, and $C = 72 \text{ fF}$. At 3.6 GHz, the inductor has a quality factor of 29. The two inductors are routed to provide a symmetric layout. In doing so, a negative mutual inductance is introduced, which increases the resonance frequency of the tank but decreases the tank Q . Three-dimensional electromagnetic simulations on the coupled geometry show, however, that this coupling coefficient is below 5%. Therefore, routing in favor of a symmetric layout was employed.

Phase-noise simulations show that the contribution to the phase noise of the emitter followers in the VCO circuit is similar to that of the differential pair. However, this configuration gives the largest possible bandwidth of the negative resistance ($-R$) amplifier cell. Laser cutting of the tank capacitor has shown that with this circuit and tank configuration, an oscillation frequency up to 4.8 GHz is possible. Fig. 5 shows the circuit topology of the traveling wave divider, which was optimized for high-frequency operation. The bottom differential pair splits the input sine wave from the voltage-controlled oscillator (VCO) into two antiphase currents. These currents are fed into a four-stage ring-locked oscillator, and a sine wave at half the input frequency propagates through the four coupled transistors. The collector currents of these transistors are 90° out of phase, so by a correct combination of currents, it is possible to generate balanced I and Q signals for a quadrature downconversion mixer pair. The traveling wave divider circuit only needs a single current source for correct operation. The quadrature outputs are decoupled from the division circuit by an additional four cascode transistors.

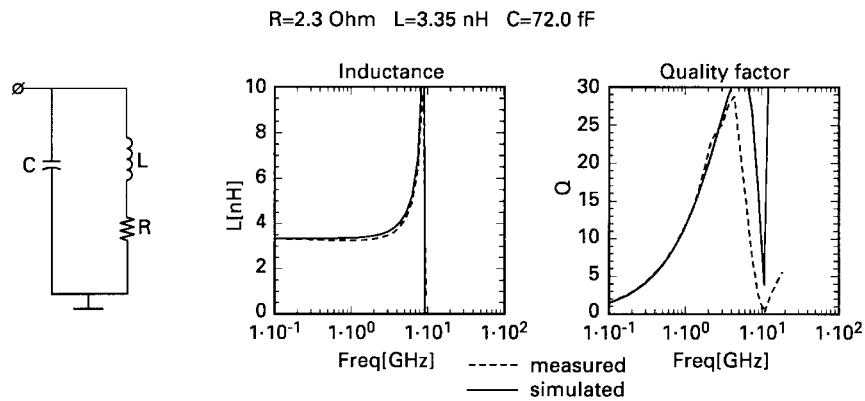


Fig. 4. Voltage-controlled-oscillator inductor performance.

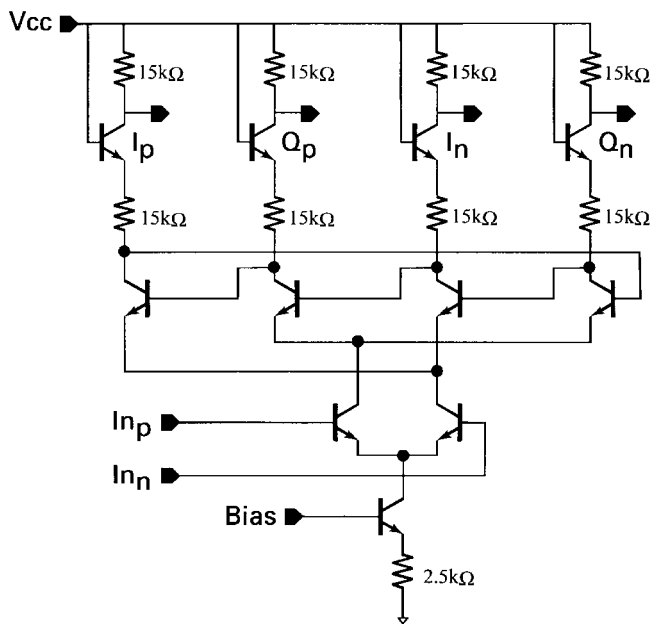


Fig. 5. Traveling wave divider circuit topology.

During experiments, it was possible to switch off the divider, hereby verifying that the 3.6-GHz signal indeed originates from the oscillator and is not a second harmonic of a 1.8-GHz oscillation of the traveling wave divider.

In Fig. 6, a plot of the divided oscillator output at 1.8 GHz is shown. This measurement was performed using a 30-kHz resolution bandwidth. A key figure derived from this measurement is a phase noise of -112 dBc/Hz at 2-MHz offset from the carrier, at a power consumption of 1.2 mW in total for both oscillator and traveling wave divider. The traveling wave divider consumes only $200 \mu\text{W}$.

Fig. 7 shows the oscillator power consumption and phase noise of several other publications on fully integrated VCO's in comparison to this work. For the phase noise, an extrapolation is made to enable a fair comparison: the theoretical phase noise at an offset that is equal to the oscillation frequency is calculated. This is done assuming a 6-dB/octave decrease in phase noise, according to Leeson's equation for oscillator phase noise [2]. Further, the reported results are normalized to a power consumption of 1 mW, under the assumption that the phase noise is inversely proportional to power consumption.

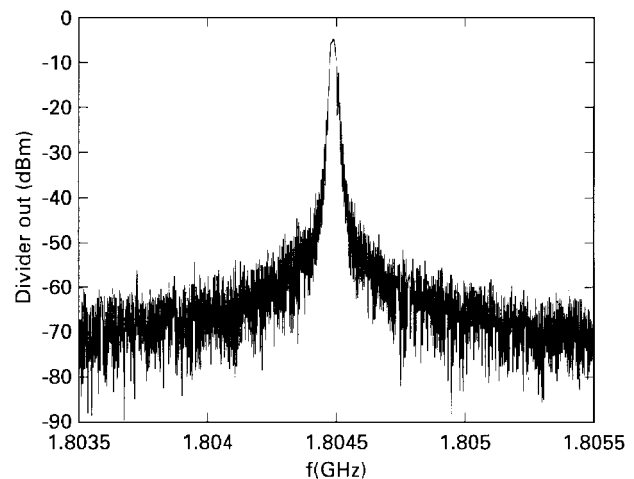


Fig. 6. Divided oscillator spectrum.

In this graph, horizontal lines represent circuits with equal performance. It is evident that this design compares well to the best of truly fully integrated silicon-based VCO's. Based on this result, extrapolations to more demanding applications and other frequencies can be made. Fig. 8 shows a microphotograph of a mounted VCO/divider chain IC. Clearly visible are the shadows of the two-turn coils on the die paddle. The total die size is 9 mm^2 , and standard wirebonding is used to mount the die in package or on a printed circuit board.

III. A 2.5-GHz DIVERSITY RECEIVER

Interfacing to external circuits is difficult for any low-power circuit because the impedance levels on-chip (in this design, between 5 and $50 \text{ k}\Omega$) will be much higher than the typical $50\text{-}\Omega$ off-chip levels. This can be solved through passive inductance-capacitance (LC)-type transformers and/or electronic buffer stages. Since the first solution consumes a lot of die area, and the second a lot of current, reducing the number of external connections is very important for low-power RF IC's. For this reason, a zero-intermediate-frequency (IF) architecture has been selected. This architecture also allows easy implementation of angle scanning diversity [3], [4]. Ideally, the total receiver, including the local oscillator (LO) generation and IF demodulation, would be implemented as a single IC.

The block diagram of the receiver is shown in Fig. 9. The front end consists of an input low noise amplifier (LNA) fol-

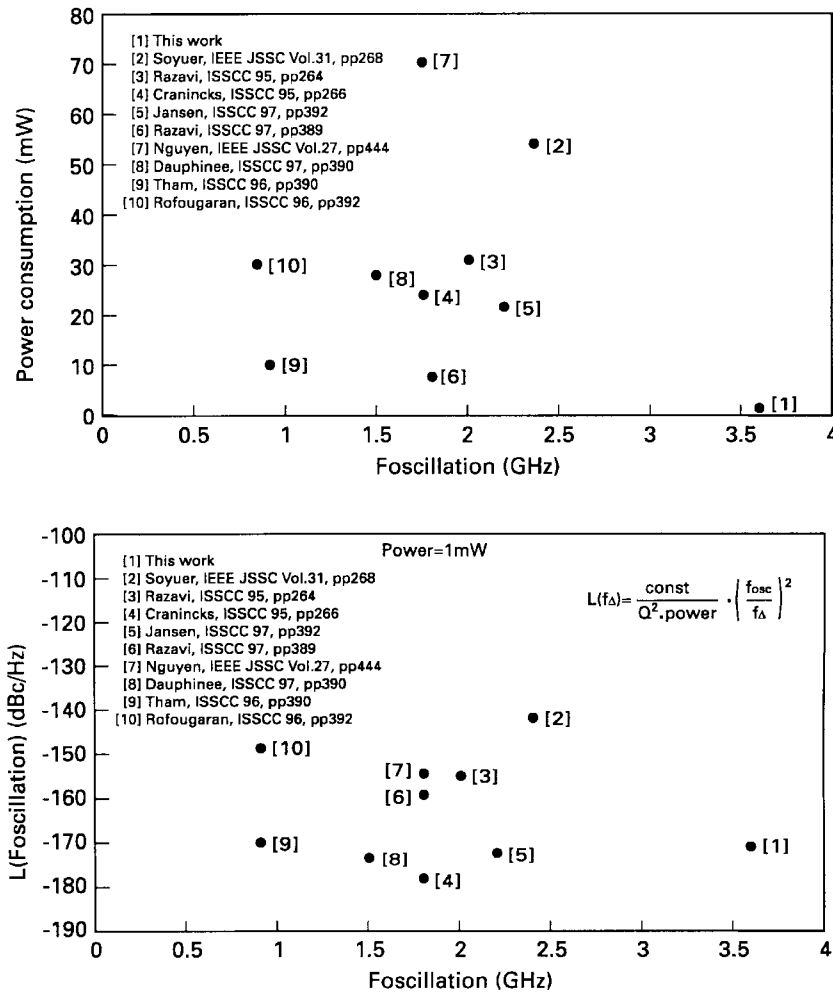


Fig. 7. Comparison of fully integrated VCO power consumption and phase noise.

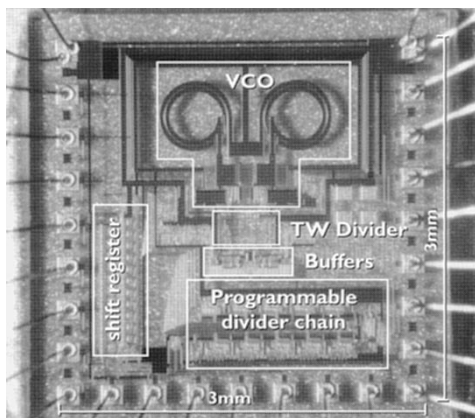


Fig. 8. Micrograph of VCO/divider IC.

lowed by quadrature mixers. The output of the mixers is processed by electronic phase shifters controlled by digital/analog (D/A) converters that are driven from two 8-bit shift registers. The phase shifted signals are then added to the signals from a second front end to achieve angle scanning diversity. The summed signals are further processed by dual IF stages.

A schematic of the LNA is drawn in Fig. 10. The RF input of the LNA uses a combination of LC circuits and electronic

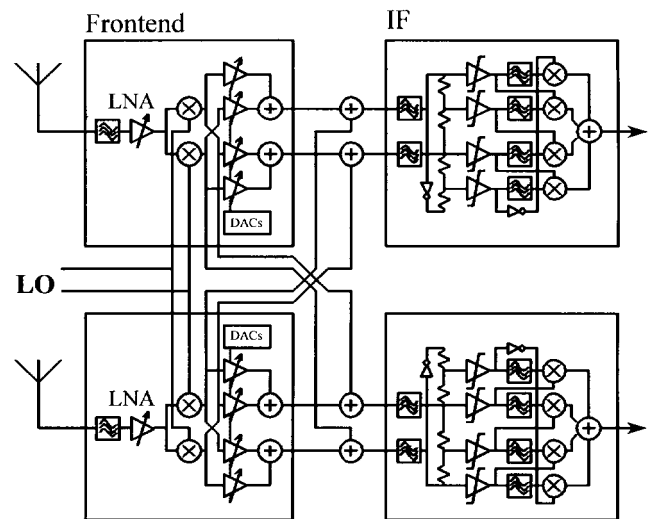


Fig. 9. Block schematic of dual beam antenna diversity receiver.

buffers to achieve the required impedance transform. This on-chip impedance transform also provide some immunity from out-of-band interferers. The impedance transform is implemented with an integrated LC-type transformer that feeds into a common base stage, T1 and T2 (2×7 transistors

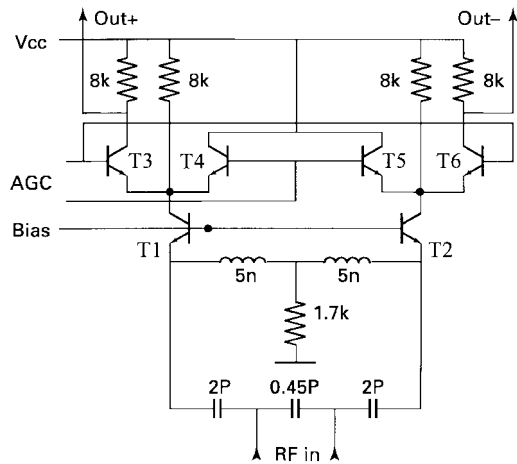


Fig. 10. LNA circuit diagram.

running at $24 \mu\text{A}$ each), with $300\text{-}\Omega$ input impedance. The output of this stage is connected to two differential pairs (T3–T6) that provide 40 dB of variable-gain operation. The output of these differential pairs feeds into the RF inputs of the mixers. The LNA provides 20 dB of voltage gain at $336 \mu\text{A}$ with a 4-dB noise figure and -20 dBm IIP3. The coils used in the LC matching circuits have three turns and a track width of $40 \mu\text{m}$ with a diameter of $600 \mu\text{m}$. The inductance value is 4.9 nH , and the Q equals 27 at 2.5 GHz with a self-resonance frequency of 8.8 GHz.

The LO inputs are implemented with electronic buffers. In a single-chip version of this receiver, the LO will obviously be an internal connection that does not need these buffers. The buffers provide 8.5 dB of gain. The mixers themselves provide 17 dB of gain, whereas the phase shifters have a maximum gain of 0 dB. The measured performance shows an overall conversion gain of 35 dB, with 6.2-dB noise figure and -22-dBm IIP3. Such an IIP3 is sufficient for low-dynamic-range systems such as Digital Enhanced Cordless Telecommunications and wireless local-area networks. The measured S11 at the input of the LNA was -12 dB . The supply current is 1.0 mA at 3.0 V, with about half that current going into the LNA and mixers and the other half into the D/A converters and phase shifters, which can be powered down independently. All circuits are biased by on-chip fully NPN bandgap reference sources. A microphotograph of the front end is shown in Fig. 11. The total die area of the front-end IC is 9 mm^2 .

A micrograph of the IF IC is shown in Fig. 12. Two of these IC's hook up directly to the diversity front ends, as drawn in Fig. 9. The IF IC consists of dual fourth-order active low-pass filters with a bandwidth of 100 kHz that provide channel selectivity, followed by interpolation and limiter stages that provide the IF gain and phase resolution.

To fit a high-bit-rate signal into a frequency-modulated channel (such as frequency-shift keying or Gaussian minimum-shift keying) with limited bandwidth, the frequency deviation is kept small, typically in the same order of magnitude as half the bit rate. When a zero-IF receiver architecture is used to receive such a signal, the IF signal will have very few zero crossings for each bit, typically one or less. The simplest IF circuits use limiters to provide gain and

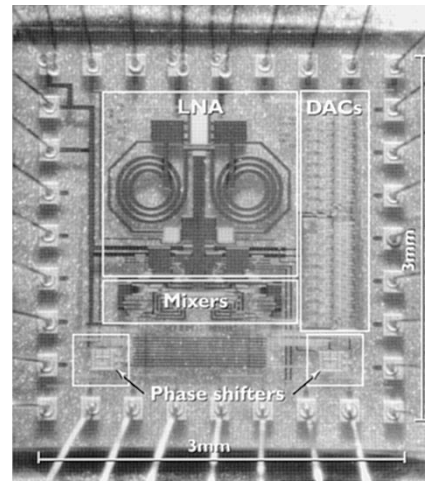


Fig. 11. Micrograph of diversity receiver.

automatic gain control. However, much information is lost in the limiting process for such small deviations in zero-IF systems. This can be solved by providing linear processing of the IF signal, but the resulting circuits are difficult to design and consume a lot of power. An alternative is to provide redundant IF signals at different phase shifts, e.g., 22.5° , 45° , 67.5° , or even smaller steps. When each of these IF signals is limited, the total number of zero crossings per bit increases. One way to look at this process is as a quantization of the phase with higher resolution. In this way, even systems with very small deviations relative to their bit rates can be implemented with zero-IF receivers. We have chosen a phase resolution of 22.5° , which implies eight IF signals, eight limiters, and an eight-channel frequency detector. A schematic of this setup is also included in Fig. 9. Because the IF signals are redundant, they can be derived from the I and Q signal by resistive interpolation rather than having to provide LO signals and mixers for each of these IF signals. This saves power and chip area. The demodulator is an extension of the differentiate and cross-multiply type of multiple phases, which provides one pulse for every zero crossing. The spacing in time of the pulses is inversely proportional to the IF frequency. Therefore, the frequency information of the IF signal can be approximated by an averaging process, e.g., a low-pass filter or an up-down counter similar to a pulse-counter demodulator. Since the simpler and lower power low-pass filter was sufficient for this system, this reconstruction has been implemented on the IF chip. The IF signals are converted to baseband information by a four-branch derivative and cross-multiply demodulator. This demodulator provides pulses at eight times the IF frequency, with positive pulses for positive frequencies and negative pulses for negative frequencies. The total measured supply current of the IF IC is $150 \mu\text{A}$ at 3 V, and the output signal of the demodulator is shown in Fig. 13.

IV. CONCLUSIONS

In this paper, the first RF receiver building blocks in the SOA process have been presented. They demonstrate the significant reduction in power consumption that can be achieved

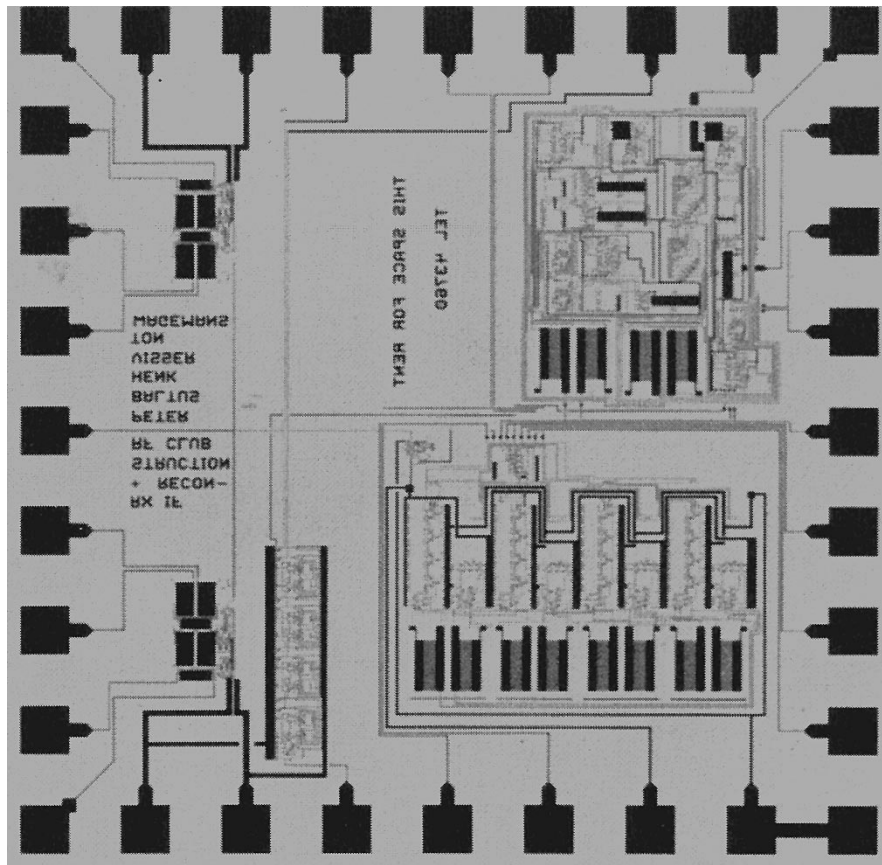


Fig. 12. Micrograph of IF IC containing channel selectivity and demodulators.

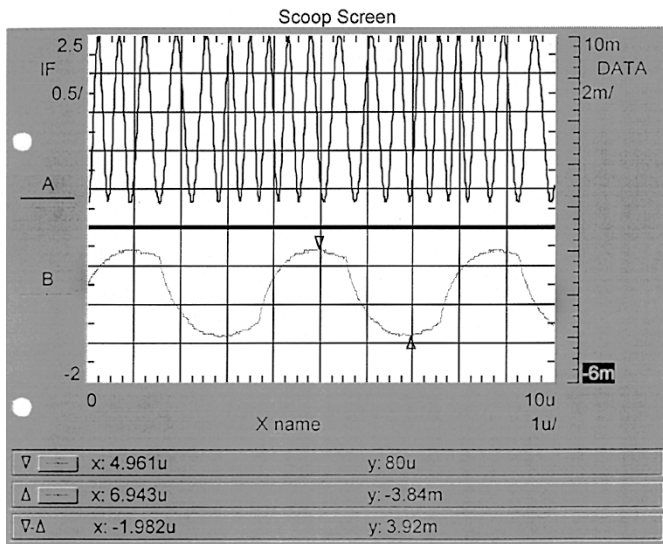


Fig. 13. Measured signal at output demodulator.

using SOA. The first IC is a fully integrated 3.6-GHz voltage-controlled oscillator with only 1-mW power consumption of the VCO itself. The second IC is a fully integrated 2.5-GHz zero-IF diversity receiver with on-chip RF selectivity consuming 3.5 mW. For testing purposes, these circuits were split up over a number of test IC's. The next focus will be to combine all RF signal-processing functions onto one IC. In doing so, we can eliminate the need for power-hungry signal buffers that are necessary to interface to a low-ohmic outside world. Designing

a low-power transceiver is not only a question of optimizing the IC technology for the circuits. Significant power savings can be achieved by considering higher level concepts such as angle scanning antenna diversity as well.

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