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An Alternative Design Flow for Receiver Performance Optimization through a Trade-off between RF and ADC

Wei Deng, Reza Mahmoudi, Pieter Harpe, Arthur van Roermund

Department of Electrical Engineering, Mixed-signal Microelectronics group, Eindhoven University of Technology, 5600 MB, Eindhoven, The Netherlands

Abstract — The lack of a systematic design strategy that can monitor the relation between RF blocks and ADC is one of the main obstacles for achieving overall system optimization. This paper presents an alternative design flow based on the translation of ADC parameters into the RF domain. This design flow indicates four variables that can be used for the trade-off between RF and ADC blocks. Associating these key variables to power consumption enables the trade-off between the block performance and system power consumption. The demonstrated capability of this method is illustrated by comparing two scenarios, related to the IEEE 802.11a standard.

Index Terms — System analysis and design, communication system performance, receivers, radio receivers, analog-digital conversion, power demand, IEEE 802.11a, wireless LAN, optimization methods.

I. INTRODUCTION

The rapid growth of wireless communication has resulted in a shift of RF applications towards high frequencies. The increased bandwidth and dynamic range requires a systematic design strategy for RF receivers. RF system engineers are mainly focusing on the performance and power consumption of RF front-ends. The lack of a proper relation between RF blocks and ADC has led to the over-specifications of these blocks and a non-optimized system [1].

Fig. 1 shows a simplified receiver chain including both RF front-end and ADC, where the interferers cause the dominant distortion. RF front-ends are usually characterized by noise figure (NF), power gain, third order input intercept point (IIP3) and power consumption [2]-[3]. The established theory enables the calculation of overall NF and IIP3 in cascaded RF blocks through the transformation of NF and IIP3 of each individual block. An extension of this theory enables the optimization of the overall power consumption through proper dimensioning of the individual RF blocks [3]. However, the main obstacles to a systematic design strategy for overall optimization are the lack of:

- a proper translation of ADC parameters to RF domain.
- a proper design flow reflecting the relation between RF and ADC blocks.

Fig. 1. Simplified receiver chain.

- a set of variables, enabling the proper dimensioning of individual block performance.

The scope of this paper is to introduce an alternative method for analyzing and optimizing the receiver performance. The capability of this method will be illustrated using an example based on the IEEE 802.11a standard.

II. TRANSLATION OF ADC PARAMETERS TO RF DOMAIN

A. Proposed ADC Model

The ADC component is modeled by two blocks: the global non-linearity block and the ADC noise block. For calculation purpose, this model is extended with a fictive and ideal DAC to translate the binary levels into analog domain. It is assumed that the transferred output analog signal has a unity gain, and no offset errors, compared to the input analog signal. This model is verified in ADS Ptolemy.

B. ADC Noise

From the perspective of an ADC designer, the parameters of interest are peak-to-peak full scale voltage (v_{FS}), sampling frequency (f_{sample}), and number of bits (n). The signal to quantization noise ratio (SQNR) of an ideal ADC with full scale sinusoid wave as input is given by $SQNR = 6.02 \cdot n + 1.76$ [4]. However, in reality, the ADC is not a stand-alone component; it is used in combination with the RF blocks in a receiver chain. From this perspective, the parameters of interest can be described as full scale input signal power (P_{FS}), sampling frequency (f_{sample}), ADC signal to noise ratio (SNR_{adc}), channel bandwidth (BW), and ADC noise figure (NF_{adc}) as

Fig. 2. (a) Translated ADC noise parameters to RF domain. (b) Translated ADC non-linearity parameters to RF domain.

shown in fig. 2(a). It is more suitable to use effective number of bits ($ENOB_{noise}$) instead of n , because it includes both ADC quantization noise and thermal noise, assuming that quantization noise behaves the same as thermal noise and has no correlation with the signal. In this case, one can write: $SNR_{adc} = 6.02 \cdot ENOB_{noise} + 1.76$. After proper derivation, NF_{adc} can be expressed as:

$$NF_{adc}[dB] = P_{FS}[dB] - \left[SNR_{adc} + 10\log\left(\frac{f_{sample}}{2 \cdot BW}\right) + 10\log(kT \cdot BW) \right] \quad (1)$$

C. ADC Non-linearity

Non-linearity is the other major concern in ADC design. In a typical design, there are two parameters of interest, firstly, the effective full scale voltage ($v_{FS,eff}$), and secondly, the total harmonic distortion (THD). However, from RF system perspective, interferer signals often cause the dominant distortion (see Fig. 1). Thus the third order input intercept point $IIP3_{adc}$ can be used to describe ADC global nonlinear property as shown in fig. 2(b). $IIP3_{adc}$ is a function of the fundamental output interference signal ($P_{Int,out}$), output third order intermodulation distortion product ($P_{IM3,adc}$) and power gain of the ADC (G_{adc}). Considering the unity gain of the ADC, one can express $IIP3_{adc}$ as:

$$IIP3_{adc}[dBm] = OIP3_{adc} = \frac{IM3_{adc}^{-1}}{2} + P_{Int,out} = \frac{3}{2} P_{Int,out} - \frac{1}{2} P_{IM3,adc} \quad (2)$$

Where $(IM3_{adc})^{-1}$ is the ratio between $P_{Int,out}$ and $P_{IM3,adc}$. Equation (2) expresses $IIP3_{adc}$ with signal dependent parameters, which is not very convenient for describing ADC inherent block properties. For further expressing $IIP3_{adc}$ with signal independent ADC block parameters, some definitions need to be introduced. To guarantee the integrity of the signal, two auxiliary parameters, ΔP_1 and ΔP_2 are usually introduced. $P_{FS} - \Delta P_1$ indicates the ADC effective input full scale power, which is the counterpart

of $v_{FS,eff}$, and depends on the ADC architecture. $P_{FS} - \Delta P_1 - \Delta P_2$ is the input interferer power (by each tone). ΔP_2 is the ratio between input interferer power and ADC effective input full scale power. Power series expansion [2] is used to translate signal dependent parameters $P_{Int,out}$ and $P_{IM3,adc}$ to ADC block parameters $P_{FS} - \Delta P_1$ and P_{HD3} , respectively. P_{HD3} is the power of the third order harmonic with ADC effective input full scale power ($P_{FS} - \Delta P_1$) as stimulus. Assuming P_{HD3} dominates all the distortion harmonics, and $P_{FS} - \Delta P_1 \gg P_{HD3}$, we have:

$$P_{Int,out} = P_{Int,in} = P_{FS} - \Delta P_1 - \Delta P_2 \quad (3)$$

$$P_{IM3,adc} = P_{dist,adc} = P_{HD3} - 3\Delta P_2 + 20\log 3 \quad (4)$$

The constant $20\log 3$ is obtained from one to one relation between the third harmonic and the third intermodulation distortion product. Substituting equation (3) and (4) into equation (2) and cancelling ΔP_2 , leads to reformulation of $IIP3_{adc}$ as:

$$IIP3_{adc}[dBm] = \frac{3}{2} (P_{FS} - \Delta P_1) - \frac{1}{2} P_{HD3} - 4.77[dB] \quad (5)$$

III. TRADE-OFF BETWEEN ADC AND RF SYSTEM PARAMETERS

In many cases, the system performance is defined as a prescribed BER, which is a function of signal to noise and distortion ratio (SNDR). SNDR can be again separated into SNR and SDR, in order to distinguish the contribution of noise and distortion, and enables the possibility of trade-off for an optimum performance. From this perspective, it is very important to analyze the impact of ADC noise and distortion on the performance of the system SNR and SDR. Assuming the phases of the distortion components of different stages uncorrelated [3], the equivalent total noise and distortion power of the system can be formulated as:

$$P_{noise,tot}[dBm] = P_{noise,adc} + \Delta P_{noise,FE} \quad (6)$$

$$P_{dist,tot}[dBm] = P_{dist,adc} + \Delta P_{dist,FE} \quad (7)$$

where $\Delta P_{noise,FE}$ and $\Delta P_{dist,FE}$ are the noise and distortion contribution by the RF front-end referred to ADC input and output, respectively (will be explained in equation (15) and (16)). Defining $P_{S,in}$ and $P_{S,out}$ as the signal power at the ADC input and output, one can formulate SNR and SDR as:

Fig. 3. ADC to system mapping for noise and distortion.

Fig. 4. Receiver signal, noise and distortion flow diagram.

$$SNR[dB] = P_{S,in} - P_{noise,tot} = P_{S,in} - (P_{noise,adc} + \Delta P_{noise,FE}) \quad (8)$$

$$SDR[dB] = P_{S,out} - P_{dist,tot} = P_{S,out} - (P_{dist,adc} + \Delta P_{dist,FE}) \quad (9)$$

Combining equation (8) and (9) with the results achieved in previous sections, enables the embedding of ADC into the overall system characterization as depicted in fig. 3. The X- and Y-axes represent the input and output of the ADC, respectively. The X1- and Y1-axes are the ADC block parameters as shown in fig. 2(a) and 2(b), respectively. On the X-axis, we can recognize: the noise contributions of RF front-end and ADC, the signal power, and the input interferer power $P_{Int,in}$ as shown in equation

(3). $P_{Int,in}$ causes a distortion signal $P_{dist,adc}(=P_{IM3,adc})$ in the desired channel. This distortion signal is a function of $IIP3_{adc}$ and $P_{Int,out}$ as formulated in equation (2). Assuming a G_{adc} of 0dB, we can recognize the following parameters on the Y-axis: $OIP3_{adc}$, output interferer power $P_{Int,out}$ as shown in equation (3), output signal power, and distortion contributions of RF front-end and ADC. From fig. 3, we can rewrite SNR for the total system as:

$$SNR[dB] = P_{S,in} - [10\log(kT \cdot BW) + NF_{adc} + \Delta P_{noise,FE}] \quad (10)$$

Combining equation (2) and (3), yields:

$$P_{dist,adc} = P_{IM3,adc} = 3(P_{FS} - \Delta P_1 - \Delta P_2) - 2IIP3_{adc} \quad (11)$$

Substituting equation (11) into equation (9), we can rewrite SDR for the total system as:

$$SDR[dB] = P_{S,out} - [3(P_{FS} - \Delta P_1 - \Delta P_2) - 2IIP3_{adc} + \Delta P_{dist,FE}] \quad (12)$$

IV. DESIGN FLOW FOR RF CHAIN

The predefined specifications of wireless standards are determining today's design strategy. Standards usually include: bandwidth of the signal (BW), minimum signal to noise and distortion ratio ($SNDR_{min}$) (derived from BER and modulation scheme), minimum detectable signal power ($P_{S,min}$), desired signal power ($P_{S,want}$) and interferer power (P_{Int}) for intermodulation characterization. This allows us to determine the receiver total noise figure and total input intercept point, as:

$$NF_{tot}[dB] = P_{S,min} - SNDR_{min} - 10\log(kT \cdot BW) \quad (13)$$

$$IIP3_{tot}[dB] = \frac{P_{Int} - P_{S,want} + SNDR_{min}}{2} + P_{Int} \quad (14)$$

Furthermore, the type of ADC dictates P_{FS} , ΔP_1 and ΔP_2 , which in turn fixes the interferer power level at the input of ADC ($P_{Int,in}$).

Optimizing the overall performance of the receiver chain demands a proper design flow, containing fixed parameters and variables. Fig. 4 represents such a flow diagram for receiver signal, noise and distortion. Note that $P_{S,min,in} = P_{S,in}$, $P_{S,want,out} = P_{S,out}$, and $SNDR_{min} = SNR = SDR$, where the latter parameters are the parameters at input and output of ADC (see Fig. 3). This flow consists of three fronts: antenna, input, and output of ADC. From this perspective, one can define the power gain of RF front-end as the ratio between P_{Int} and $P_{Int,in}$. Utilizing the NF relation of a cascade (RF front-end plus ADC), and using equation (10), one can relate NF_{FE} to $\Delta P_{noise,FE}$ as:

$$\Delta P_{noise,FE} = P_{S_{min,in}} - SNDR_{min} - 10 \log(kT \cdot BW) - 10 \log \left(10^{\frac{NF_{tot} + G_{FE}}{10}} - 10^{\frac{NF_{FE} + G_{FE}}{10}} + 1 \right) \quad (15)$$

Similarly, through the cascade relations of IIP3 and equation (12), IIP3_{FE} and ΔP_{dist,FE} can be related as:

$$\Delta P_{dist,FE} = P_{Swant,out} - SNDR_{min} - 3(P_{FS} - \Delta P_1 - \Delta P_2) - 10 \log \left[10^{\frac{IIP3_{tot} + G_{FE}}{5}} - 10^{\frac{IIP3_{FE} + G_{FE}}{5}} \right] \quad (16)$$

Thus, there are four variables, NF_{adc}, ΔP_{noise,FE} and IIP3_{adc}, ΔP_{dist,FE} as emphasized in fig. 4, which can be used to trade-off between RF front-ends and ADC to achieve the system requirements. These variables enable:

- the trade-off between the RF front-end and ADC performance.
 - the adaption of RF front-end and ADC performance for different system specifications.
- If the functions of these variables versus power consumption of their described blocks are given, they again enable:
- the trade-off between RF front-end and ADC performance for minimum system power consumption.
 - the comparison of individual block with different designs or different technologies, to find minimum system power consumption.

V. EXAMPLES

Allowing a P_{FS} of 4dBm (50Ω), a ΔP₁ of 1dB, a ΔP₂ of 6dB, an f_{sample} of 640MS/s and a BW of 20MHz, table I shows two scenarios with different combinations of NF_{adc}, ΔP_{noise,FE} and IIP3_{adc}, ΔP_{dist,FE} for a receiver system following the IEEE 802.11a standard. Scenarios A and B correspond to a relaxed configuration for the RF front-end and the ADC, respectively. The impact of the choice between these scenarios on the system power consumption can be investigated through the following relation [5]:

$$P_{sys} = P_{C,FE} \cdot (IIP3_{FE} - P_{noise,FE}) + P_{C,adc} \cdot (IIP3_{adc} - P_{noise,adc}) \quad (17)$$

where P_{C,FE} and P_{C,adc} denote the power coefficient of the front-end and ADC, respectively. For a flash type of ADC, P_{C,adc} is dominant over P_{C,FE}. This implies that scenario B has a lower system power consumption than scenario A, when a flash ADC is used.

Table II shows the impact of ADC on overall system performance if the channel bandwidth of standard IEEE802.11a is fictively increased to 200MHz. Keeping the key ADC design parameters SNR_{adc}, f_{sample} and IIP3_{adc}

constant, one can see from table II that the required noise figure of RF front-end is decreased to 5.8dB. In this case,

TABLE I. EXAMPLE OF TWO SCENARIOS

		Scenario A: Relaxed front-end	Scenario B: Relaxed ADC
ADC	NF _{adc}	43dB	55dB
	IIP3 _{adc}	21.7dBm	17dBm
	SNR _{adc}	50dB (8bits)	38dB (6bits)
	IIP3 _{adc} - P _{noise,adc}	66.5dB	63dB
Front-end	ΔP _{noise,FE}	14dB	2dB
	ΔP _{dist,FE}	11.4dB	2dB
	NF _{FE}	14.8dB	10.7dB
	IIP3 _{FE}	-25.8dBm	-23.8dBm
	IIP3 _{FE} - P _{noise,FE}	60.4dB	79.7dB

TABLE II. BROADBAND COMMUNICATION EXAMPLE

	BW= 20MHz	BW= 200MHz
10log(f _{sample} /2*BW)	12dB	2dB
NF _{tot}	15dB	8dB
NF _{FE}	14.8dB	5.8dB

the ADC has a crucial impact on the system performance. To optimize power of the new system, the design flow introduced in the previous sections can be used.

VI. CONCLUSION

This paper has presented an alternative design flow for trade-off between RF front-end and ADC block performance by translating ADC parameters into RF domain. This approach indicates four variables for achieving optimum power consumption in a receiver chain. Associating these variables to the power consumption enables the trade-off between RF and ADC block for minimum overall power consumption.

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