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Quad Active-Bridge Single-Stage Bidirectional Three-phase AC-DC Converter with Isolation: Introduction and Optimized Modulation

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Abstract—This paper introduces the quad active-bridge (QAB) ac-dc converter, which provides isolation and bidirectional power flow in a single-stage topology. While Matrix-based topologies commonly use bipolar voltage switches, the proposed solution allows the use of unipolar voltage switches. Compared to a six-switch PFC, the average voltage stress is reduced by a factor two. A modulation scheme is derived for this converter, that is analytically optimized towards minimum conduction losses to improve the conversion efficiency. The modulation scheme consists of closed-form algebraic solutions such that no look-up tables are required for implementation. Considerations for converter design and the main component selection procedures are given. The proposed topology and modulation strategy is implemented in a 20 kW prototype. Measurements are conducted and show that the methods operate as expected. Experimental results show that the load step is stable, the power factor is close to unity, and the phase current THD is than 5%. Lastly, it is shown that the circulating current can be controlled independent of the output power. The methods and tools provided can be used for the design and analysis of ac-dc power converters based on the QAB-topology.

Index Terms—power conversion, ac-dc converters, three-phase electric power

I. INTRODUCTION

HIGH-performance ac-dc power converters are required in a broad range of applications to allow, for example, electric cars to be recharged, solar panels and wind turbines to deliver energy to the grid, and high-voltage dc grids to operate. Various topologies exist for these applications [1]–[7]. In some cases, for example in a battery charger for an electric car, the power can even flow in both directions: charging using solar energy during daytime and powering the household during the night, when the solar panels are inactive. To ensure safety and low leakage currents, galvanic isolation between energy sources is commonly desired, but often is not implemented due to the additional cost and complexity.

The quad active-bridge (QAB) converter for three-phase ac-dc conversion allows bi-directional power flow and galvanic isolation [8]. No intermediate high-voltage bus is used, and no bipolar voltage switches are required. Furthermore, the average voltage stress is a factor two lower when compared to a regular six-switch inverter. This makes the converter highly competitive for applications where high-power, compact, and low-cost solutions are desired. While the existing phase-shift modulation scheme does result in soft-switching operation,

the circulating currents can be high and significantly limit the conversion efficiency.

This paper describes the power-balance control method for the QAB topology. This method employs an algebraically optimized modulation scheme to minimize the circulating current. Moreover, it is made possible to scale the circulating current independent from the AB output currents to, for instance, actively control the thermal stress of active and passive components.

Outline

This paper focuses on introducing the quad active-bridge ac-dc converter topology, proposes a modulation strategy and contains experimental verification. The paper is structured as follows. Firstly, the topology is introduced and the neutral-voltage lift concept is described. Then the modeling technique and the modulation strategy are discussed, followed by the simulation and measurement results. Lastly, the conclusions are presented.

II. INTRODUCING THE QAB TOPOLOGY

The proposed QAB-topology is shown in Fig. 1. The full bridges on the mains side are connected to the primary side of transformers T_R , T_S and T_T (see Fig. 1). The secondary terminals of the transformers are series-connected. The voltages are therefore summed on the secondary side. An inductor, L_σ , is used to determine the maximum power flow and the amount of circulating current, similar to the situation in a DAB topology [9]–[17]. In this analysis, the transformers are assumed to have 1:1 winding ratio. As can be seen, a capacitor C_{NVL} is added to the neutral line. The function of this capacitor is to create an offset in the neutral, hence the name: neutral-voltage lift capacitor.

Due to the fact that in a balanced three-phase system $\langle i_{CM}(t) \rangle = 0$, the current through capacitor C_{NVL} is zero as well, and its voltage remains constant. This voltage, $v_{\text{NVL}}(t)$, can therefore be controlled by the common-mode current through all three phases, defined by

$$i_{CM}(t) = -i_{C,\text{NVL}}(t) = i_R(t) + i_S(t) + i_T(t).$$

By ensuring that $v_{\text{NVL}}(t) > -\min(v_{nN}(t))$ with $n \in [R, S, T]$ always holds, the voltages across all switching legs are positive, as shown in Fig. 2. That is to say

Fig. 1. Proposed QAB-converter: a single-stage bi-directional ac-dc converter topology with galvanic isolation.
Note: for simplicity, switching frequency decoupling and filtering are not drawn.

Fig. 2. Waveforms showing the principle of neutral-voltage lift. The voltage off-set results in purely positive voltages over the full bridges.

$$v_n(t) = v_{nN}(t) + v_{NVL}(t) = \sqrt{2}V_{nN} \cos(\omega_{\text{mains}}t + \theta_n) + v_{NVL}(t),$$

where ω_{mains} is the mains grid frequency. The voltage off-set $v_{NVL}(t)$ allows the direct connection between the half-bridge modules and the mains. Due to this superposition, the average voltage stress of all ac-side switches equals V_{NVL} . On the other hand, in a two stage topology such as a six-switch rectifier followed by a dc-dc converter [5], [18] the average voltage stress of the semiconductor exposed to the dc-link is twice as high. This means that in the proposed QAB-converter the single-event burnout (SEB) sensitivity is reduced and thereby lifetime is increased [19]–[22]. Moreover, when compared to converters using bidirectional switches, such as [1], the number of semiconductor is reduced by a factor two, reducing the conduction losses and converter cost. It must also be noted that, when one of the semiconductor switches in a certain AB fails, the remaining ABs can continue to operate normally.

The proposed control block diagram for this converter is shown in Fig. 3. The ac current references are generated locally using a PLL, which ensures grid synchronization and unity power factor operation. The amplitude of these currents,

and thereby the output power, is determined by $i_{\text{mains,ref}}$. To stabilize the neutral-lift capacitor voltage, a common-mode current $i_{\text{CM,ref}}$ is subtracted from the mains phase current references by compensator Γ_{NVL} . The resulting references are fed to the current controller, which consists of a unity feed-forward and a feedback compensator Γ_i . The output of the current controller is fed to the system decoupler, which decouples control parameters using the converter model and linearizes the system response. The output of the system decoupler is fed to the PWM generator, which delivers the gate signals. The contents of the various blocks are described in the following sections.

A. Neutral-voltage lift

To implement NVL, some points require attention, which are the power-up sequence and in-rush current limiting of the converter, as well as the control of v_{NVL} . When the converter is powered on, a pre-charge period is required in order to charge the capacitor C_{NVL} and to prevent high in-rush currents. The pre-charging is achieved by temporarily placing a (PTC) resistor in series with the mains connections, as shown in Fig. 4. As can be seen, the capacitor is then charged via the semiconductor body diodes and these resistors. After the capacitor voltage has reached a sufficiently high value, the pre-charge resistors are bypassed by switches that are connected in parallel to these resistors. Then, the NVL voltage control loop is activated in order to further charge the capacitor to its desired value. This process is shown in Fig. 5. Here, t_1 indicates the moment where the converter is connected to the mains grid, t_2 indicates the moment where the voltage approaches the mains peak voltage $\hat{v}_{nN}$, and the bypass relays are closed. Then, the control loops are activated to further charge the capacitor towards the desired voltage $v_{NVL,\text{ref}}$. Finally, t_3 indicates the moment where the converter starts operating normally. From this point onwards, the common-

Fig. 3. Proposed control layout, consisting of a PLL, a current controller Γ_i , a system decoupler, a common-mode current controller Γ_{NVL} , and a pulse-width modulator.

Fig. 4. Pre-charging of NVL capacitor via resistors. The red line indicates one of the possible current paths. When pre-charging has completed, the switches are closed to bypass the resistors.

Fig. 5. Waveforms while pre-charging the NVL capacitor.

mode current becomes negligible because the capacitor voltage is not changing anymore, hence

$$i_{CM}(t) = i_{NVL}(t) = C_{NVL} \frac{dV_{NVL}(t)}{dt} = 0. \quad (1)$$

The value of the capacitor C_{NVL} is dependent on two things. Firstly, it must be selected such that the control loop is able

to stabilize its voltage and can provide sufficient disturbance rejection. Secondly, the magnitude of the disturbances, that are present in the capacitor current, are dependent on the disturbance rejection of the converter phase current controllers. An estimation of the capacitor value can be done as follows. By knowing the disturbance rejection $S_i(s)$ of the converter current control loop at the mains frequency ω_{mains} , and the RMS phase current I_n , an estimation of the disturbance current $I_{CM,d}$ can be made by

$$I_{CM,d} = 3I_n S_i(j\omega_{mains}). \quad (2)$$

Then, by defining a desired voltage swing on the capacitor $V_{NVL,d}$ and a given disturbance rejection $S_{NVL}(s)$ of the capacitor voltage control loop, the capacitor value can be found by

$$C_{NVL} = \frac{I_{CM,d} S_{NVL}(j\omega_{mains})}{\omega_{mains} V_{NVL,d}}. \quad (3)$$

For instance, with $S_i(j\omega_{mains}) = -30$ dB disturbance rejection of $I_n = 30$ A RMS at 50 Hz mains frequency, an allowed voltage swing of $V_{NVL,d} = 10$ V RMS, and $S_{NVL}(j\omega_{mains}) = -20$ dB disturbance rejection of the capacitor voltage control loop, the capacitor value must be approximately

$$C_{NVL} \approx 88 \mu\text{F}. \quad (4)$$

III. CONVERTER FOURIER-SERIES MODEL

This section introduces a modeling method for the QAB converter. For this purpose, a voltage source model is derived as follows. The ABs are all reflected to the primary side, and the secondary sides of all transformers are connected in series. The resulting schematic is shown in III. It must be noted that reflecting a source from the secondary side to the primary side equals reversing its polarity. In the following, the parameter i indicates the number of ABs, dictated by the QAB-converter topology to be equal to $i = 4$. The parameters n and m refer to an arbitrary AB in the topology, therefore $n, m \in [R, S, T, dc]$.

In this model, each AB generates a voltage u_n across a transformer T_n . The transformer primary side voltage equals the

Fig. 6. Schematic diagram of QAB topology where full bridges and transformers are replaced by voltage sources and are all reflected to the primary side.

secondary side voltage because all transformers are assumed to be ideal, which means there is no magnetizing inductance and no leakage inductance, and the winding ratio is 1:1. A separate inductor L_σ is added that represents the combined leakage inductance of all transformers as follows

$$L_\sigma = \sum_{n=1}^i L_{\sigma, T_n}. \quad (5)$$

The AB corresponding to each transformer T_n is labeled n . Finally, all transformer voltages u_n can be represented by voltage waveforms produced by voltage sources, as shown in III.

The block-shaped waveforms u_n produced by the ABs have an amplitude, a duty cycle, a period time and a phase shift, as shown in Fig. 7(a). There, the gate signals of switches S_{nx} are indicated by black bars. As suggested in the figure, it holds that

$$u_n(t) = u_{n1}(t) - u_{n2}(t), \quad (6)$$

where $u_n(t)$ is the voltage across the transformer T_n secondary side, and v_n the supply of the AB n and thereby defines the amplitude of the voltage over the transformer $u_n(t)$. The waveforms are transformed to Fourier-series, which are subsequently used to derive the current through the inductor L_σ in the circuit. Finally, the output powers of each AB can be found by using the Fourier-series of the current and voltages, resulting in an analytical converter model.

It is assumed that the switching frequency of the ABs, ω_{sw} , is much higher than the frequencies present in the supply voltage of the AB, $v_n(t)$, such that may be assumed that

$$v_n(t) = v_n(t + T_{sw}) \quad (7)$$

with $T_{sw} = \frac{2\pi}{\omega_{sw}}$. Variables that use the above assumption are indicated by the $'$ -symbol.

In view of the quantities in Fig. 7(a), the following arrays of variables are defined:

$$\mathbf{u}'(t) = \begin{pmatrix} u'_R(t) \\ u'_S(t) \\ u'_T(t) \\ u'_{dc}(t) \end{pmatrix}, \quad \mathbf{v}' = \begin{pmatrix} v'_R \\ v'_S \\ v'_T \\ v'_{dc} \end{pmatrix}, \quad \mathbf{d} = \begin{pmatrix} d_R \\ d_S \\ d_T \\ d_{dc} \end{pmatrix}, \quad \mathbf{\Phi} = \begin{pmatrix} \phi_R \\ \phi_S \\ \phi_T \\ \phi_{dc} \end{pmatrix} \quad (8)$$

where $\mathbf{u}'(t)$ contains the set of block-shaped voltages $u'_n(t)$ at the secondary side of the high-frequency transformers.

Fig. 7. Model of a single AB used for Fourier-analysis. (a) Switched-node voltages and gate drive signals for transformer voltage u'_n , (b) corresponding AB schematic diagram.

The set of active-bridge bus voltages is combined in $\mathbf{v}'$. The set of phase-shifts between the full-bridge switching legs is represented by $\mathbf{\Phi}$, and $\mathbf{d}$ is the set of duty-cycles for $u'_n(t)$.

Then, the function $\mathbf{u}'(t)$ can be written in the orthogonal Fourier-series representation

$$\mathbf{u}'(t) = \sum_{k=1}^{\infty} \mathbf{Ua}'(k) \cos((2k-1)\omega_{sw}t) + \mathbf{Ub}'(k) \sin((2k-1)\omega_{sw}t) \quad (9)$$

with

$$\mathbf{Ua}'(k) = \mathbf{U}'(k) \begin{pmatrix} \sin((2k-1)(\mathbf{\Phi} + 0.5\pi\mathbf{d})) \\ -\sin((2k-1)(\mathbf{\Phi} - 0.5\pi\mathbf{d})) \end{pmatrix}, \quad (10)$$

$$\mathbf{Ub}'(k) = \mathbf{U}'(k) \begin{pmatrix} \cos((2k-1)(\mathbf{\Phi} + 0.5\pi\mathbf{d})) \\ -\cos((2k-1)(\mathbf{\Phi} - 0.5\pi\mathbf{d})) \end{pmatrix} \quad (11)$$

and $\mathbf{U}'(k) = \frac{2\mathbf{v}'}{\pi(2k-1)}$. The current contribution through L_σ of source voltage $v'_n(t)$ is equal to the integral of the sum of the inductor voltage divided by the reactance of the inductor, being

$$\mathbf{i}'_\sigma(t) = \frac{\int \mathbf{u}'(t) dt}{L_\sigma} = \frac{\sum_{k=1}^{\infty} -\mathbf{Ub}'(k) \cos((2k-1)\omega_{sw}t)}{(2k-1)\omega_{sw}L_\sigma}$$

$$+ \frac{\sum_{k=1}^{\infty} \mathbf{Ua}'(k) \sin((2k-1)\omega_{sw}t)}{(2k-1)\omega_{sw}L_{\sigma}} \quad (12)$$

Hence, the total inductor current is equal to the superposition of all currents, and therefore found to be

$$i'_{\sigma}(t) = \sum_{k=1}^{\infty} I'_{\sigma a}(k) \cos((2k-1)\omega_{sw}t) + I'_{\sigma b}(k) \sin((2k-1)\omega_{sw}t) \quad (13)$$

with the Fourier-coefficients

$$I'_{\sigma a}(k) = \frac{-\sum_{n=1}^i \mathbf{Ub}'_n(k)}{(2k-1)\omega_{sw}L_{\sigma}}, \quad I'_{\sigma b}(k) = \frac{\sum_{n=1}^i \mathbf{Ua}'_n(k)}{(2k-1)\omega_{sw}L_{\sigma}}. \quad (14)$$

To obtain a relatively simple expression that can be used for optimization purposes, only the first harmonic is used ($k_{\max} = 1$). By doing this, the coefficients become

$$\mathbf{Ua}'(1) = \mathbf{U}'(\sin(\Phi + 0.5\mathbf{d}\pi) - \sin(\Phi - 0.5\mathbf{d}\pi)) \\ = 2\mathbf{U}' \cos(\Phi) \sin(0.5\mathbf{d}\pi) \quad (15)$$

$$\mathbf{Ub}'(1) = \mathbf{U}'(\cos(\Phi + 0.5\mathbf{d}\pi) - \cos(\Phi - 0.5\mathbf{d}\pi)) \\ = -2\mathbf{U}' \sin(\Phi) \sin(0.5\mathbf{d}\pi). \quad (16)$$

with $\mathbf{U}' = 2\mathbf{v}'/\pi$. This is an approximation, similarly to [11], [12]. Now, by defining

$$\mathbf{X} = \sin(0.5\pi\mathbf{d}) \quad (17)$$

the power of source n when using only the first harmonic is found by

$$P'_n = 0.5I'_{\sigma a}(1) \mathbf{Ua}'_n(1) + 0.5I'_{\sigma b}(1) \mathbf{Ub}'_n(1) \\ = \frac{8}{\omega_{sw}L_{\sigma}\pi^2} v'_n X_n (v'_1 X_1 \sin(\phi_1 - \phi_n) + \dots + v'_i X_i \sin(\phi_i - \phi_n)) \quad (18)$$

and the current through L_{σ} is found by

$$I'_{\sigma} = \sqrt{0.5 \left(\sum_{n=1}^i \frac{4v'_n X_n}{\pi\omega_{sw}L_{\sigma}} \sin(\phi_n) \right)^2 + 0.5 \left(\sum_{n=1}^i \frac{4v'_n X_n}{\pi\omega_{sw}L_{\sigma}} \cos(\phi_n) \right)^2}. \quad (19)$$

The AB input current can be found by

$$i'_n = \frac{P'_n}{v'_n}. \quad (20)$$

Using the method as presented in [23], the soft-switching boundaries can be determined as well. This is not covered in this paper.

IV. POWER-BALANCE CONTROL

The power-balance control (PBC) method is proposed for the QAB-converter. The PBC uses Newton-optimization in order to minimize the circulating current. Moreover, it is possible to scale the circulating current independent from the AB output currents to actively control the thermal stress of active and passive components.

When assuming ideal efficiency, the sum of the powers of ABs delivering power (P'_{pos}) is equal to the sum of the powers of ABs receiving power (P'_{neg}), as described by

$$P'_{\text{pos,set}} = \sum_{n=1}^i \{P'_{n,\text{set}} : P'_{n,\text{set}} \geq 0\} \quad (21)$$

$$P'_{\text{neg,set}} = \sum_{n=1}^i \{P'_{n,\text{set}} : P'_{n,\text{set}} < 0\} \quad (22)$$

$$P'_{\text{pos,set}} = P'_{\text{neg,set}}. \quad (23)$$

This is similar to an $i = 2$ situation where all positive power is processed by only one source $U'_{\text{pos}} = v'_{\text{pos}} X_{\text{pos}}$, as well as the negative power is processed by another source $U'_{\text{neg}} = v'_{\text{neg}} X_{\text{neg}}$. The following therefore assumes a two-sources problem. Further on, the model is extended to distribute the power across all ABs of the QAB-converter.

The RMS value of the current through the leakage inductance L_{σ} determines the resistive losses in the converter. To minimize the RMS current through the inductor, the following optimization problem should be solved:

$$\text{minimize } I'_{\sigma} \quad (24)$$

$$\text{with } \begin{pmatrix} P'_{\text{pos}} \\ P'_{\text{neg}} \end{pmatrix} = \begin{pmatrix} P'_{\text{pos,set}} \\ P'_{\text{neg,set}} \end{pmatrix}, \quad (25)$$

with P'_n the active power of AB n , resulting from the first-harmonic approximation ($k_{\max} = 1$) given by (18). $P'_{n,\text{set}}$ is the set-point of the active power of AB n . Here, the optimization algorithm selects the duty cycles d_n and phase shifts ϕ_n to have the desired output power with the minimum amount of (RMS) current through the converter.

It is assumed that the first harmonic is dominant in causing circulating currents. The cost function W is simplified by minimizing

$$W = 2 \left(\frac{\pi\omega_{sw}L_{\sigma}I'_{\sigma}}{4} \right)^2, \quad (26)$$

which yields the same Φ and $\mathbf{d}$ because the parameters ω_{sw} and L_{σ} are both kept constant in the optimization procedure. By substitution of (19) into (26), the cost function W is found to be

$$W = \left(\sum_{n=1}^i v'_n X_n \sin(\phi_n) \right)^2 + \left(\sum_{n=1}^i v'_n X_n \cos(\phi_n) \right)^2. \quad (27)$$

While the minimization of W results in the lowest circulating currents, it does not guarantee the output power equals the power set-point. This is, however, a constraint which needs to be met. Therefore

$$\sum_{n=1}^i (P'_n - P'_{n,\text{set}})^2 = 0, \quad (28)$$

to ensure all outputs have the desired power. (28) is valid when $|\phi_m - \phi_n| \ll \pi/2$, such that $\sin(\phi_m - \phi_n) \approx \phi_m - \phi_n \forall n, m$ where $\{n, m \in \mathbb{N} | n \leq i, m \leq i\}$ holds, as this linearisation is used to calculate the phase shifts. It can be shown that a strong

approximation of the criterion in (28) can be accomplished when

$$(\phi_{\text{pos}} - \phi_{\text{neg}})^2 = \alpha^2, \quad (29)$$

where α is a parameter introduced to fix the maximum cross-difference between the phase shifts, to provide a trade-off between model accuracy (linearisation error) and the amount of circulating current. The parameter should be in the linear range of the model, bounded to $0 < \alpha < \frac{\pi}{2}$. Note that, when (29) is met, the desired output powers are guaranteed to be within the linearisation errors, and the error becomes smaller when α is smaller.

Using the method of Lagrange multipliers [24], the constraint (29) is taken into account together with the cost function (27) as follows:

$$\text{minimize } H = W + \lambda \left((\phi_{\text{pos}} - \phi_{\text{neg}})^2 - \alpha^2 \right). \quad (30)$$

Now, the optimum is found when for each parameter (X_n , ϕ_n) the derivatives of H are equal to zero.

First, the cost function (27) can be simplified by using the approximation

$$W = \left(\sum_{n=1}^i v'_n X_n \sin(\phi_n) \right)^2 + \left(\sum_{n=1}^i v'_n X_n \cos(\phi_n) \right)^2 \quad (31)$$

$$= (v'_1 X_1)^2 + (v'_2 X_2)^2 + 2(v'_1 X_1)(v'_2 X_2) \cos(\phi_1 - \phi_2) \quad (32)$$

$$\approx U'^2_{\text{pos}} + U'^2_{\text{neg}}, \quad (33)$$

which is valid because $\cos(\phi_{\text{pos}} - \phi_{\text{neg}}) \rightarrow 0$ as the phase shift is selected to be large to optimize efficiency, as described in the next paragraph.

Newton's method is used to find the optimum for $i = 2$, where each term of the Jacobian of H is set to zero. The solution is obtained from

$$\text{minimize } H = (U'_{\text{pos}})^2 + (U'_{\text{neg}})^2 + \lambda \left((\phi_1 - \phi_2)^2 - \alpha^2 \right) \quad (34)$$

After substitution of ϕ_n from (18) (similar to phase-shift control from [12]) and assuming $\phi_1 = 0$ yields the following optimization assignment:

$$\begin{aligned} \text{minimize } H &= (U'_{\text{pos}})^2 + (U'_{\text{neg}})^2 \\ &+ \lambda \left(\arcsin \left(\left(\frac{\omega_{sw} L_{\sigma} \pi^2}{8(U'_{\text{pos}} + U'_{\text{neg}})} \right) \left(\frac{P'_{\text{pos}}}{U'_{\text{pos}}} - \frac{P'_{\text{neg}}}{U'_{\text{neg}}} \right) \right)^2 - \alpha^2 \right). \end{aligned} \quad (35)$$

By power conservation it holds that $P_2 = -P_1$, such that this equation can be rewritten into

$$\begin{aligned} \text{minimize } H &= (U'_{\text{pos}})^2 + (U'_{\text{neg}})^2 \\ &+ \lambda \left(\arcsin \left(\left(\frac{\omega_{sw} L_{\sigma} \pi^2}{8(U'_{\text{pos}} + U'_{\text{neg}})} \right) \left(\frac{P'_{\text{pos}}}{U'_{\text{pos}}} + \frac{P'_{\text{pos}}}{U'_{\text{neg}}} \right) \right)^2 - \alpha^2 \right). \end{aligned} \quad (36)$$

This optimization is carried out by equating the Jacobian of H to zero, which is equal to

$$\mathbf{J} = \begin{pmatrix} 2U'_{\text{pos}} - \frac{2\lambda\sigma P'_{\text{pos}} \arcsin(\sigma P'_{\text{pos}}/U'_{\text{pos}}U'_{\text{neg}})}{U'^2_{\text{pos}}U'_{\text{neg}} \sqrt{1-(\sigma^2 P'^2_{\text{pos}}/U'^2_{\text{pos}}U'^2_{\text{neg}})}} \\ 2U'_{\text{neg}} - \frac{2\lambda\sigma P'_{\text{pos}} \arcsin(\sigma P'_{\text{pos}}/U'_{\text{pos}}U'_{\text{neg}})}{U'_{\text{pos}}U'^2_{\text{neg}} \sqrt{1-(\sigma^2 P'^2_{\text{pos}}/U'^2_{\text{pos}}U'^2_{\text{neg}})}} \\ \arcsin^2 \left(\frac{\sigma P'_{\text{pos}}}{U'_{\text{pos}}U'_{\text{neg}}} \right) - \alpha^2 \end{pmatrix} \quad (37)$$

with

$$\mathbf{J} = \begin{pmatrix} \frac{\partial H}{\partial(U'_{\text{pos}})} \\ \frac{\partial H}{\partial(U'_{\text{neg}})} \\ \frac{\partial H}{\partial \lambda} \end{pmatrix}, \quad \sigma = \frac{\omega_{sw} L_{\sigma} \pi^2}{8}. \quad (38)$$

Solving $\mathbf{J} = \mathbf{0}$ for U'_{pos} and U'_{neg} with $\alpha = \pi/2$ results in

$$U'_{\text{pos}} = v'_{\text{pos}} X_{\text{pos}} = \frac{\pi \sqrt{P'_{\text{pos, set}} \omega_{sw} L_{\sigma}}}{2\sqrt{2}} \quad (39)$$

$$U'_{\text{neg}} = v'_{\text{neg}} X_{\text{neg}} = \frac{\pi \sqrt{P'_{\text{neg, set}} \omega_{sw} L_{\sigma}}}{2\sqrt{2}} \quad (40)$$

with $P'_{\text{pos, set}}$ the sum of the power set-points of all positive sources, and $v'_{\text{pos}} X_{\text{pos}}$ the sum of all phasor lengths of all positive sources. Furthermore, because it holds that $P'_{\text{pos, set}} = P'_{\text{neg, set}}$, the phasor lengths are equal, being

$$U'_{\text{neg}} = U'_{\text{pos}}. \quad (41)$$

with $\alpha = \pi/2$. Then, calculating the elements of $\mathbf{d}$ and $\mathbf{\phi}$ using (17) and (18) and substitution with $\alpha = \pi/2$, assuming $P'_{\text{pos}} = -P'_{\text{neg}} \geq 0$ yields, with some manipulations,

$$\begin{aligned} \phi_{\text{pos}} &= -0.5\alpha = -\pi/4 \\ \phi_{\text{neg}} &= 0.5\alpha = \pi/4, \end{aligned} \quad (42)$$

which meets the constraint $(\phi_{\text{pos}} - \phi_{\text{neg}})^2 = \alpha^2$. It must be noted that $U'_{\text{pos}} = U'_{\text{neg}}$ because the corresponding powers are equal, and so from (39) the maximum output power is achieved when $\max(X_{\text{pos}}, X_{\text{neg}}) = 1$.

The two-AB solution is based on a linearized model which is valid as long as $\sin(\phi_{\text{pos}} - \phi_{\text{neg}}) \approx \phi_{\text{pos}} - \phi_{\text{neg}}$. This solution can be improved significantly when a description is used which has a broader validity range, as shown in this section. Also, the model is adapted such that it can be applied to the QAB-converter. Furthermore, control over I'_{σ} is implemented, which allows to manipulate the losses without changing the output powers of the ABs.

As shown graphically in Fig. 8, for a given $P'_{\text{pos, set}}$, the following parameters can be defined:

$$\begin{aligned} a &= U'_{\text{pos}} \sin\left(\frac{\alpha}{2}\right) & a^{\circ} &= U'_{\text{pos}} \sin\left(\frac{\alpha^{\circ}}{2}\right) \\ b &= U'_{\text{pos}} \cos\left(\frac{\alpha}{2}\right) & b^{\circ} &= U'_{\text{pos}} \cos\left(\frac{\alpha^{\circ}}{2}\right) \end{aligned} \quad (43)$$

By empirical evaluation of the circulating current in a large range of scenarios, it is found that $\beta_{\max, \text{limit}} = 2.7$ will typically result in minimum circulating current over the full load range. Therefore, this value is used in the evaluation in this paper.

V. COMPONENT DIMENSIONING

Designing the QAB-converter involves selecting the ratings and values of its components. The most important parameters to assist the selection procedure for the main circuit components are given in the following.

The voltage v_{NVL} can be said to equal

$$v_{\text{NVL}} = 1.15 \hat{v}_{nN}, \quad (63)$$

such that sufficient voltage margin is present even when small disturbances occur in the mains grid. Moreover, the value of the capacitor C_{NVL} is found using (3).

The value of the inductance L_{σ} is determined by (39) such that

$$L_{\sigma} < \frac{8(\hat{v}'_n + v'_{\text{NVL}})}{\pi^2 \omega_{\text{sw}} \hat{i}_{\text{mains}}}. \quad (64)$$

This value is the upper limit, and it should be taken into account that the first-harmonic approximation has inaccuracies, and that a safety margin must be taken into account if the converter will be operated at the currents that are used in the above calculation. Generally, it will be sufficient to take 25% power reserve into account to compensate these two issues, which means that L_{σ} must be reduced by the same amount.

The peak current of this inductor can then be estimated by using (19). The maximum current is reached for a phase shift of $\pi/2$. Then, by using (39) the inductor voltage is found to be

$$V'_{\sigma} = \frac{2}{\sqrt{2}} U'_{\text{pos}} = \frac{\pi}{2} \sqrt{P'_{\text{pos, set}} \omega_{\text{sw}} L_{\sigma}}, \quad (65)$$

with

$$P'_{\text{pos, set}} = (v'_{\text{NVL}} + \hat{v}_{nN}) \hat{i}_{\text{mains}}, \quad (66)$$

given that $n \in [R, S, T]$, resulting in

$$\hat{i}'_{\sigma} = \frac{\pi \sqrt{(v'_{\text{NVL}} + \hat{v}_{nN}) \hat{i}_{\text{mains}}}}{2 \sqrt{\omega_{\text{sw}} L_{\sigma}}}. \quad (67)$$

Moreover, the RMS current is equal to

$$I_n = \frac{\hat{i}'_{\sigma}}{\sqrt{2}}. \quad (68)$$

The current i_{σ} flows through all semiconductors and magnetic components, due to the fact that all these components are connected in series. This current therefore also defines the current rating of these parts.

The peak voltages of the semiconductors on the mains side and dc side are equal to

$$\hat{v}_n = \begin{cases} v_{\text{NVL}} + \hat{v}_{nN} & \text{for } n \in [R, S, T] \\ v_{dc} & \text{for } n \in [dc]. \end{cases} \quad (69)$$

The average semiconductor voltage, on the other hand, is defined by

$$\langle v_n \rangle = \begin{cases} \langle v_{\text{NVL}}(t) \rangle & \text{for } n \in [R, S, T] \\ v_{dc} & \text{for } n \in [dc]. \end{cases} \quad (70)$$

The switching frequency ω_{sw} must be established to the find results of the above equations. Because many a thing determine its optimal value, one can do an optimization which uses, for instance, the resulting converter losses and cost. This optimization procedure is, however, not described in this paper.

The analysis that is carried out assumes that the transformers are ideal and have a 1:1 winding ratio. This means, however, that the output voltage must be in a certain range for the converter to perform properly. If a higher or lower output voltage is desired, the winding ratios of the transformers should be changed. To add the transformer winding ratio, n_{ratio} , the values for analysis are found according to

$$u'_{dc} = \frac{u'_{dc,s}}{n_{\text{ratio}}}, \quad v'_{dc} = \frac{v'_{dc,s}}{n_{\text{ratio}}}, \quad i_{dc} = n_{\text{ratio}} i_{dc,s}, \quad i_{\sigma,s} = \frac{i_{\sigma}}{n_{\text{ratio}}}, \quad L_{\sigma,s} = n_{\text{ratio}}^2 L_{\sigma}, \quad (71)$$

where $u'_{dc,s}$, $v'_{dc,s}$, $i_{dc,s}$, and $L_{\sigma,s}$ are the secondary-side values. The transformer winding ratio can be used to minimize circulating currents in a three-phase application. To achieve maximum utilization of the available voltage, hence minimize the current required to transfer a certain power, unity duty cycle must be obtained, and it follows from (45) that therefore

$$X_{dc} = 1 = \frac{U_{\text{pos}} P_{dc}}{P_{\text{pos}} v'_{dc}} \quad (72)$$

where

$$U_{\text{pos}} = \frac{\pi \sqrt{P'_{\text{pos, set}} \omega_{\text{sw}} L_{\sigma}}}{2 \sqrt{2}} \quad (73)$$

which, in the case that one of the three mains phase voltages are maximum and by using (64), equals

$$U_{\text{pos}} = \frac{\pi \sqrt{(\hat{v}_{nN} + v_{\text{NVL}}) \hat{i}_{\text{mains}} \omega_{\text{sw}} \frac{8(\hat{v}'_n + v'_{\text{NVL}})}{\pi^2 \omega_{\text{sw}} \hat{i}_{\text{mains}}}}}{2 \sqrt{2}} \quad (74)$$

$$= \hat{v}_{nN} + v_{\text{NVL}} \quad (75)$$

such that, when using power conservation according to

$$P_{dc} = \frac{3 \hat{v}_{nN} \hat{i}_{\text{mains}}}{2}, \quad (76)$$

it follows that

$$\frac{3 \hat{v}_{nN} \hat{i}_{\text{mains}}}{2 \hat{i}_{\text{mains}} v'_{dc}} = \frac{3 \hat{v}_{nN} n_{\text{ratio}}}{2 v'_{dc,s}} = 1 \quad (77)$$

$$n_{\text{ratio}} = \frac{2 v'_{dc,s}}{3 \hat{v}_{nN}}. \quad (78)$$

This ratio is the number of turns on the secondary side divided by the number of turns on the primary side of each transformer.

Remark that, in practical applications, and in the analysis that is used, the inductor L_{σ} is located on the secondary side. Hence, when $n_{\text{ratio}} \neq 1$, $L_{\sigma,s}$ must be used. Moreover, in

TABLE I
SIMULATION AND MEASUREMENT PARAMETERS

Parameter	Value	Unit
ω_{sw}	$2\pi \cdot 45$	krad/s
V_{nN}	230	V ac RMS
V_{dc}	500	V
C_{NVL}	220	μF
C_{NVL} voltage	375	V
L_{σ}	28	μH
γ	1

Fig. 9. Block diagram showing the setup used for the measurements.

this case $i_{\sigma,s}$ defines the current through the secondary-side transformer windings, inductors and switches.

Transformers have a magnetizing inductance L_{mag} , which causes reactive current to flow through the ABs. In some situations, this current can help to increase the range in which ZVS operation is achieved. This aspect, however, is not included in this analysis.

To comply with EMC regulations and standards, common-mode and differential-mode filters should be added. These filters must be designed such that the discontinuous input currents of the ABs are filtered sufficiently. To analyze the input current waveforms and frequency content, the provided modeling technique can be used. The filter design procedure itself is not included in this paper.

VI. RESULTS

Measurement and simulation parameters are specified in Table I. Simulations have been carried out using MATLAB and the Plexim PLECS toolbox to verify the converter operation and the proposed control method. Moreover, to verify the converter operation, measurements were carried out on a 20 kW QAB-converter prototype with SiC MOSFET modules.

For the measurements, a setup is used which consists of a power analyzer, two sources, and a controlling computer, as shown in Fig. 9. The dc-side power source comprises a load resistor and a dc power supply, such that both current sourcing and current sinking on the dc-side is possible. The ac-side power source consists of three four-quadrant power amplifiers which are combined to form a three-phase ac source. Amidst the sources and the QAB-converter prototype is a power

TABLE II
OVERVIEW OF EQUIPMENT USED FOR THE MEASUREMENTS.

Equipment	Type
Power analyzer	Yokogawa WT3000E (4x 1kV 30A elements)
AC source	Spitzenberger & Spies DM 15000 / PAS
DC source	Combined dc power supply and load resistor
- DC power supply	Regatron TopCon TC.P.20.1000.400.S.HMI
- Load resistor	Frizlen BWV 83
Oscilloscope	LeCroy WaveRunner 44MXi-A
- High-voltage probes	Tektronix P5200A
- Current probe	Tektronix TCP303

Fig. 10. Overview photo of prototype QAB-converter in laboratory set-up.

analyzer to measure the performance of the converter. Table II shows a summary of all equipment that is used. A photo of the setup is shown in Fig. 10.

Firstly, the initialization of the neutral-voltage lift is verified and shown in Fig. 11. As can be seen, it pre-charges via the body diodes and series resistors. Then, when the gate drivers and the control loop are initialized, the voltage is lifted further, up to the working voltage. This procedure is according to Fig. 5.

Next, waveforms of the ac- and dc-side were measured at 10 kW in rectifier mode. These are shown in Fig. 12. Some distortions are present near the peaks of the current. These irregularities worsen significantly if the dead time is increased from 400 ns to 800 ns.

A load step is measured from -5 kW to +5 kW, which is

Fig. 11. Measurement of neutral-voltage lift (blue, 50 V/div) and common-mode current (yellow, 1 A/div) during the initialization phase of the converter.

Fig. 12. Measurement with 10 kW input power and rectifier operation, showing the converter ac-side voltages and currents (top, 150 V/div, 10 A/div), and dc-side voltage and current (bottom, 300 V/div, 10 A/div).

Fig. 13. Measurement with input power load step from 5 kW rectifier mode to 5 kW inverter mode, showing the converter ac-side voltages and currents (top, 150 V/div, 5 A/div), and dc-side voltage and current (bottom, 300 V/div, 5 A/div).

shown in Fig. 13. The behavior is as expected.

Then, at over 14 kW, which is the maximum output power of the ac-source, detailed information of the input and output is given in Table III. As can be seen, the power factor is high, and the current waveforms have a relatively low total harmonic distortion.

The power factor has been measured in both inverter and rectifier mode, which is shown in Fig. 14. It is demonstrated that its value is higher than 0.98 from 10% output power onwards.

Then, the parameter γ was varied while measuring the RMS current i_{σ} , as shown in Fig. 15. This is done for a range of input powers and compared with simulation results. As

TABLE III
MEASUREMENT DATA OBTAINED AT 14 kW INPUT POWER, OPERATING AS RECTIFIER.

Parameter	Value
Mains voltage	229.5 V RMS
Mains current	20.65 A RMS
Mains power	14.17 kW
Mains power factor	0.9967
Mains current THD	4.5%
DC voltage	501.5 V
DC current	26.21 A
DC power	13.14 kW

Fig. 14. Power factor of QAB-converter prototype operating as rectifier (black) and inverter (grey dashed).

can be seen, the current can be varied while maintaining the same output power. The significant difference that appears to be present between simulation and measurements results for lower values of γ might be caused by resistive losses, semiconductor dead time effects, or errors in matching the actual magnetics with the models, for instance. For γ close to 1 the predictions are correct, and the trend of the response is correct as well. The mismatch does not cause any other unexpected behavior, and it is therefore anticipated that it does not preclude thermal stress control to be used effectively.

Finally, some measurements are taken to show the transformer voltages u_n with $n \in [R, S, T, dc]$ in both the rectifier mode and the inverter mode, as shown in Fig. 16 and Fig. 17 respectively. Here, it can be clearly seen that each transformer is modulated according to its own setpoint, and that the reactive currents are low, as governed by the PBC method. Moreover, it can be seen that almost no ringing and other parasitic effects are present.

Fig. 15. Measured effect of parameter γ on RMS current of i_{σ} averaged over a full ac mains cycle at various input powers and compared with simulations, with $\gamma \in [1, 0.9, 0.8, 0.7]$ (bottom to top).

Fig. 16. Measured switched-nodes voltages u_n and current i_σ at 10 kW input power in rectifier mode. Top: u_{dc} (yellow), u_R (magenta), u_S (blue), u_T (green), all 200 V/div. Bottom: i_σ , 20 A/div.

Fig. 17. Measured switched-nodes voltages u_n and current i_σ at 10 kW input power in inverter mode. Top: u_{dc} (yellow), u_R (magenta), u_S (blue), u_T (green), all 200 V/div. Bottom: i_σ , 20 A/div.

VII. CONCLUSION

In this paper a fundamentally new method for ac-dc conversion has been analyzed and a modulation strategy is proposed. The method comprises two essential parts, namely a neutral-voltage lift capacitor (C_{NVL}) and a Quad Active Bridge (QAB) topology. Galvanic isolation is provided, making the converter suitable for battery chargers, medical equipment, non-interruptible power supplies, lithography machines, and IT equipment, among others. Furthermore, the converter is capable of bi-directional power flow to allow, for example, power supply systems to charge and discharge batteries or recover braking energy of motion systems.

The proposed modulation scheme provides an optimized method to regulate the power flow in the converter, and allows scaling of the circulating current. The latter enables for instance thermal stress reduction. Measurements demonstrate the potential of the QAB-converter and the neutral-voltage lifting principle. Furthermore, it has been shown that the algebraic model of the converter is valid, and that the phase currents are properly regulated in the prototype converter.

The analysis methods, modulation strategy, and component dimensioning guidelines can be used for the design and ana-

lysis of ac-dc power converters based on the QAB-topology. The methods are validated to be accurate, and it is demonstrated that the topology operates as expected. Additionally, the features of this converter make it an attractive alternative to common two-stage topologies.

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