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PROGRAMMABLE LOW NOISE AMPLIFIER WITH
ACTIVE-INDUCTOR LOAD

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ABSTRACT
A common gate CMOS low noise amplifier (LNA) with an active-
inductor load is presented. For large inductance values, an on-
chip passive inductor requires considerable silicon area and it is
quality-factor (Q) limited, a situation that can be rendered as
impractical. Hence, the purpose of this work is to seek the
possibility of using active inductors in RF circuits as substitutes
for passive ones. Moreover, an active inductor opens avenues for
programmability, e.g. it is possible to attain an amplifier with a
programmable center frequency. It is shown in this paper that by
proper design optimization the active-inductor's noise
contribution can be minimized. HSPICE simulations using
0.5~HP technology show that our amplifier has a tuning range of half
decade for a center frequency at 1GHz. The simulated gain, noise
figure, and power consumption are 20dB, 3.65dB, and 14mW,
respectively.

I. INTRODUCTION
Motivated by the growing market of RF communications systems,
much effort has been devoted to the implementation of RF
components in a CMOS technology. The low noise amplifier
(LNA) is the most demanding block in an RF system in terms of
noise-figure and linearity. Inductors are fundamental for the
design of low noise amplifiers. Most of the published LNAs[1,2,3,9]
are implemented by using on-chip spirals. These inductors
consume too much area and are quality factor limited.
Nevertheless, by applying techniques such as the ones proposed in
[4,4], it is possible to compensate the quality factor of these
inductors. Recently, an active inductor[5,6] which can operate close
to the transistors fT was proposed. However, in LNA designs, the
problem associated with active inductors is not primarily the
frequency response but the additional noise introduced by its
active components. In this paper, we carry out a thorough noise
analysis of a common-gate LNA using an active-inductor load.
We demonstrate how through careful design optimization the
LNA's noise figure is minimized and finally we present
simulation results to substantiate our findings.

II. OVERVIEW OF LNA DESIGN
Conventional design objectives for LNAs are to minimize the
amplifier's noise figure, to provide reasonable gain with good
linearity at RF frequency, and to provide good input matching to
the antenna or to the RF filter. LNAs can be classified into
common gate[1] or cascaded common source[2,7] architectures. To
achieve high gain at RF, a large inductor load with high quality
factor is desired. This also helps to reject out-of-band signals and
noise. However, silicon-based on-chip spiral inductors cannot
meet the above requirement due to the associated parasitic
capacitance and resistance losses that arise from the substrate and
metal lines. Large inductance values can only be fabricated by
removing the inductor's underlying silicon substrate. This
introduces additional processing steps and reliability problems.
Furthermore, these on chip inductors occupy a large silicon area
and are not tunable. For instance, the estimated physical size of a
40nH inductor using Greenhouse's formula[8] is more than
0.06mm². The area of such inductor is obviously excessive. Thus,
an active inductor that can be implemented with a reasonable
physical size seems a good alternative for its passive equivalent.

III. DESIGN OF ACTIVE INDUCTOR
An often-used way for making active inductors is through the
combination of a gyrator and a capacitor. Proposed circuits
such as the ones depicted in Fig. 1 exploit the parasitics within
the devices. Those active inductors can operate in the GHz range.

![Diagram of active inductor using gate parasitic capacitor of M2]

(a) cascade  (b) regulated cascode

To reduce the inductor loss in the circuits of Fig. 1 it is necessary
to decrease the output conductance at node V2 either by using
cascoding or regulated cascoding techniques[9]. Simultaneously,
the integration zero is pushed further to a lower frequency,
thereby increasing the frequency range of the inductance. With
these circuits it is easier to implement a large inductance with
less power consumption or less area because of the trade-offs
between g_m and C_{gs}.

Based on a first order small signal analysis the equivalent RLC
network for this inductor is shown in Fig. 2 where,

\[ L = \frac{C_{gs2}}{S_{m1}g_{m2}} \]  

(1)
\[ r_L = \frac{G_{m1}}{S_{m1}S_{m2}} \] (2a)

\( G_{o1} \) is equivalent output conductance at node \( V_2 \) in Fig. 1.

\[ G_{o1} = \frac{E_{ds1}E_{ds3}}{E_{m3}} \] for Fig. 1(a) (2b)

\[ G_{o1} = \frac{E_{ds1}E_{ds3}E_{ds4}}{E_{m3}S_{m4}} \] for Fig. 1(b) (2c)

\[ C = C_{g1} \]

\[ R = \frac{1}{S_{m2}} \] (4)

\[ z = \frac{G_{o1}}{C_{g2}} \] (5)

\[ p = \frac{S_{m2}}{C_{g2}} \] (6)

The self-resonant frequency for the inductor is

\[ \omega_0^2 = \frac{S_{m1}}{C_{g2}} \] (7)

and the \( Q \) at self-resonant frequency \( \omega_0 \) can be written as

\[ Q_L = \frac{\omega_0 C_{g2}}{G_{o1}} = \sqrt{\frac{S_{m1}S_{m2}C_{g2}}{G_{o1}^2 C_{g2}}} \] (8)

\[ r_L = \frac{G_{m1}}{S_{m1}S_{m2}} \]

\( G_{o1} \) is equivalent output conductance at node \( V_2 \) in Fig. 1.

\[ G_{o1} = \frac{E_{ds1}E_{ds3}}{E_{m3}} \] for Fig. 1(a) (2b)

\[ G_{o1} = \frac{E_{ds1}E_{ds3}E_{ds4}}{E_{m3}S_{m4}} \] for Fig. 1(b) (2c)

\[ C = C_{g1} \]

\[ R = \frac{1}{S_{m2}} \] (4)

\[ z = \frac{G_{o1}}{C_{g2}} \] (5)

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\[ Q_L = \frac{\omega_0 C_{g2}}{G_{o1}} = \sqrt{\frac{S_{m1}S_{m2}C_{g2}}{G_{o1}^2 C_{g2}}} \] (8)

**Fig. 2.** Equivalent RLC model of active inductor

The most challenging problem associated with active inductors is their poor noise performance as compared to their passive equivalents. Without loss of generality, the noise of the active inductors shown in Fig. 1 can be calculated as shown in Fig. 3.\(^9\)

\[ dv_{gm1} = 4KT\gamma \cdot df \] (9)

\[ dv_{gm2} = 4KT\gamma S_{m2} \cdot df \] (10)

where \( K \) is the Boltzman constant, \( T \) is the absolute temperature, \( df \) is the noise bandwidth, and \( y \) is the coefficient of the channel’s thermal noise. These noise sources contribute additional noise, which in theory degrades the LNA’s performance. However, in Section IV, it will be shown that through careful design, the effects of these noise sources on the LNA can be minimized as well.

**IV. ACTIVE INDUCTOR LNA DESIGN**

As a vehicle to illustrate the relevance of an active inductor, we chose the common-gate LNA because it requires a large inductor that is often impractical for a passive on-chip implementation. For the analysis consider an LNA with the regulated cascode active-inductor load as depicted in Fig. 4. Inductance \( L_o \), which can be done off-chip,\(^1\) is tuned to be resonant with the input transistor’s \( C_{gs} \). Input impedance matching is done through the input transconductance \( 1/S_{m1} \) which can be adjusted by \( V_g \). \( V_p \) is set to make the current flow through \( M_o \) and \( M_p \) be the same allowing us in this way to have individual control over the active inductor. Namely, it allows us to have a constant \( g_{mn} \) and to adjust \( I_1, I_2 \), and \( I_3 \) separately to control the inductor’s \( L, \omega_o \), and \( Q \) values. The inductance value and center frequency can be set by varying \( I_1 \) and \( I_2 \), while the quality factor can be tuned by varying \( I_3 \), independently. Fig. 5 shows the implementation of current sources \( I_1, I_2 \) and \( I_3 \), where \( I_1 \) and \( I_2 \) are implemented using P-type high swing cascode current mirrors and \( I_3 \) is implemented using N-type equivalents. Requirements for the output impedance of \( I_1 \) and \( I_2 \) are not as demanding as for \( I_3 \) which is best implemented with a regulated cascode current source. Observe that the more complex the current source is, the more poles and zeros it will introduce. This obviously degrades the LNA’s high frequency response. In our case, we use a cascode current mirror for \( I_1, I_2 \) and \( I_3 \).

Neglecting the non-idealities of the current sources, the LNA’s gain can be written as \( g_{mn} \cdot R_{eq} \) where, \( R_{eq} \) is the output impedance of \( M_o \) and \( M_p \) respectively. \( R \) and \( r_L \) are shown in Fig. 2 and \( Q \) is defined as

\[ Q = \frac{1}{\omega R_{eq}} C_{out} = \frac{Q_L}{R_{eq}} \] (11)

A small-signal analysis reveals that the LNAs noise factor is

\[ \text{Noise Factor} = 1 + \frac{\gamma + 4\gamma S_{m1} + 4\gamma S_{m2}}{\gamma S_{m1} + 4\gamma S_{m2}} + \frac{4r_L^2}{S_{m1} S_{m2} R_{eq}^2} + \frac{4r_L^2}{S_{m1} S_{m2} R_{eq}^2} \] (12)

If \( Q \) is sufficiently large, the noise factor can be rewritten as

\[ \text{Noise Factor} = 1 + \frac{\gamma + 4\gamma S_{m1} + 4\gamma S_{m2}}{\gamma S_{m1} + 4\gamma S_{m2}} + \frac{4r_L^2}{S_{m1} S_{m2} R_{eq}^2} + \frac{4r_L^2}{S_{m1} S_{m2} R_{eq}^2} \] (13)

It follows that to minimize the noise factor of the proposed common-gate active-inductor LNA, a large value of \( R_{eq} \) is needed. As \( R \) is normally the dominant term in \( R_{eq} \), the current flow through \( M_o \) should be minimized to obtain a good noise performance. Observe from (1) that to keep constant the desired...
inductance value it is possible to decrease $g_{m2}$ by bringing $12$ and the size of $M2$ to a minimum while simultaneously enlarging $g_{m1}$ by increasing $I1$ and the size of $M1$. This minimizes the third and fourth terms of (13). Also, the last term of (13) can be minimized by biasing $M3$ at a higher gate-source voltage to achieve a relatively small transistor size. However, good linearity requires a large $I2$ bias current and a relatively low quality factor. Moreover, to avoid instability, the high frequency zero should be put beyond the dominant pole $(g_{m2}/c_{os2})$ to avoid the negative resistance. Therefore, trade-offs between noise figure, linearity and stability should be taken into account.

Also, the last term of (13) can be minimized by biasing $MP$ at a higher gate-source voltage to achieve a relatively small transistor size. However, good linearity requires a large $I2$ bias current and a relatively low quality factor. Moreover, to avoid instability, the high frequency zero should be put beyond the dominant pole $(g_{m2}/c_{os2})$ to avoid the negative resistance. Therefore, trade-offs between noise figure, linearity and stability should be taken into account.

V. SIMULATION RESULTS

The proposed circuits were simulated using HSPICE. The transistor model used is MOSIS Bsim1 for the HP 0.5μm CMOS process. Table 2 shows a summary of design parameters for several inductance values. One can see that it is easier to obtain large inductor values through less power consumption.

<table>
<thead>
<tr>
<th>Inductor</th>
<th>$I1$ (μA)</th>
<th>$I2$ (μA)</th>
<th>$I3$ (μA)</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>20nH</td>
<td>400u</td>
<td>500u</td>
<td>100u</td>
<td>3.3mw</td>
</tr>
<tr>
<td>100nH</td>
<td>40u</td>
<td>120u</td>
<td>50u</td>
<td>0.70mw</td>
</tr>
</tbody>
</table>

Fig. 6 shows the programmability properties of the LNA's frequency response and noise analysis. The Noise Figure calculated from this Figure is 3.65dB. The tuning range of the resonant frequency is nearly half decade at 1GHz by varying $I2$. However, when $I2$ varies, the quality factor varies as well which also causes the gain of the amplifier to vary. This variation can be compensated by adjusting $I1$. The result of this fine tuning is that we can keep the gain nearly constant when tuning $I2$ as shown in Fig. 6. The actual tuning range of $I2$ is 50-300μA. Recall that $I1$ is the tuning variable for the quality factor. When decreasing $I3$, the quality factor $Q$ increases, which leads to an increase of the equivalent parallel resistance $Q/R_L$. However, the gain of this LNA is kept nearly stable due to the dominant term of the $R/(r_{ds}/r_{ds})$ in $R_{eq}$. Fig. 7 shows how the noise figure is affected by $I2$. For this plot, $I1$ is varied accordingly to keep a constant inductor value thereby a constant center frequency at 1GHz. The linearity of the LNA, which is normally evaluated by the input-referred third-order intercept point (IIP3), is plotted in Fig. 8. The simulated IIP3 is around -17dBm; however, the 1dB compression point appears around -34dBm. The LNA's nominal gain at 1GHz is 20.5 dB, using an inductor of 50nH. The noise figure is 3.65dB, input matching is 69Ω @ 1GHz, power supply is 3.3v and power dissipation is around 14mW.

The frequency response and noise analysis of the LNA with the cascode active inductor of Fig. 1b is also presented in Fig. 9. The simulated gain is 15.5dB, noise figure is 3.65dB, input matching 57Ω @ 1GHz, IIP3 is 0dBm and $P_{1db}$ is -23dBm. As a way of reference, a comparison between our design using the regulated cascode active-inductor and other designs reported in the literature is presented in Table 3.
VI. CONCLUSION

In this paper, we have presented a single-ended LNA with an active inductor load. We showed how an active inductor is a suitable substitute for its passive equivalent in situations where large inductance values are needed. Careful design optimization leads to an amplifier with minimum noise figure and programmable center frequency.

VII. REFERENCES


