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A Power Supply Ramping and Current Measurement Based Technique for Analog Fault Diagnosis

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Abstract

In this paper we present a methodology for fault diagnosis of analog circuits based on the observation of power supply currents. In the proposed technique, fault signature dictionaries are generated from the currents in the power supply bus. To obtain signatures rich in information for efficient diagnosis, the transistors in the circuit are forced to operate in all regions of operation by using a ramp signal at the supply instead of the conventional constant dc signal. The signatures are then clustered into different groups using a Kohonen neural network classifier. This technique has the potential to detect and diagnose single and multiple shorts as well as open circuits. The theoretical and experimental results of the proposed technique are verified using a CMOS Operational Transconductance Amplifier (OTA) circuit.

1: Introduction

Measurement of power supply currents was found to be very useful for testing CMOS ICs because of its potential to detect a large class of manufacturing defects [1–3]. The power supply nodes are the universal nodes of any circuit in the sense that they are always accessible and provide the necessary bias currents for all the elements in the circuits. As the distribution of the bias currents will be altered upon the occurrence of a faulty condition in the circuit, observing the power supply currents can be fruitful. In digital circuits, current testing is emerging as a very useful tool in detecting delay faults and other process defects which cannot be modeled by the traditional stuck-at models. These techniques basically rely on the fact that, in digital circuits, under nominal conditions, there is little or no supply currents. Any deviations from this nominal behavior result in the flow of abnormal currents which can be used to detect the presence of a fault [4].

However, this supply current monitoring technique has found no applications in analog circuits. To apply the power supply current observation concept to analog fault diagnosis, major modifications should be made to the existing current testing techniques. This is because of two factors: i) the emphasis here is on fault diagnosis which requires more than a simple observation of abnormal currents and ii) unlike in digital circuits, bias currents always exist between the power supplies and in most cases abnormal currents cannot be defined.

The application of a ramp signal at the power supply nodes instead of the conventional step (or dc voltage) can potentially make the majority of the transistors in the circuit operate in all the regions of operation. Namely, they can work in cutoff, weak inversion linear and saturation. Hence, the \( V_{dd} \) ramp signal provides bias currents rich in information. Once the signatures are generated from these current responses, the fault clustering approach presented in [5] and [6] is used to create the fault dictionary. As the occurrence of short (single or multiple) or open circuits can drastically change the amount of current and its flow in the power supply bus, this technique can successfully diagnose faults. This technique is independent of the linearity or nonlinearity of the system, circuit or component. The vector mapping capability of the neural network helps in taking care of the process parameter drifts and component tolerance effects in this approach. Details regarding the Kohonen network can be found in [7].

2: Power supply ramping

Fault diagnosis typically requires a set of signatures, each representing a behavioral condition (we refer to the faulty and fault–free cases as behavioral conditions, BCs), which are often significantly different from each other. For efficient fault diagnosis purposes, the application of a ramp signal at the power supply is investigated in this section. The bias currents existing in the supply bus are a function of the operating point as well as of the topology of the circuit. For a constant supply voltage, this relationship can be represented as shown below:

\[
I_{bias} = f(O, T)
\]

(1)
where \( O \) is the operating condition of the circuit and \( T \), the topology. If either \( O \) or \( T \) of eqn. (1) is perturbed, the supply current changes. Now, consider the application of a ramp signal at one power supply. The ramp signal is shown in Fig. 1 and can be defined as a function of time as \( V_{dd}(t) = V^* t \) for \( t < t_1 \) & \( V_{dd}(t) = VDD \) for \( t > t_1 \) where, \( VDD \) is the desired positive supply voltage.

![Fig. 1: Ramp Signal](image)

From the basic CMOS transistor theory, the operating condition of a circuit can be seen as a function of gate–source (\( V_{gs} \)), drain–source (\( V_{ds} \)) and threshold (\( V_t \)) voltages of each transistor. This can be represented as:

\[
O = f(V_{gs}, V_{ds}, V_t) \tag{2}
\]

Fig. 2 shows a simple CMOS inverter circuit with a current source load implemented by M2. If a ramp signal is applied at the positive supply voltage of the inverter, then \( V_{gs} \) and \( V_{ds} \) of both transistors will also vary with time. The regions of operation of the transistors are defined as:

**Transistor M2:**
- \( V_b - V_{dd}(t) < V_{tp} \) \quad Subthreshold
- \( V_b - V_{dd}(t) - V_{th} > V_o(t) - V_{dd}(t) \) \quad Saturation
- \( V_b - V_{dd}(t) - V_{th} < V_o(t) - V_{dd}(t) \) \quad Linear

**Transistor M1:**
- \( |V_{gs} - V_{ds}| < |V_{tp}| \) \quad Subthreshold
- \( V_b - V_{dd}(t) - V_{th} > V_o(t) - V_{dd}(t) \) \quad Linear
- \( V_b - V_{dd}(t) - V_{th} < V_o(t) - V_{dd}(t) \) \quad Saturation

These basic expressions can be used to obtain the different ranges of \( V_{dd} \) and the corresponding regions of operation of both the transistors. The expressions for the supply current, \( I_{dd} \), can be easily obtained once the regions of operation of both transistors are known.

![Fig. 2: Vdd ramping on a CMOS inverter](image)

Fig. 3 shows the output voltage response for a \( V_{dd} \) sweep of the inverter. The different ranges of \( V_{dd} \) can also be identified in Fig. 3, where \( V_{ss} = -2.5 \text{V} \). At point 1, we have \( V_{dd} = V_b - V_{tp} \); correspondingly at point 2 \( V_o = -V_{th} \) and at point 3 we have \( V_{dd} \) represented at point 2.

![Fig. 3: Regions of Operation of M1 & M2](image)

From the above discussion, it can be seen that power supply ramping changes the operating conditions of the devices involved. This results in variable supply currents. Supply current also varies with time and can be defined as:

\[
I_{dd}(t) = f(O(t), T) \tag{3}
\]

where

\[
O(t) = f(V_{gs}(t), V_{ds}(t), V_t) \tag{4}
\]

For the different regions of Fig. 3, the supply current \( I_{dd} \) can easily be obtained from literature [8].

Common defects inducing bridging faults and open circuits change the topology of the circuit. To this effect, consider a bridging fault between the drain and source of M2. This fault can be modeled as a short circuit with a small resistor (typically of 5 ohms) between \( V_{dd} \) and \( V_o \). Neglecting the small voltage drop across this resistor, we obtain \( V_o(t) = V_{dd}(t) \). As M2 is functionally eliminated in this topology, the region of operation of the remaining transistors (M1 in this case) will be different from the other topologies (caused by other BCs).
For the sake of illustration, the inverter circuit is simulated under nominal and faulty conditions and the plots are shown in Fig. 4. The top plot in Fig. 4 shows the ramp signal applied at the power supply, the plot in between shows the nominal supply current flow and the bottom plot shows the flow of the current with the drain and source of M2 shorted. Under this fault case, M2 can be replaced by a small resistor. Hence, transistor M1 is always in saturation and thus sinks maximum current at all times as seen in Fig. 4. The results show that the circuit can be diagnosed correctly, if the responses of the supply currents are used to obtain the signatures. Hence, it can be concluded that the application of ramp signal at the power supply node is an effective method of generating signatures rich in information.

Fig. 4: Ramp signal at Vdd, nominal and faulty supply current responses.

3: Procedure
The proposed Idd current measurement technique consists of three stages 1) signature generation, 2) signature classification, and 3) diagnosis. The first stage involves the definition of BCs to be considered, generation of the responses for each BC and obtaining signatures from the responses. The BC definitions can be obtained from any approach that models the physical process defects, such as inductive fault analysis [9]. The circuit under test is simulated with each BC induced, and the current response in the power supply bus is noted at m different points of time with the ramp signal applied to the supply node. A set of n optimal sampling points can be chosen from these m points to form a signature of the response. A technique that performs the derivative of each response and forms a set of optimal test points at which there is a significant change in the response value with respect to its previous values is presented in [6].

Next, a Kohonen network (Fig. 5) with n inputs and N processing elements, where N is the number of BCs and n is the dimensionality of the signature, is trained. The Kohonen network maps the signatures from the initial random vector space onto the processing elements. This vector mapping property of the Kohonen network is used to classify the signatures, and thus, to identify the faults. Fig. 6 shows the flow diagram to generate the signatures. These signatures are then used to train a Kohonen network. A cluster table is generated by recording the winner processing unit for each input signature. If a unit wins for more than one signature, then the fault cases associated with those signatures are said to be collapsing faults. These faults cannot be isolated from each other using only these signatures. This phenomenon of reducing the initial vector space, that includes all the signatures, to a vector space consisting of fewer signatures as fault clustering. If this new vector space represented by a unit consists of only a single signature, then the fault case associated with that signature can be isolated. Such a cluster is called an isolated cluster.

The fault diagnosis procedure involves measurement of the power supply current and generation of the test signature. This signature is then used as the input to the trained Kohonen network to obtain the cluster of BCs that best matches the test signature. Thus the BC existing in the circuit can be successfully diagnosed. This procedure is shown in Fig. 7.
The proposed technique is verified on the OTA circuit shown in Fig. 8 with BC definitions given in Table 1. This circuit is simulated using HSPICE with each BC induced one at a time. Data is obtained by measuring the current through the ammeter. The ramp signal with a pulse width of 6ms and a rise time of 24ms is applied at the positive power supply of the circuit. The data is obtained by performing a transient analysis on the circuit swept from 1ms to 29ms with increments of 5ms. These responses are obtained initially with 59 data points. The optimal sampling point analysis on these responses yielded 52-dimensional signatures. The signatures generated for these BCs are then used to train several Kohonen networks according to the Multiple Kohonen Single Analysis approach presented in [5].

To illustrate the multiple bridging and open circuit fault diagnosis capability of the proposed technique, the BCs considered in Table 1 are extended to include a few open and multiple faults. Table 2 gives the definition of the additional BCs considered. It should be observed that the term branch open is used instead of open drain or open source. This terminology is because an opened drain or source on any of the transistors leads to the absence of current flow in that branch.

---

**Table 1. BC definition for the OTA**

<table>
<thead>
<tr>
<th>BC</th>
<th>SHORT BETWEEN NODES</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Fault Free</td>
</tr>
<tr>
<td>1</td>
<td>1 &amp; 2</td>
</tr>
<tr>
<td>2</td>
<td>1 &amp; 7</td>
</tr>
<tr>
<td>3</td>
<td>2 &amp; 4</td>
</tr>
<tr>
<td>4</td>
<td>2 &amp; 15</td>
</tr>
<tr>
<td>5</td>
<td>4 &amp; 7</td>
</tr>
<tr>
<td>6</td>
<td>4 &amp; 12</td>
</tr>
<tr>
<td>7</td>
<td>4 &amp; 13</td>
</tr>
<tr>
<td>8</td>
<td>4 &amp; 16</td>
</tr>
<tr>
<td>9</td>
<td>7 &amp; 8</td>
</tr>
<tr>
<td>10</td>
<td>13 &amp; 15</td>
</tr>
</tbody>
</table>

**Table 2. Extended BC definitions for the OTA**

<table>
<thead>
<tr>
<th>BC</th>
<th>FAULT CASE</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>Branch 1 open</td>
</tr>
<tr>
<td>12</td>
<td>Branch 2 open</td>
</tr>
<tr>
<td>13</td>
<td>Branch 4 open</td>
</tr>
<tr>
<td>14</td>
<td>Branch 5 open</td>
</tr>
<tr>
<td>15</td>
<td>short between 4 &amp; 13</td>
</tr>
<tr>
<td>16</td>
<td>short between 2 &amp; 15</td>
</tr>
<tr>
<td>17</td>
<td>short between 1 &amp; 4</td>
</tr>
<tr>
<td>18</td>
<td>short between 1 &amp; 7</td>
</tr>
</tbody>
</table>
Behavioral Conditions

For the sake of fault injection, open circuits are modeled by a large resistor in parallel with a small capacitor. The KC-Base generated for all the 19 BCs, including the extended BCs shown in the Table 2 is shown in Fig.9. It can be seen that there are only 2 non isolated clusters and each of which contain only 2 BCs. (4,8 and 11, 12). The diagnosis procedure involves the measurement of test signatures from the circuit under test. The diagnosis capability will be as expected and shown in the KC-Base diagrams if there is a good matching between the simulated and measured responses. The measured responses can be given as the input to the Kohonen networks in the KC-Base and the fault cases existing in the circuit can be identified. The OTA was fabricated through the MOSIS 2" tiny chip. For the ease of fault injection, each node of the circuit was made accessible through external chip pads. Test signatures were generated for each of the BCs listed in the Tables 1 and 2. The test signatures obtained were given as input to the Kohonen network trained on the signatures from the simulations. For all the BCs considered, the diagnosis was precise and the induced fault was identified. All the 18 signatures generated from circuit simulation were presented as inputs one at a time to the Kohonen networks in the KC-base, 14 out of the 18 BCs are identified exactly. The BCs 4,8 as well as 11 and 12 were clustered together and the diagnosis result does not distinguish between them.

5: Features and remarks

5.1: Open circuit diagnosis capability

The existing techniques for fault diagnosis of analog circuits do not have the potential to diagnose both shorts and open circuits at the same time. Any open branch in the circuit will result in zero current flowing in the output branch of the circuit. As the proposed technique measures the total current in all branches, the occurrence of opens in various branches will result in different supply currents. Hence, efficient diagnosis of open circuits is possible.

5.2: No additional access points

In this technique, only the power supply node is needed externally for signature generation and measurement purposes. Hence, the cost of increased silicon area needed for more access points is avoided.

5.3: Built-in current monitoring

The currents in the power supply bus can be monitored with additional circuitry. Several techniques have been proposed to measure the supply currents [10–12]. Implementation of these current sensors permits automatic diagnosis capability and can be incorporated in an automatic test equipment. Electron-beam probing can also be used to measure the power supply currents [13].

6: Conclusions

A non-conventional analog fault diagnosis technique based on the application of a ramp signal at the power supply node and the measurement of the supply current, is presented. The proposed methodology is verified with experiments involving a practical CMOS integrated OTA circuit. The features of this technique conclusively prove that this technique overcomes most of the limitations of the present diagnosis methods and can diagnose open circuits.

References


