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160 Gbit/s line-rate data routing through monolithic multi-stage optical switch circuit

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A monolithic, multi-stage, photonic circuit comprising up to four cascaded, SOA-based, crossbar switches is assessed at record 160 Gbit/s serial line rates. Power penalties of only 1.2 dB signify an important route to high-speed, high-density optoelectronic integrated circuits.

Introduction: Optoelectronic circuits with high levels of circuit connectivity and nanosecond time-scale reconfigurability of massively broadband optical signals may play an increasing role in high-capacity data transfer optical networks. Photonic integrated semiconductor optical amplifier (SOA) gate-based circuits have received particular attention owing to the promise of low control complexity with bandwidth independent power consumption and fast reconfigurability [1–3]. Serially multiplexed data formats, on non-critical wavelengths grids, may offer reduced inventory and management simplification. To date, however, ultra-high-speed processing in SOAs has been demonstrated by exploiting nonlinearity in combination with precision filtering [4] or interferometric all-optical switching [5]. This has not allowed sophisticated multi-stage monolithic integration. In this Letter we quantify 160 Gbit/s line-rate data integrity for monolithically interconnected SOA gate switches for the first time. The SOA gates have been integrated to create a scalable optoelectronic monolithic multi-stage optical switching circuit. Power penalty is studied for increasing numbers of SOA switches in the tested paths.

Photonic integrated circuit: The four input, four output multi-stage optoelectronic switching circuit is implemented on an active-passive regrown InGaAsP/InP epitaxial wafer [6]. An N-stage planar architecture [7] using optoelectronic crossbar switch elements connects the inputs to the outputs in an electronically reconfigurable manner. SOA gates enable switching of crossbar states by means of electrical currents to each of 12 control electrodes in the circuit. Fig. 1a shows the arrangement of the optical waveguides and the 12 electrodes. Fig. 1b shows a photograph of the tested circuit attached to a gold-plated AlN tile. Wire bonds are visible at each of the electrodes. The total circuit area is implemented within chip dimensions of 4.3×2.8 mm.

Fig. 1 Integrated multi-stage optical switch
a Schematic diagram showing waveguide and electrode layout
b Photograph of circuit

The crossbar switch element is adapted from a previously presented design [8] now allowing the interconnection of the active SOA gates with passive waveguides for reduced noise performance. At the optical level, two crossbar switch inputs are broadcast to the outputs. SOA gates determine the connections between crossbar inputs and outputs and partially compensate losses from the passive waveguides, splitters and combiners at each stage. At the electronic level, the SOA gates are paired together with common electrodes to give simple cross- and bar-state control. The pairs of SOA gates are also placed within the same active islands by introducing additional waveguide bends and crossings to enable the more compact photonic circuit.

The interconnection of the six crossbar switch stages is implemented using a combination of deep- and shallow-etched passive waveguides. The circuit is folded to accommodate the pre-placed active islands

used for the SOA gates. A mask design error and a short circuit prevent complete connectivity between all optical inputs and optical outputs. Nonetheless, 20 electronically-programmable, intra-circuit paths have been confirmed and are summarised in Table 1. The uncompleted connections are listed as n/c. The N-stage planar architecture is rearrangeably non-blocking [7] and therefore a number of connections include two possible intra-circuit paths. In this work we study ultra-high-speed routing over the shortest two-stage path (I0-O0) and the longest four-stage path (I0-O2) as shown in Fig. 1a.

Table 1: Interconnection table showing on-state SOA gates for confirmed intracircuit paths

		Outputs			
		O0	O1	O2	O3
Inputs	I0	ac	n/c	bcek, bfil	becl, bfik
	I1	bc	n/c	acek, afil	acel, afik
	I2	n/c	hi	cfgk, egil	cfgl, egik
	I3	n/c	gi	cfhk, ehil	cfhl, ehik

High-speed transmission: The 160 Gbit/s serial data is generated with an optically time division de/multiplexed [9], single-wavelength data channel centred at 1550 nm using the arrangement shown in Fig. 2. An aggregate optical power of +7 dBm in-fibre is injected into the circuit with the polarisation state optimally aligned. Reflections from the as-cleaved facets can lead to oscillation at high current. This may be suppressed with appropriate antireflection coatings to facilitate net gain. In this work, operating fibre to fibre losses are −13 and −15 dB for the two- and four-stage paths, respectively. Losses here are dominated by fibre to chip coupling. Electrodes *a* and *c* are each biased at 120 mA for the two-stage path. Electrodes *b*, *c*, *e*, *k* are biased at 85, 100, 120 and 130 mA, respectively, for the four-stage path.

Fig. 2 Experimental arrangement for BER assessment of multi-stage optical switch at 160 Gbit/s

Erbium-doped fibre amplifier (Amp), optical bandpass filter (BPF), variable optical attenuator (VOA)

Fig. 3 BER performance at 160 Gbit/s serial line rates

Demultiplexed channels denoted by triangles, diamonds, squares, circles. Open black symbols denote back-to-back performance without switch. Solid symbols denote routing through two stages. Open symbols denote routing through four stages

Power penalty performance is assessed from the bit error rate (BER) dependence on received power as shown in Fig. 3. Back-to-back measurements of the error rate performance are made without the inclusion of the photonic integrated circuit. Subsequent comparative measurements are made after routing the data through two and four SOA gate stages. Power penalties from 0.5 to 0.7 dB and from 1.0 to

1.2 dB are observed for the two and four stages, respectively. These values are sensitive to the electrode bias currents. The eye diagram after four-stage routing is shown in Fig. 4 with a clear opening between the ones and the zeros levels.

Fig. 4 Eye diagram for 160 Gbit/s data at output after four stages of crossbar switch elements

Conclusion: Power penalties of 1.2 dB are achieved at 160 Gbit/s serial data rates over four stages of crossbar switches in a monolithic interconnection architecture. This represents an important milestone in high-bandwidth monolithic circuit integration and offers a highly promising route to large-scale ultra-high-line-rate optoelectronic circuits.

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One or more of the Figures in this Letter are available in colour online.

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