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Abstract: A compact scalable reconfigurable multiwavelength router is proposed and demonstrated using an electronically gated cyclic router. Simultaneous wavelength-multiplexed channel allocation is performed with power penalties of 0.2–0.8 dB. Nanosecond timescale reconfiguration is achieved within a 2-ns guard band using semiconductor optical amplifier gates.

Index Terms: Optical communication, wavelength-division multiplexing, tunable filters, semiconductor optical amplifiers.

1. Introduction

There is an increasing need for fast-programmable, wavelength-division-multiplexed (WDM) optical links in telecommunications backbones [1], interconnection systems [2], and access networking [3]. Increasingly complex and power efficient circuits operating at higher data rates have lead to a renewed effort to develop integrated optoelectronic sub-systems. Assembly is simplified, and losses are removed through a reduction in the number of unnecessary fiber-to-chip interfaces. The additional opportunities for parallel optoelectronic processing in wavelength-multiplexed links offer an important route to further hardware efficiencies.

Integrated circuits for multiwavelength links have been proposed using Bragg grating filters [4], [5], ring resonators [6], [7], and arrayed waveguide gratings [1]–[3], [8], [9]. Circuit-level implementation with gratings and ring resonators is frustrated by the tight fabrication tolerances and intrinsically low number of output ports. In contrast, arrayed waveguide gratings, offer robust passband specification, polarization and temperature insensitivity [10], and loss-independent scaling to hundreds of connections [11]. Fast reconfigurability may be introduced through either semiconductor optical amplifier (SOA) gate arrays or electro-optic phase tuning. The individual SOA gating of wavelength channels between paired arrayed waveguide gratings has already enabled fast wavelength blocking for a single-input–single-output circuit [2]. Fast-programmable electro-optic phase shifters within delay-matched arrayed waveguides have enabled excellent wideband unicast routing with up to 16 outputs [8], [9]. Cyclic router operation in the arrayed waveguide gratings allows an additional multiwavelength routing function [12], but reconfigurable cyclic routers have yet to be studied.
In this work, we propose, fabricate, and characterize a reconfigurable cyclic router. Fast reconfigurability is enabled by the integrated SOA gate array which operates with simple digital signals. The cyclic router offers inherently scalable, multichannel, parallel processing and is programmable in both space and wavelength. The circuit concept is presented in Section 2. Component-level characterization is described in Section 3. Low-power penalty data routing is studied for two modes of multiwavelength operation in Section 4, signifying a route to hardware and energy-efficient networking. Nanosecond reconfigurability is analyzed in Section 5 by means of full bit error assessment to show high link utilization.

2. Fast-Programmable Cyclic Router

The cyclic router circuit is designed to allow the selective routing of bands of wavelength channels to any of the four outputs by selectively biasing the four SOA gates. The input signal is broadcast to the gate array, and appropriate electrical biasing of the gates determines the circuit transfer function, allowing multiple wavelengths to be simultaneously routed. The mapping of the four wavebands to each of the four outputs is shown in Table 1. The free spectral range for the presented $4 \times 4$ router is five times the channel separation, leaving one band unconnected for each free spectral range.

The circuit layout is shown schematically in Fig. 1. The waveguide mask layers and the active island mask are shown, highlighting the placement of the input, outputs, enumerated SOA gates, and the cyclic router. Both shallow- and deep-etched waveguides are used within the circuit. The waveguides are highlighted in black, and the regions for deep-etched sidewalls are denoted by the grayed areas. The input waveguide at the right-hand side is angled at 7° off facet-normal for reduced reflectivity. A fundamental-spatial-mode filter implemented with a $1 \times 2$ multimode interference coupler is used to condition the signal propagating into the circuit. Two stages of $1 \times 2$ multimode interference (MMI) splitters are then used to broadcast the input to each of the SOA gates. The use of cascaded $1 \times 2$ splitters, rather than a single-stage $1 \times 4$ splitter, is believed to allow an improved splitting uniformity with a relaxed fabrication tolerance. Deep-etch waveguides are used to allow tight bend radii. Shallow-to-deep waveguide transitions are implemented on each side of the active island. The SOA gates at the central active island are implemented as shallow-etched, ridge-waveguide devices for improved efficiency. The four SOA gates each have a length of 140 $\mu$m and are angled at 12° relative to the active island length. These fit within the same compact $30 \times 750$ $\mu$m active island, and all the circuit elements are accommodated into a small area of under 5 mm$^2$ with a total chip length of 4.6 mm.

The circuit is implemented monolithically on a regrown active-passive InGaAsP/InP epitaxy [13], [14]. The active region comprises four InGaAsP quantum wells with the gain centered at 1550 nm. The passive waveguide structure consists of a 500-nm core with quaternary composition $Q = 1.25$ $\mu$m sandwiched between binary InP alloy epitaxial layers. Shallow- and deep-etched
waveguides are defined by a two-step reactive ion etch. The first step is performed with the shallow waveguides masked. Deep-etch waveguides are used to define the waveguide splitters and tight waveguide bends. Radii of down to 100 $\mu$m are used both entering the cyclic router and within the cyclic router itself. Fig. 2 shows a micrograph composed from detailed scanning microscope images of the device at the central part of the circuit. The cyclic router and the SOA gate array are visible with the four p-type gate electrodes.

3. Circuit Operation

The cyclic router is designed with a channel spacing of 3.2 nm (400 GHz) and a free spectral range of 16 nm (2 THz). A two-etch-step process [15] defines the compact cyclic router. In the architecture [16] studied in this work, this results in deep-etched arrayed waveguides of radii varying from 100 $\mu$m to 220 $\mu$m between the shallow-etched free propagation regions. No passband flattening is implemented. The spectral response is initially analyzed through simulation with the Agilent Advanced Design System microwave simulation tool. Transfer functions are plotted in Fig. 3(a). Transfer functions from the single input to each of the four outputs are shown overlaid. A uniform spectral performance with less than 2-dB variation is predicted across a bandwidth of 100 nm. Six passbands are feasible within the measured range of 100 nm for each of four wavebands and four paths. Up to four of the wavebands may be simultaneously routed from the one input to any combination of the four outputs. It is also feasible to route densely spaced wavelength-multiplexed channels within each passband. Both modes of operation are studied in Section 4.

The transfer function is studied initially in terms of the experimentally measured amplified spontaneous emission spectra. The SOA gate is biased at 50 mA. The four output side spectra are overlaid in Fig. 3(b) for SOA gate 1 enabled. Comparable responses are also observed for all combinations of gates and outputs. Four wavebands are seen for each free spectral range, and the fifth is skipped as designed. The unfiltered spontaneous emission from the input side is also shown with a variation of under 4 dB over the 100-nm measurement range. Lensed fibers are used for...
fiber-chip coupling with an estimated facet to fiber loss of 6 dB. The measurement resolution bandwidth is 0.1 nm. Good qualitative agreement is observed between the experimental and simulated transfer functions. The mean and standard deviation for the difference between simulated and measured passband peaks is measured to be 0.32 nm and 0.26 nm, respectively. Channel walk-off is observed leading to a free spectral range variation from 15.2 nm to 16.8 nm over the six bands.

SOA gate characteristics are not directly quantifiable, and so, transparency current is first determined to infer the absolute SOA gain. An injected optical input signal is chopped at 200 Hz and detected under forward biased conditions with a bias tee. The amplitude of the chopped signal passes through a minimum as the DC bias current is scanned from the absorbing regime to the amplifying regime, giving an estimated amplifier transparency current of 6 mA (1.8 kA/cm²). Dependence of gain on bias current subsequently indicates an on-state SOA gain of 3.5 dB and off-state loss values exceeding 10 dB. The gain saturates at a current of 26 mA, and this operating point is selected for routing measurements.

Passive component and waveguide losses are estimated to be 17 dB by measuring on-chip loss for the SOA gates biased at transparency. Simulations for circuit elements and measurements on isolated test structures indicate that this loss comprises 3.5 dB for the waveguide splitters, 0.5 dB for the mode filters, 4 dB for the cyclic router, and 3 dB for the waveguides, underestimating the total measured on-chip loss by only 2 dB.

4. Wavelength-Multiplexed Data Routing

Routing is studied for the case of: i) single wavelength routing, ii) waveband multiplexing, and iii) the combination of in-band plus waveband multiplexing, to explore performance with increasing data rate. Fig. 4(a) shows the experimental arrangement for the assessment of one up to three simultaneously routed wavelength channels for these modes of operation.

The WDM transmitter comprises of wavelength-multiplexed lasers operating with 7-dBm continuous wave output power. The channels are externally modulated at 10 Gb/s, and optical data is decorrelated using 10 km of standard dispersion fiber before the input of the circuit under test. Two wavelength channels (1538.3 nm and 1539.1 nm) are set within the same passband (within waveband 3) to study in-band multiplexing. A third wavelength channel (1554.2 nm) is offset by one free spectral range of the cyclic router to enable the study of the waveband multiplexing scheme ii). The combination of all three wavelengths allows simultaneous in-band and waveband multiplexing iii).

Bit-error-rate measurements are performed using a 2³¹ – 1 pseudo random bit sequence. Selective biasing of the SOA gate electrodes enables waveband allocation to each of the output ports as listed in Table 1. The routed signals are subsequently demultiplexed and assessed with an error detector. Bit error rates measured for the wavelength channel at 1554.2 nm are shown in Fig. 4(b). A low power penalty between 0.2–0.8 dB is achieved for multiple channel operation. The logarithmic dependence of error rate on received power implies performance is limited by noise.
The multiplexed performance for three wavelengths gives a penalty of only 0.2 dB. This improvement with increasing channel number has been previously observed for multiwavelength switching [17]. This is believed to result from reduced aggregate power fluctuations when summing wavelength channels with decorrelated bit sequences. Bit-error-rate measurements for the other two channels were also performed and show consistently low, wavelength-multiplexed penalties between 0.2–0.8 dB as well.

5. Nanosecond Programmable Routing

The impact of nanosecond switch transitions on data integrity is studied by inputting wavelength-multiplexed data to the circuit and periodically changing the operating state of two SOA gates. The guard-band time allowed for switching between operating states is set at 2 ns to allow for the transition time for the electronic signal generator and the imperfect impedance matching at the photonic circuit. The SOA gates are impedance matched simply with $37\Omega$ surface mount resistors. The 10–90% switching response of the SOA was measured to be 1.4 ns for continuous-wave optical signals.

The experimental arrangement to study dynamic optical routing of wavelength channels is shown in Fig. 5(a). Two multiplexed wavelength channels (1544.2 nm and 1547.5 nm) are amplitude modulated at 3 Gb/s using a shorter pseudo random bit sequence of $2^{15} – 1$ length and input to the router. The trigger signals derived from the pattern generator and used to synchronize the switch electronics impose the shorter pattern sequence and define the packet length at 87.3 $\mu$s. The sequence is repeated without deliberately introduced guard bands or preambles. The two wavelength channels are individually routed to the same port by alternating the bias state of SOA gates 1 and 2. The output from the router is amplified, and out-of-band amplified spontaneous emission is removed with a dual-band filter constructed with a delay-matched de/multiplexer pair.
The time-resolved dynamic operation is shown in the oscilloscope traces for Fig. 5. SOA gates 1 and 2 are switched with complementary 2-V square wave signals to enable the routing of the two wavelength channels to the same outputs in consecutive time periods. Output port 1 is monitored for the periodically gated router for the two wavelengths individually input (b) and (c) and then simultaneously (d). The time traces show that the data sequence is transmitted only for the on-state of the corresponding SOA gate. For the off-state, the transmission is suppressed. When both the wavelength channels are present, a repeated data sequence encoded over two time-interleaved wavelength channels is received, as shown in Fig. 5(d). This oscilloscope trace shows a stable transition between packets as the circuit is reconfigured.

Bit-error-rate measurements for the received optically time-multiplexed data are performed and shown in Fig. 5(e). Comparisons are made between the dynamically switched operation and non-switched state for each of the SOA gates. Error performance is also recorded with the circuit completely removed. A change in receiver circuit leads to a change in absolute sensitivity. The additional power penalty results from the doubling of the amplified spontaneous emission bandwidth when using dual-channel filtering. Dynamically routed time-multiplexed data exhibits a power penalty of 3.0 dB, which is only marginally higher than the values measured for static operation. Two data points even imply that a negative power penalty can be achieved, but the logarithmic trend lines indicate that this is within measurement accuracy. This dynamic power is measured for all bits received at the output with a very short 2-ns guard time signifying a very high link utilization.

6. Discussion

The nanosecond-reconfigurable waveband router provides simultaneous and dynamic multichannel operation and a route to capacity scaling using both in-band and waveband multiplexing. In this design, up to six wavelength channels can be used for waveband multiplexing over 100-nm bandwidth, allowing energy-independent data-capacity scaling. Low gate-operating powers (26-mA current and 1.34-V voltage) per gate already leads to picoJoule per bit optoelectronic switching energy (1.16 pJ/bit) for the $3\lambda \times 10$ Gb/s data rates demonstrated. The digital mode of operation is feasible with simple, low-speed, electronic circuitry. The use of only 2-ns guard time for $2^{15} - 1$ packet patterns signifies very high optical layer link utilization in the experiments performed.

The cyclic router architecture is intrinsically scalable to larger port counts. The cascaded MMI stages for the SOA gate array do, however, add $3.5 \log_{2} N$ dB to the on-chip loss for N connections. Loss-free operation does, however, remain a possibility through increased gain in the SOAs gates. This would also enable an improved extinction ratio and thereby reduce problematic crosstalk [18], which would be necessary for higher connectivity and higher numbers of channels. A more sophisticated space switch preceding the cyclic router will additionally enable more sophisticated system-level routing.

7. Conclusion

The first demonstration of a gated cyclic router is presented. Multiband operation for $3\lambda \times 10$ Gb/s channels with 0.2–0.8-dB power penalty is shown. A power penalty of 3.0 dB is measured for nanosecond timescale dynamic wavelength routing. With a compact chip area of less than 5 mm², simplified digital control, and a fabrication-tolerant, scalable design, this is a highly promising approach to hardware-efficient, wavelength-agile networking.

References


