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A 30GHz Integrated Time-Division Multiplexing Front-End for Phased-array Applications in SiGe

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Abstract—This paper presents a fully integrated receiver front-end for time-division multiplexing phased-array system. The 30GHz front-end includes a low-noise amplifier (LNA), a 4:1 multiplexer, a mixer, and a clock sequencer. The circuit has been implemented in a 0.25 μ m, 130GHz- f_T SiGe process. The front-end shows a input reflection coefficient (S11) of -20dB, a minimum measured LNA-Multiplexer noise figure (NF) of 4.1dB, and a maximum conversion gain (CG) of 18.9dB at 30GHz. Measurements show a 1dB input compression point of -32.3dBm, a third order intercept point (IIP₃) of -22dBm, and a channel isolation of 23dB at 30GHz. This system reduces receiver power consumption by reducing ADC numbers.

I. INTRODUCTION

Today, wireless communication systems are moving towards high frequencies in order to satisfy the increasing bandwidth demands. Local Multipoint Distribution Services, LMDS [1], can be considered as one of these applications, operating at 28.5GHz with a signal bandwidth of 28MHz. At high frequencies, the reduced antenna size makes the multiple antenna system an attractive solution. The main advantage of phased-array receive is SNR enhancement. Analog beam-forming (ABF) combines the signal from each antenna in analog domain and relax the dynamic range of the following receiver blocks. However, the phase information from each antenna is also lost.

Figure 1. Time-division multiplexing phased-array receiver block diagram.

On the other hand, digital beam-forming (DBF) convey signal amplitude and phase into digital domain, which provides more flexibility and control of the signal by applying various algorithms. Nevertheless, the hardware replication, especially the power hungry ADCs, will increase the overall power consumption, area and cost.

As such, an alternative phased-array system that preserves signal information and reduces ADC power consumption is needed. Fig. 1 shows the block diagram of such a phased-array system. It combines N paths into one path by time-division multiplexing. All the blocks after the multiplexer, namely mixer, low pass filter, and ADC are shared by N channels. Hence the power consumption, especially the ADC power consumption, is scaling proportionally to the ratio of bandwidth expansion coefficient and N. Because of the sub-sampling behavior, there are two conditions needed to be fulfilled for the proper use of this system. First, the received interference level should be low, and second, the phase difference of the incoming signal should be small.

In this paper, we present a 30GHz solution for the system. Alongside the specifications of LMDS applications, this article aims to explore the capabilities of this concept in the sense of larger bandwidth, e.g. 500MHz. The system trade-offs will be discussed in section II. Section III gives the detailed design method for each building block. The measured results of the individual block and the system are given in section IV.

Figure 2. Spectrum of the baseband signal after down-conversion.

Figure 3. Simplified schematic of the LNA, Multiplexer, and Mixer.

II. PHASED-ARRAY SYSTEM

The time-division multiplexing phased-array receiver uses a clock controlled multiplexer to combine N paths into one. The combined path contains the signals from the various paths in different time slots. After down-conversion, low-pass filtering, and digitization, the time multiplexed signal is demultiplexed by the synchronous clock to recover the original N signals in digital domain. Then, the signals are processed by beam-forming algorithms. As this system differs from a conventional receiver system, there are a few parameters which need to be considered carefully:

- The multiplexer essentially incorporates a switch for each path which loads the LNA and drives the mixer. To minimize the influence to the LNA and mixer when changing of the switch status, the input (S11) and output (S22) matching of the multiplexer should be maintained regardless of the switch status. Moreover, to retain all amplitude and phase information from each antenna element to DSP without mixing between each channel, the forward (S21) and reverse (S12) isolation of the OFF switch should be high enough to eliminate signals from other paths.
- To recover the signal from each path correctly in digital domain, the sampling rate for each path (f_s) must fulfill the Nyquist sampling theory: $f_s > 2 \cdot BW$, where BW is the single side bandwidth of the incoming modulated signal. As a result, the multiplexer sampling rate f_{MUL} can be expressed as: $f_{MUL} = N \cdot f_s > 2N \cdot BW$ (as shown in Fig. 2 when $N=4$), which means that the incoming signal bandwidth is limited by the multiplexer switching speed. LMS applications demands a $f_{MUL} > 224\text{MHz}$ and applications of 500MHz require a $f_{MUL} > 4\text{GHz}$.

III. TECHNOLOGY AND CIRCUIT DESIGN

The technology used for the design is the $0.25\mu\text{m}$ SiGe BiCMOS process developed by NXP semiconductors [2]. It provides HBT transistors with 130GHz f_T and 140GHz f_{max} , respectively. The system consists of: LNA, multiplexer, mixer, and clock generator. The design methodology of each

block will be described in detail in the following sections.

A. LNA Design

The differential LNA (as shown in Fig. 3) consists of inductively degenerated cascade Q1-Q2 and Q3-Q4, driving load inductors LC1-LC2. Inductors LB1-LB2 and LE1-LE2 are selected together with the emitter width of Q1-Q2 in order to realize noise and impedance matching simultaneously. Scaling input transistor Q1-Q2 ($0.4\mu\text{m} \times 9.1\mu\text{m}$) brings the real part of the optimum source impedance for minimum noise figure close to 50Ω at 30GHz . Gyration of the emitter impedance of LE1-LE2 in series with the base resistance of Q1-Q2 sets the real part of the input impedance to 50Ω thereby matching $Re[Z_{in}]$ with in the desired operation range. The inductor LB1-LB2 connected in series with the base is made series resonant with the input loop to set the imaginary part of the input impedance. Inductors LC1-LC2 are selected as matching components to tune the LNA output and the following multiplexer input at 30GHz .

B. Multiplexer Design

The circuit implementation of the multiplexer is shown in Fig. 3. It consists of parallel identical switches 1-4, with shared output load inductors LC3 & LC4. The switch uses current steering technique to minimize switching time. A differential common-emitter stage, formed by transistor pair Q5-Q6, translates voltage into current. The switching function is achieved by transistors Q7-Q10, where transistor pair Q8-Q9 provide the core amplification element of the switch. When control voltage CO1 is high, Q8 & Q9 are biased in forward active region, and Q7 & Q10 are in cut-off region, thus allowing the signal to pass from port 1 to 5. When CO1 is low, the bias current is steered toward transistors Q7 & Q10, which connects port 1 directly to the supply.

This topology inherently implements an absorptive switch. At input ports 1-4, it is ensured that the total current flow through the input transistors is always constant. At output port 5, the total current flow through the load inductors is also constant. Hence, the source and load impedance of the low noise amplifier and mixer will remain constant regardless of the state of the switch.

C. Quadrature Mixer Design

The mixer design is a double-balanced Gilbert cell as shown in Fig. 3. It down-converts the RF signal at 30GHz to the IF frequency of 10GHz. Further down-conversion will be considered in the future design. The trans-conductance portion of the mixer Q11-Q12 interfaces with the multiplexer output by inductors LC3 & LC4, and it is optimized to achieve the highest power gain and the lowest noise figure simultaneously. The bias current density and transistor size of the switching parts Q13-Q16 were chosen for the highest operating speed to maximize the conversion gain. The emitter degeneration resistors RE1-RE2 and the loading resistors RC1-RC2 are designed to trade-off the gain and the linearity performance of the mixer.

D. Clock Generator Design

The timing clock generator generates the control signals CO1-CO4 by proper division of an input clock signal. It converts the input clock into four non-overlapping pulses, each with 25% duty cycle. The timing circuit is driven by a sinusoidal input clock but its operation is digital, divided in two parts: a modulus 4 counter and additional logic to obtain the four outputs. Table 1 represents the operation states of the timing circuit. The modulus 4 counter is implemented as a two bit counter. The counting is done in gray mode instead of binary. In this way, only one bit changes at the transition between states. This is important in high-frequency operation because it eliminates overlapping and glitches on CO1-CO4 if the outputs O0 and O1 have different

Figure 4. Timing clock generator circuit.

Figure 5. Simulated timing clock generator waveforms.

TABLE I.
TRUTH TABLE OPERATION OF THE TIMING CIRCUIT.

Q1	Q0	CO1	CO2	CO3	CO4
0	0	1	0	0	0
0	1	0	1	0	0
1	1	0	0	1	0
1	0	0	0	0	1

switching speed. The circuit including the modulus 4 counters and additional logic is represented in Fig. 4. The D-type flip-flops provide Q0 and Q1 outputs according to Table 1 ($D1 = Q0$ and $D0 = Q1$). The outputs CO1-CO4 are obtained by combining the flip-flop outputs Q1 and Q0 using only NOR gates. Fig. 5 shows the simulated waveforms of the outputs CO1-CO4 connected to the switching input of the switch cells. The simulations were performed with a 4GHz input clock with no overlapping on the outputs. The voltage swing on each output is larger than 300mV, which is adequate to drive the switch well into ON/OFF state.

IV. MEASUREMENT RESULTS

The measurements were performed on three different circuits. All measurements were performed on-wafer. Millimeter wave G-S-G-S-G probes are used to probe the RF, LO, CLKIN, and IF ports. The DC signals are supplied by multi-contact probe, and in the system measurement, the VCC is supplied by a needle probe. For demonstration purpose and also to reduce the complexity, only one LNA was fabricated in this work, which means only one channel out of four was activated. The other three channels were internally terminated by 100Ω resistors.

A. LNA-Multiplexer Measurement

The performance of the LNA-Multiplexer combination is measured with controllable switches. Fig. 6(a) and (b) show the S parameters of the circuit when the switch is at ON/OFF situation, respectively. S11 (-20dB) and S22 remain constant regardless of the switch status. The transmission, measured by S21 is 14.4dB (ON) and -9.3dB (OFF), which gives 23dB isolation between each RF channel. Fig. 8(a) shows the comparison between simulated and measured noise figure. The minimum measured noise figure was 4.1dB at 30GHz.

B. Front-end Measurement

The front-end measurement includes the LNA, the multiplexer, and the mixer with controllable switches. To evaluate the linearity of the front-end, both 1-dB compression point (P_{1-dB}) and input third-order intercept point (IIP_3) were measured. Fig. 7(a) shows the front-end 1-dB compression point measurement with a RF input signal sweeping from -45 to -20dBm at 30GHz, a -5dBm LO signal at 20GHz, and the IF output power was measured at 10GHz. The measured P_{1-dB} is -32.3dBm. For the IIP_3 measurement, two tones were applied to the RF input to generate IF signals at 9.999 and 10.001GHz. The third order intermodulation (IM3) products appear at 9.997 and 10.003GHz, respectively. The results are shown in Fig. 7(b). The measured IIP_3 of the circuit is -22dBm. The conversion gain of the front-end was measured

with both ON/OFF switch situations as shown in Fig. 8(b). The RF frequency was swept from 21 to 39GHz with -33dBm input power. The measured maximum conversion gain is 18.9dB at 30GHz, and the channel isolation is 23dB, matched with the isolation measurement result in the previous section.

Figure 6. LNA-Multiplexer S-parameter measurement (a) ON (b) OFF.

Figure 7. Front-end linearity measurement (a) IP_{1-dB} (b) IIP_3 .

Figure 8. (a) LNA-Multiplexer noise figure measurement. (b) Front-end conversion gain measurement with switch ON and OFF status.

Figure 9. System die photograph

Figure 10. Measured system output spectrum (IF).

C. System Measurement

The system measurement includes the LNA, the multiplexer, the mixer, and the clock generator. A micro photograph of the fabricated circuit is shown in Fig. 9.

Fig. 10 shows the output spectrum of the mixer with a -38dBm RF signal input at 30GHz, -5dBm LO signal at 20GHz, and -10dBm clock signal at 4GHz (1GHz clock for each channel). The output behaves as a switched 10GHz tone with 1GHz sampling spacing and 25% duty-cycle, confirmed by the theory shown in Fig. 2. Compared to a conventional receiver, the multiplexer with 25% duty cycle receives 1/4 of the input signal power, which gives another 12dB drop for the 0th order harmonic at 10GHz (this drop will be compensated in the digital domain by combining 4 paths together). Considering also the 3dB loss in each cable, 4.7dB loss in each balun-probe setting and the conversion gain of 18.9dB, the output power at 10GHz can be calculated as:

$$\begin{aligned} & \underbrace{-38dBm}_{\text{input power}} \underbrace{-3dB}_{\text{cable loss}} \underbrace{-4.7dB}_{\text{balun loss}} \underbrace{+18.9dB}_{\text{F-E gain}} \underbrace{-12dB}_{\text{sampling loss}} \underbrace{-4.7dB}_{\text{balun loss}} \underbrace{-6dB}_{\text{cable loss} \times 2} \end{aligned}$$

Resulting in -49.5dBm, which closely agrees to the value shown in marker 1 (Fig. 10).

V. CONCLUSION

An integrated 30GHz time-division multiplexing phased-array front-end system, in a 0.25 μ m SiGe process has been presented. The complete circuit occupies 1.1 mm², and dissipates 72mA from 3.3V supply. The design provides 18dB conversion gain, -20dB matching, 4.1dB LNA-multiplexer NF, -22dBm IIP3, and 23dB channel isolation at 30GHz. The system output spectrum shows a switched 10GHz tone with 1GHz sampling spacing and 25% duty-cycle, which matches the sampling theory and confirms that this design is capable of reducing receiver power consumption by reducing ADCs.

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