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Fully Balanced 60 GHz LNA with 37 % Bandwidth, 3.8 dB NF, 10 dB Gain and Constant Group Delay over 6 GHz Bandwidth

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Abstract — This paper presents a two-stage fully integrated 60 GHz differential Low Noise Amplifier implemented in a TSMC bulk CMOS 65 nm technology. Implementation of a voltage-voltage feedback enables the neutralization of the Miller capacitance and the achievement of flat gain with a deviation of ± 0.25 dB over the entire 6 GHz bandwidth. It features a transducer gain (Gt) of 10 dB along with a noise figure (NF) of 3.8 dB, NF_{min} of 3.7 dB and a constant delay time. IIP3 is 4 dBm. It consumes 35 mW from a 1.2 V supply and only occupies 330 x 170 μm .

Index Terms — Millimeter wave amplifiers, transformers, broadband amplifiers, CMOS analog integrated circuits, 60 GHz, LNA.

I. INTRODUCTION

The market demand for RF transceivers providing communication links of several Gb/s data rate motivates the use of the broadband WPAN ISM band at 60 GHz. These systems require receivers with a low noise figure (NF) and flat band response because of the complex modulation scheme. Combination of low NF, sufficient bandwidth, high gain and low voltage operation are important properties of LNAs.

The design of mm-wave LNAs in CMOS causes many challenges because of lossy passives and the Miller capacitance. Several LNAs have been reported in recent years [5]–[9]. To defeat the loss in the passives, SOI technology [6] has been used and in order to neutralize the Miller capacitance, cascode has been applied [7], [9].

This paper describes a fully differential 60 GHz LNA (Fig. 1) in bulk CMOS employing transformer feedback resulting in a flat and broadband response. Miller effect is defeated using gate-drain capacitance neutralization [1], which is achieved when the following equation is satisfied (n is the transformer turn ratio and k is its coupling factor):

$$\frac{n}{k} = -\frac{C_{gs}}{C_{gd}}, \quad n = \sqrt{\frac{L_d}{L_s}} \quad (1)$$

The circuit design procedure and the transformer design are discussed in section II and III. Section IV discusses

the layout. The simulation results pre and post layout are shown in section V and section VI shows the measurement and verification results. In section VII the presented LNA is benchmarked against 60 GHz LNAs found in literature.

Fig. 1. Circuit of the V-V transformer FB LNA as discussed in [1]. The coupling is indicated by the symbols next to the coils.

II. DESIGN PROCEDURE

Main design goal for the LNA is low NF combined with a high gain. Both are a function of MOS transistor bias and width, passives choices, and source impedance Z_{src} . The MOS transistor bias was chosen as a compromise between noise and gain performance. The small signal circuit is shown in Fig. 2.

A. Transformer Specifications and Voltage Gain

To achieve C_{gd} neutralization, the transformer turn ratio n divided by the coupling factor k should be equal to the ratio between C_{gs} and C_{gd} with a negative sign (1), which is approximately 2.3 in the used technology.

To maximize gain, the turn ratio should be as high as possible and L_s should resonate with $(n^2 C_{gd} + C_{gs})$ to tune out these parasitic capacitances. The former leads along with (1) to a high $|k|$ (which is ± 1 at maximum), and the latter sets the inductance value for the inductors used in the transformer. The resulting voltage gain then converges to n . Given a certain MOS transistor width at the chosen bias the transformer properties are thereby known.

Fig. 2. Small signal circuit of the V-V transformer feedback LNA. For reasons of clarity the single ended circuit is shown.

B. Input Impedance

The input impedance with $k \approx -1$ is shown in (2):

$$Z_{in} = 2 \left(R_g + \frac{1}{j\omega C_{gd} (1+n)} + j\omega L_g \right) \quad (2)$$

To create a resistive input impedance, L_g is chosen to resonate with $(1+n)C_{gd}$. This also maximizes the gain.

C. Noise Figure

The calculated noise factor F is given below, in which γ is a process dependent variable:

$$F \approx 1 + 2 \frac{R_g}{R_{src}} + \quad (3)$$

$$2 \frac{\gamma g_m}{R_{src}} \left| \frac{R_{src} + 2j\omega L_g}{2} \left(\frac{\omega^2}{(1+n)\omega_t^2} + \frac{j\omega}{\omega_t} \right) + \frac{1}{g_m} - \frac{j\omega}{g_m(1+n)\omega_t} \right|^2$$

$$\approx 1 + 2 \frac{R_g}{R_{src}} + 2 \frac{\gamma g_m}{R_{src}} \left| \frac{R_{src} + 2j\omega L_g}{2} \cdot \frac{j\omega(C_{gs} + C_{gd})}{g_m} + \frac{1}{g_m} \right|^2$$

$L_{g,opt,NF}$ and $R_{src,opt,NF}$ are, after differentiating (3):

$$\frac{\partial F}{\partial L_g} = 0 \rightarrow L_{g,opt,NF} = \frac{1}{\omega^2 (C_{gs} + C_{gd})} \quad (4)$$

$$\frac{\partial F}{\partial R_{src}} = 0 \rightarrow R_{src,opt,NF} = \sqrt{\frac{R_g}{\gamma g_m}} \quad (5)$$

Combining equations (2), (4) and (1) with $k \approx -1$ it is seen that $X_{src,opt,NF} = X_{in}^* = 0$ can be created at the center frequency resulting in low NF and high G_t . Comparing equations (2) and (5) it follows $R_{src,opt,NF} \neq R_{in}$ so a tradeoff is made between NF and G_t . To increase G_t two stages were cascaded. The F_{min} of the LNA is equal to:

$$F_{min} = 1 + \frac{2\omega}{\omega_t} \sqrt{R_g \gamma g_m}, @ 60\text{GHz} \rightarrow 1 + \sqrt{R_g \gamma g_m} \quad (6)$$

Fig. 3. Used transformer structure. For reasons of clarity the vias connecting the two bottom metals are only shown at the beginning and at the end of the metal strips. In reality many vias are distributed along the metal lines. The top inductor (L_s) connects two metal lines in parallel to lower the inductance and increase the Q-factor. The lower inductor (L_d) has two turns. The two inductors are placed exactly on top of each other to achieve the highest possible coupling ($|k| \leq 1$). The width of the metal lines is chosen to be $3 \mu\text{m}$. This decision constitutes a trade-off between Q-factor and resonance frequency [4].

III. TRANSFORMER DESIGN

The transformer used in the LNA was constructed using EM simulation software (ADS Momentum). The resulting structure is shown in Fig. 3. The transformer has been optimized to have high $|k|$ and high Q-factor inductors [4]. To satisfy equation (1) a turn ratio n of 1.8 has been chosen along with a coupling factor k of -0.76.

The simulated Q-factors of the inductors are higher than 10 at the frequency of interest. Simulated values for L_d and L_s are respectively 137 pH and 42 pH. A patterned shield has been placed underneath the transformers to reduce substrate coupling.

IV. LAYOUT

In Fig. 4 the layout of the core of the LNA is shown. At the left the differential input of the first stage is shown and at the right the differential output of the second stage. The two stages are connected to each other with a DC-blocking capacitor between the output of TF₁ and the input of L_{g2} . All RF interconnects longer than $10 \mu\text{m}$ used were simulated in ADS Momentum and Cadence RC-extraction was used for all other structures. L_{g1} and L_{g2} are approximately 110 pH and 150 pH respectively.

The transistors are indicated in Fig. 4 and are situated underneath the metal lines connecting the transformer structures. Transistor width stage 1 is $35 \mu\text{m}$ and stage 2 is $25 \mu\text{m}$. The vertical lines surrounding the transformers

Fig. 4. Layout of the LNA (330 x 170 μm). Shown are only the top metal layers to clarify the structure. Patterned shields are used underneath the inductors, transformers and coplanar waveguides (not shown). In and output reference planes are indicated by the dashed lines.

are the DC power lines and biasing of the LNA. Coplanar waveguides with shielding have been used to connect the different components to each other. This results in low coupling to the substrate and between components.

The input and output of the LNA are connected to bondpads using CPWs (see Fig. 5). This results in losses and an impedance shift. The resulting source and load impedance of the circuit at the input and output indicated in Fig. 4 is approximately $37 + j10 \Omega$. Open-short-load structures are added to de-embed the circuit. A lot of effort has been put into making the design as symmetrical as possible to reduce common mode.

V. SIMULATION RESULTS

The design consisted of an iterative process between circuit simulations, EM simulations and RC-extraction. After the first circuit simulation a G_t of 13 dB with a NF of 3.1 dB was simulated at 61 GHz. The IIP_3 of the LNA was approximately 2.6 dBm with a 1 dB_c of -11.8 dBm.

After EM-simulation and RC-extraction the performance changed due to the parasitic effects. G_t decreased by 2.3 dB to 10.7 dB and the NF increased by 0.5 dB to 3.6 dB. These simulation results are shown in Fig. 6. The IIP_3 increased to 4 dBm and the 1 dB compression point increased to -9.8 dBm. The simulated G_t variation in the band of interest is smaller than ± 0.15 dB and the 3 dB bandwidth is approximately 50 - 73 GHz which is approximately 37 % of the center frequency at 61 GHz. The simulated power consumption is 35 mW at 1.2 V supply and 0.8 V gate bias.

All simulations were performed using a source impedance of 30Ω , which was chosen as a compromise between NF and G_t , see Fig. 7. This is not equal to the conventional 100Ω for a differential topology. This is because the antenna could be connected directly to the LNA, allowing a different antenna (source) impedance.

Fig. 5. Total LNA chip with bondpads and one de-embedding structure. Size die = 960 x 980 μm , size LNA = 330 x 170 μm .

VI. MEASUREMENTS AND VERIFICATIONS

To verify the behavior of the LNA a number of measurements were performed using a differential measurement setup. DC power consumption is seen to be equal to the simulated value of 35 mW. The NF and s-parameters are verified independently by the Technical University Eindhoven and NXP Research.

A. S-Parameters

The S-parameters were measured using Agilent E8361A PNA. Calibration was verified using WinCal XE software.

After de-embedding the measured G_t with $Z_{src} = 30 \Omega$ is 10 dB at 61 GHz (Fig. 6). The measured in-band deviation is ± 0.25 dB. The s_{12} -parameter is below -47 dB over the entire measured band of 55 - 67 GHz and the group delay is ≈ 20 ps and behaves constant over the band of interest. The differential stability factor (K-factor) stays above 30 in the measured band.

In common mode, the maximum transducer gain is equal to -2 dB resulting in a CMRR of 12 dB. The s_{12} -parameter is below -42 dB, and K-factor stays above 70 in this case.

Fig. 6. Measured and simulated performance (post layout).

TABLE I BENCHMARKING

Reference	Process	Topology	G_t (dB)	NF (dB)	3 dB BW	IIP ₃ (dBm)	V _{dd} (V)	P _{DC} (mW)
[5]	90 nm	3 stage CS	15	4.4	10 %	N/A	1.3	4
[6]	65 nm (SOI)	2 stage casc.	12	8	22 %	N/A	2.2	36
[7]	90 nm	2 stage casc.	14.6	<5.5	25 %	-6.8	1.5	24
[8]	65 nm	2 casc. + 1 CS	22.3 (A _v)	6.1	13 %	N/A	1.2	35
[9] (LNA + mixer, HG)	45 nm	2 stage casc.	26	6	N/A	-12	1.1	23
This work	65 nm	2 stage CS	10	3.8	37 %	4	1.2	35

B. Noise Figure

NF was measured in the band 59.5 – 66 GHz (Fig. 6). Z_{src} during this measurement is equal to $37 + j10 \Omega$, while the input reflection coefficient for the noise source stays below -15 dB. The average measured value in this band is equal to 3.8 dB. To the author's knowledge this is the lowest value found in literature around 60 GHz. NF_{min} of the circuit is found to be 3.7 dB using a load-pull setup in NXP. During this measurement the source impedance for NF_{min} was also verified with the simulated value.

C. Large Signal Measurements

The measured IIP₃ is equal to 5 dBm at 57.5 GHz and 4 dBm at 60 GHz which is in close agreement with the simulation. Measured 1 dB_c is -4.6 dBm and deviates from the simulated value because in simulation a Z_{load} of 100 Ω was used.

VII. BENCHMARKING

The performance of existing 60 GHz LNAs is compared with this work in table 1. The LNAs presented in [5]-[7] are single ended, and [8] has a differential output. It is seen the work presented in this paper shows the lowest NF along with the highest bandwidth. The relative low gain is

Fig. 7. NF and G_t variation as a function of R_{src} . The star in the figure indicates the measurement result without use of the load-pull setup.

because only 2 CS stages are used. The use of feedback results in a high IIP₃.

VIII. CONCLUSION

A 60 GHz differential LNA was realized and measured exhibiting the lowest NF and highest bandwidth to date. High IIP₃ was measured, resulting in a high dynamic range. EM simulations were used to simulate transformers and interconnect and are proven accurate enough. Measurements are in close agreement with simulations.

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REFERENCES

- [1] D. J. Cassan and J. R. Long, "A 1 V Transformer-Feedback Low-Noise-Amplifier for 5 GHz Wireless LAN in 0.18 μ m CMOS" *IEEE J. Solid-State Circuits*, Vol. 38 No. 3 Mar. 2003.
- [2] J. R. Long, "Monolithic Transformers for Silicon RF IC Design" *IEEE J. Solid-State Circuits*, Vol. 35 No. 9, pp 1368-1382, Sep 2000.
- [3] G. Gonzalez, *Microwave Transistor Amplifiers* 2nd edition, Prentice Hall 1997.
- [4] H. M. Cheema, E. Janssen, R. Mahmoudi and A. van Roermund, "Monolithic Transformers for High Frequency Bulk CMOS Circuits" *IEEE SiRF*, Jan. 2009.
- [5] E. Cohen, S. Ravid and D. Ritter, "An Ultra Low Power LNA with 15dB Gain and 4.4 dB NF in 90nm CMOS Process for 60 GHz Phase Array Radio" *IEEE RFIC Symp. Dig.*, pp. 61-64, June 2008.
- [6] A. Siligaris, C. Mounet, B. Reig, P. Vincent and A. Michel, "CMOS SOI Technology for WPAN. Application to 60 GHz LNA" *IEEE ICIDT, Int. Conf. on*, June 2008.
- [7] T. Yao, M. Q. Gordon, K. K. W. Tang, K. H. K. Yau, M. -T. Yang, P. Schvan and S. P. Voinigescu, "Algorithmic Design of CMOS LNAs and PAs for 60-GHz Radio" *IEEE J. of Solid-State Circuits*, pp. 1044 – 1057 May 2007.
- [8] C. Weyers, P. Mayr, J.W. Kunze, U. Langmann, "A 22.3dB Voltage Gain 6.1dB NF 60GHz LNA in 65nm CMOS with Differential Output" *ISSCC Dig. Tech. Papers*, Feb. 2008.
- [9] J. Borremans, K. Raczowski, P. Wambacq, "A Digitally Controlled Compact 57-to-66GHz Front-End in 45nm Digital CMOS" *ISSCC 2009*, Feb. 2009.