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320Gb/s Data Routing in a Monolithic Multistage Semiconductor Optical Amplifier Switching Circuit

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Abstract Record 320Gb/s data serial line rate routing is demonstrated for a multistage integrated optoelectronic switching circuit using semiconductor optical amplifiers. Power penalties of only 2.2dB are achieved in up to four stages of monolithically integrated crossbar switch elements.

Introduction

The increasing demand for high-capacity data transfer in optical networks is driving research into broadband integrated switching systems [1]. Semiconductor optical amplifier (SOA) circuits offer the potential for uncooled, fast reconfigurable and loss-less routing.

Recent test-bed studies for switching networks have focussed on the gating of wavelength multiplexed data using networks of discrete SOAs [2-5]. Tens of wavelength multiplexed 10Gb/s data streams have also been routed using multiple stages of discrete SOA amplifiers with low power penalty [6-7]. At higher line rates, nonlinearities in discrete SOAs have been studied. Cross-gain modulation has been exploited for 100Gb/s line rate wavelength conversion [8]. SOA based nonlinear interferometers have facilitated ultrafast routing [9]. Tight-filtered four-wave-mixing has enabled ultrahigh speed optical time domain demultiplexing [10]. It has however been challenging to replicate ultrahigh speed operation in integrated SOA based sub-systems. Photonic integrated circuits to date have operated at more modest line-rates. 40Gb/s has been demonstrated for multi-wavelength transmitters [11], tuneable wavelength convertors [12], and two input two output switch matrices [13]. The number of stages of active elements in an integrated circuit has been relatively modest. Recent reports of 10Gb/s routing through a monolithically integrated three stage Clos network represents one of the most complex circuits reported to date [14].

In this work, we present a step change in the operating line rate for multi-stage photonic integrated circuits. 320Gb/s line-rate data is routed in a multistage interconnection network, with up to four monolithically cascaded SOA based crossbar switch stages.

Switch Circuit Architecture

A multistage interconnection network is implemented using six monolithically interconnected 2x2 crossbar switch elements.

Four inputs connect to four outputs by means of electronically programmable SOA gates. The circuit design is based upon the N-stage planar architecture proposed by Spanke [15] as shown schematically in Figure 1.

Fig. 1: 4x4 scalable multistage switch architecture superimposed on a 8x8 N-stage planar architecture

The dark grey four input, four output (4x4) layout in figure 1 is superimposed on the larger light grey network to highlight the connection scalability of the architecture. There are sufficient numbers of crossbar stages in the architecture to enable re-arrangeably non-blocking operation. At the physical layer, this is representative of a broad class of multistage interconnection network architectures based on the concatenation of crossbar elements. In the realised circuit, the paths implemented have varying numbers of stages, allowing insight into the role of the number of successive switch elements on signal degradation.

Photonic Integrated Circuit

The circuit has been realised using an active-passive regrown InP epitaxy to enable the integration of high performance SOA gates with low loss waveguide components. This is believed to avoid noise and excessive distortion in the passive photonic wiring. A multi-project wafer with predefined active component placement is used [16], which leads to a requirement for a folded architecture in the fabricated circuit. Active islands are in a column, defining the placement of SOA gates within the crossbar switch elements, as shown

in Fig. 2. These islands comprise five InGaAsP quantum wells which are grown with a gain peak at 1550nm.

Fig. 2: Circuit layout using crossbar switch elements with inset of crossbar detail

Each crossbar switch element comprises four semiconductor optical amplifier gates arranged in a broadcast and select waveguide arrangement [17]. However, the electronic interface is simplified by connecting bar state and cross state electrodes as shown in the inset of Fig. 2.

Two amplifier gates are placed in each active island for enhanced integration density. The waveguides are shown as black lines. The light-shaded gold rectangular regions represent p-side electrodes. The waveguides are manipulated with tight 0.1mm radius deep-etch bends to allow high density wiring and minimum complexity p-metal patterning. This also enables the simplified electronic control. The waveguide crossings and the majority of the straight waveguides are implemented with a shallow ridge waveguide etch for low-loss operation. Adiabatic mode conversion is implemented for the transitions between shallow and deep etched waveguides.

The optical inputs (I0-I3) and optical outputs (O0-O3) are located at the same left facet of the circuit. The optical paths comprise a high number of passive elements as well as the active semiconductor optical amplifier gates within the crossbar elements themselves. Mode filters are implemented using 1×1 multimode interference (MMI) waveguides at the inputs and outputs to promote single mode propagation through the circuit. The splitting operation is performed using symmetric 1×2 multimode interference couplers and combiners.

The control electrodes (labelled a-l) address the amplifier pairs within the active islands. The bar state electrodes address the semiconductor

optical amplifiers pairs which connect the inputs directly to the corresponding outputs. The cross state electrodes enable the exchange of input and output connection. An inadvertent exchange of nodes in the mask design and two electronic short circuits in fabrication restricted connectivity to twenty verified paths through the circuit. The multistage network enables more than one path through the circuit for certain combinations of inputs and outputs. This reduces blocking probabilities when routing arbitrary combinations of inputs to outputs.

The viable paths include the longest and shortest paths through the circuit, and therefore allow a study into the scalability of massively broadband photonic integrated switching circuits.

320Gb/s switch performance

The experimental arrangement for the high line-rate assessment of the photonic integrated circuit is presented in Fig. 3. The optical input signal is generated by optically time division multiplexing delayed copies of the same data sequence.

Fig. 3: Experimental arrangements

A 40Gb/s pulse pattern generator encodes data onto the 40GHz optical pulse train. Three stages of half-pattern-length differential delay Mach-Zehnder interferometers are used to generate the 2^7-1 pseudo random bit sequence at the full line rate of 320Gb/s. The amplified data is transmitted over 58 metres of dispersion managed fibre prior to injection into the circuit under test. The fibre is needed as the switch test-bed and high speed test facilities are located in different laboratories. An in-fibre power of +7dBm, centred at a wavelength of 1559nm, is injected into the switching circuit. Fibre lenses are used with estimated chip to fibre coupling losses of 6.5dB. The output

signal is subsequently retransmitted over a further 58 metres of dispersion managed optical fibre.

Two and four stage routing is assessed by considering routing between input I2 and outputs O1 and O3 as shown in Fig 2. The two stage path requires the on-state operation for the bar electrodes h and i. These are both biased at 85mA. The four stage routing is enabled by biasing electrodes k, i, e and g with currents 75mA, 82mA, 93mA and 100mA respectively. The typical operating voltage is below 2V, corresponding to a worst case power consumption of 0.2W per gate. This may be extrapolated to 1.2W for a fully operational circuit. Four inputs operating at 320Gb/s line-rate would lead to a 0.93 picojoule per bit optoelectronic energy consumption.

The signals at 320Gb/s are studied initially with an optical sampling oscilloscope in the time domain and also with an optical spectrum analyser. Figure 4(i)-(iii) shows the multiplexed signals as eye diagrams. The levelled powers show clear eye openings with comparable amounts of noise.

Fig. 4: Eye diagrams and spectra at 320Gb/s
 (i) input eye diagram
 (ii) two stage output eye diagram
 (iii) four stage output eye diagram
 (iv) input optical spectrum
 (v) two stage output spectrum
 (vi) four stage output spectrum

Optical spectra are shown in figure 4 (iv)-(vi) for the input to the circuit and the two outputs after two and four stages. Spectra are measured after the low noise erbium doped fibre amplifier in the receiver part of the experimental arrangement. The similarity between the optical

spectra indicates minimal levels of nonlinear interaction, for both two and four stages of monolithically concatenated stages of optical amplifier switch stages. An optical attenuator with loss set to 16dB is used in place of the circuit when performing input signal measurements and back to back measurements to ensure comparable noise performance in the receiver amplifier. The losses associated with the switching circuit are dominated by fibre to chip coupling losses of 6.5dB per facet. Additionally the operating currents are deliberately limited to below the round trip gain to avoid oscillation from the uncoated facets. Appropriate coatings would therefore enable further loss compensation.

Bit error rate measurement

The data integrity is assessed by individually selecting and characterising lower line-rate time multiplexed tributaries at the receiver [18]. These are selected by mixing the data signal with a 10GHz phase-locked pulse train in a periodically poled Lithium Niobate crystal. Each of the thirty two 10Gb/s time interleaved tributaries is assessed in turn. Fig. 5 shows the dependence of error rate on the received optical input power for one such tributary. A trend-line is included for the back-to-back conditions.

Fig. 5: Bit error rate for channel 1;
 (x) input: no crossbar switch stages
 (●) output after two crossbar switch stages
 (○) output after four crossbar switch stages

The power penalty at the error rate of 10^{-9} is observed to increase from 0.8dB for two stages up to 2.2dB for four stages. Data points for switch circuit output measurements also show a discernable deviation from the anticipated logarithmic sensitivity response of the receiver. The deviation from the back to back response increases with the number of stages. The degradation may be attributable to a build up of amplified spontaneous emission and signal distortion.

Data integrity is assessed for all the tributary channels of the 320Gb/s signal. To ensure clarity, and verify successful data transmission for the remaining channels, bit error rate is presented for all the channels. At a received power of -16dBm, all channels operate with error rates below 10^{-7} as shown in Fig. 6.

Fig. 6: Error rate performance for all channels.

(x) no crossbar switch elements
 (●) two crossbar switch elements
 (○) four crossbar switch elements

Conclusions

The highest line-rate serial transmission is reported for a multistage photonic integrated switching network. A route to energy efficient signal processing through increasingly sophisticated, high speed, photonic integrated circuits is identified.

This represents a step change in the operating speeds for multi-stage integrated photonics in

general, and optoelectronic switching networks in particular.

References

- 1 I.H. White et al. J. Optical Net, 8, 215-224, 2009.
- 2 N. Sahri et al., OFC, PDP, 2001.
- 3 A. Shacham et al., IEEE J. Lightwave Tech., 23, 10, 3066-3075, 2005.
- 4 A. Shacham et al., OFC, OThF7, 2007.
- 5 Y. Kai et al., ECOC, We2.D.4, 2008.
- 6 J. Crijns et al., IEEE Photon. Technol. Lett., vol. 14, no. 10, pp. 1481-1483, Oct. 2002.
- 7 L. H. Spiekman et al., IEEE Photon. Technol. Lett., vol. 12, no. 8, pp. 1082-1084, Aug. 2000.
- 8 A.D. Ellis et al., Electronics Letters, 34, 20, 1958-1959, 1998
- 9 J.P. Turckiewicz et al., IEEE J Lightwave Technology, 23, 1, 225-235, 2005
- 10 E. Tangdiongga et al., Optics Letters, 32, 835-837, 2007
- 11 R. Nagarajan et al., Elec Lett, 41, 6, 2005.
- 12 S. C. Nicholes et al., IEEE J. Lightwave Tech. Letters, 28, 4, 641-651, 2010.
- 13 E.F. Burmeister and J.E. Bowers, Photonics Technology Letters, 18, 1, 103-105, 2006
- 14 H. Wang et al., ECOC post-deadline 2009
- 15 R. Spanke and V.E. Benes, Applied Optics, 26, 7, 1226-1229, 1987
- 16 JePPIX integration platform www.JePPIX.eu
- 17 A. Albores-Mejia et al. IET Electronics Letters, 2009, 45, 6, 313-314.
- 18 F. Gomez-Agis et al, Elec Lett., July 2010