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11.5 A 2.75mW Wideband Correlation-Based Transceiver for Body-Coupled Communication

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Electronic devices in contact or in close proximity to the human body can use its conductive properties to establish body coupled communication (BCC) between each other. This human centric communication paradigm can be used for wireless body-area networks to reduce the impact of interference on/from RF systems, to avoid the fading effect that the body has on radio systems and to enable power efficient, high data-rate wireless links.

BCC, without skin contact, can be realized via two electrode RX/TX devices capacitively coupled to the human body (Fig. 11.5.1); TX generates a variable electric field while RX senses the variable potential of the body with respect to the environment. The signal transfer along the body has high-pass characteristics with a corner frequency determined by the input impedance of the RX device. A signal attenuation of less than 70dB has been measured between devices placed at various positions on the human body (Fig. 11.5.1, [1,2]). Concerning interference, the body-channel is especially affected by interference below 1MHz while for higher frequencies the observed interference level is below -75dBm (Fig. 11.5.1). However, in the FM band the body starts acting as an antenna and this level may rise to -30dBm [4]. The BCC implementation in [3] used wideband digital TX signals and was very low-power but a cognitive FSK approach [4] was preferred to it due to the afore-mentioned high levels of FM interference above 50MHz.

Here, as in [3], we couple a wideband digital signal to the human body but instead of a 50 Ω input resistance for the RX we use high resistance so that the RX can effectively sense the 1 to 30MHz band, thus avoiding the FM band. Moreover, for further interference suppression, we designed a novel correlation-based RX that attenuates any signal that is poorly correlated to the expected one.

The transceiver architecture is shown in Fig. 11.5.2. Figure 11.5.3 shows functional and measured waveforms. The TX performs Manchester encoding on the digital data-stream so that at least one voltage transition occurs per bit. The RX input stage is a clamped low-noise amplifier (LNA). For each bit-period the electrodes are shorted for a short time (20% duty cycle) and the DC level of the amplifier is restored. For the rest of the period the input resistance is very high and the input signal is amplified. This approach suppresses low frequency interference while the fast voltage transitions from the TX are amplified when they occur during the RX period. The bandwidth of the LNA is limited to 30MHz so that high frequency interference is attenuated. The interference is further suppressed by correlating the output of the LNA with a one-bit *data template* with transitions in the middle of the RX period (Fig. 11.5.3). For this purpose, the received signal is multiplied by -1 in the first half of the period and by +1 in the second half and the result integrated. The computed *data correlation* is maximal for digital-like transitions occurring in the middle of the RX period, while any other signal is strongly suppressed. At the end of the RX period, a comparator detects the polarity of the *data correlation* and regenerates the received bits. For a maximum SIR/SNR of the data reception the *data template* must be synchronized to the incoming voltage transitions. This is achieved with a synchronization loop that correlates the LNA output with a *synchronization template* with two opposite transitions at $\frac{1}{4}$ and $\frac{3}{4}$ of the RX period. The amplitude and polarity of the *phase correlation* at the end of the RX period gives a measure of the phase error between the *data template* and the RX signal. The phase error is then processed by a pulse amplitude modulator (PAM) that generates a pulse with fixed duration and amplitude proportional to its input. The pulse is fed to a loop filter (LF) the output of which controls a VCO that clocks the timing controller so that the phases of the clamp and template signals are adjusted. Since the polarity of the phase correlation depends also on the polarity of the incoming voltage transition (Fig. 11.5.3),

the loop is first stabilized with a predetermined synchronization sequence. Then, in order to track the phase during data reception, the output of the *phase detector* is multiplied by ± 1 according to the polarity of the detected data. For this reason, the bandwidth of LF must be small enough to keep the system stable when the received bits are wrongly detected.

The schematics of LNA, PAM and correlators are shown in Fig. 11.5.4. The LNA is a two-stage amplifier. The first stage is a CMOS inverter, the second is a common source cascoded amplifier with resistive load and degeneration. M1, M4 and M7 implement the clamping functionality. The total LNA gain and bandwidth are 38dB and 30MHz, respectively. The PAM circuit is a differential G_m amplifier with a switched output that creates current pulses during the clamp period. M20-23 select the polarity of the output according to the detected data. The data and phase correlators are folded cascode G_m -C integrators and the multiplication is performed by inverting the current flow at their output by switching M12-15 in accordance with the data or synchronization templates. The RC at the input of the correlator realizes a differential high-pass filter at 1MHz for further suppression of low frequency interference. The VCO is a five-stage ring oscillator with 33 to 53MHz tuning range. Its frequency is divided by five in the timing controller such that the system bit-rate is 8.5Mb/s at the VCO center frequency. LF is passive RC and together with the data comparator is implemented on the test board.

Separate ICs for the RX/TX circuits and the VCO have been designed in 130nm CMOS (Figure 11.5.7). The measured BER of the data correlator path alone against interference is shown in Fig. 11.5.5, where FM interference of 100kHz bandwidth is swept from 250kHz to 100MHz. A BER of less than 10^{-3} is measured for 450 μ V RX signal (68dB attenuated 1.2V digital signal) with -74dBm interference for all frequencies (in compliance to Fig. 11.5.1). The BER is still below 10^{-3} for a -68dBm interference with frequencies below 5MHz and above 20MHz, where higher interference levels are most likely to arise [4]. The highest sensitivity to interference is observed in the 5 to 20MHz band as the correlation time is close to the interference period. Higher interference suppression in this band can be achieved by increasing the correlation time or using error correction codes. Figure 11.5.5 shows that the jitter of the synchronization loop during the synchronization sequence at 8.5Mb/s is 14.8ns without interference and 22.4ns with a -68dBm, 15MHz, interference. An evaluation of different interference scenarios is ongoing. Figure 11.5.6 summarizes the overall performance.

In this work 1.2V digital signals for TX are used, an RX band of 1 to 30MHz is chosen and a new robust BCC architecture is proposed that altogether provide reliable performance in the presence of interference. The measured BER and jitter show that performance competitive to the cognitive FSK approach [4] can be achieved with a simpler implementation. The energy consumption at 8.5Mb/s is 0.32nJ/b, lower than [4] (0.37nJ/b), and the core area is 0.19mm².

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Figure 11.5.1: Body-couple communication concept and body-channel measurements: propagation losses and interference power.

Figure 11.5.2: Architecture of transceiver for body coupled communication.

Figure 11.5.3: Functional and measured waveforms.

Figure 11.5.4: Schematics of the low noise amplifier, pulse amplitude modulator and correlator.

Figure 11.5.5: BER measurements of data detection path alone and jitter measurements during synchronization sequence.

BCC transceiver	TX: capacitively coupled digital signals; RX: input clamping plus correlation based data detection and phase detection		
Process	130 nm CMOS, 6M, 1.2V		
RX Bandwidth	1 to 30MHz		
Input Impedance	>1M Ω during RX period <50 Ω during clamp <1pF input capacitance		
VCO	42.5MHz center frequency 33MHz-53MHz tuning range		
Clamp duty cycle	20%		
Sensitivity@BER=10 ⁻³	350 μ V _{pp}		
Data Rate	Maximum 8.5Mb/s		
Jitter	15ns without interference 22ns with interference		
Power Consumption and Area	TX core	0.6mW	0.009mm ²
	RX core	2.1mW	0.168mm ²
	VCO core	52 μ W	0.009mm ²
	total	2.75mW	0.19mm ²
Energy/bit@8.5Mb/s	0.32nJ/b		

Figure 11.5.6: Summary of design parameters and performance.

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Figure 11.5.7: Micrographs of 1×1mm² RX/TX chip (280×600µm² core area) and 550×650µm² VCO chip (90×100µm² core area).