A 60 GHz Digitally Controlled Phase Shifter in CMOS

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Yikun Yu, Peter Baltus, Arthur van Roermund
Department of Electrical Engineering,
Eindhoven University of Technology
Eindhoven, the Netherlands

Dennis Jeurissen, Anton de Graauw, Edwin van der Heijden, Ralf Pijper
NXP Semiconductors, Research
Eindhoven, the Netherlands

***Abstract*— This paper presents a 60GHz digitally controlled phase shifter in the 65nm CMOS technology. Using a differential varactor-loaded transmission-line architecture, the phase shifter achieves a phase resolution of 22.5°, an average insertion loss of 8.5 to 10.3dB and a return loss of better than 10dB from 55 to 65GHz. The phase shifter occupies an area of only 0.2mm^2. To the knowledge of the authors, this is the first 60GHz digitally controlled phase shifter with a phase resolution of 22.5° in silicon reported to date. It is well suited for a 60GHz phased array.**

I. INTRODUCTION

Recently there is much interest in the 60GHz frequency band for high-speed short-range wireless communication [1] – [7]. The large bandwidth available around 60GHz, with at least 3GHz worldwide overlap (59 to 62GHz), offers the possibility of data transmission at rates of several gigabits per second.

At 60GHz the path loss is high due to the small wavelength thus it is necessary to use a high gain antenna. Phased array [8] is a well-known technique to provide an increased antenna gain and directionality as well as electronic-controlled beam steerability by using multiple antennas. This is highly beneficial to the 60GHz wireless system.

Phase shifters are essential components in a phased array to adjust the phase of each antenna path and steer the beam. As shown in Figure 1, by placing the phase shifters after the LNAs, the received signals from the multiple antennas are amplified, phase shifted and combined before frequency down conversion. The RF beam forming architecture does not require any additional mixers, LO signals, analog-to-digital or digital-to-analog converters as compared to a standard single-antenna transceiver. Furthermore, because of the spatial filtering of interferers, the dynamic range and therefore the power dissipation of the mixers and subsequent stages can be reduced. Thus RF beam forming has the advantage of low cost and low power. The main challenge is to design a low-loss broadband and high-resolution phase shifter with a phase control range of 360° at 60GHz [6], [7] especially in a low cost CMOS technology.

This work presents the design of a 60GHz digitally controlled phase shifter in the 65nm CMOS technology. Using a differential varactor-loaded transmission-line architecture, the phase shifter has a phase resolution of 22.5°, an average insertion loss of 8.5 to 10.3dB and a return loss of better than 10dB from 55 to 65GHz. To the knowledge of the authors, this is the first 60GHz digitally controlled phase shifter with a phase resolution of 22.5° in silicon reported to date.

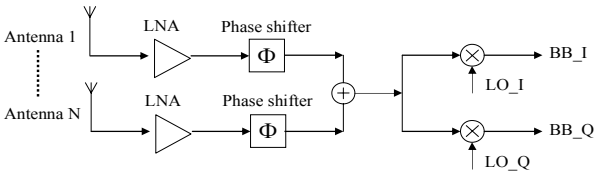

Figure 1. An RF beam forming receiver in which the received signals from multi antennas are amplified, phase shifted and combined before down conversion.

II. DESIGN OF PHASE SHIFTER

A phase shifter with a phase control range of 360° and a phase resolution of 22.5° is the typical requirement in phased array systems [8]. Phase shifters can be designed by tuning the lumped element equivalent of a transmission line.

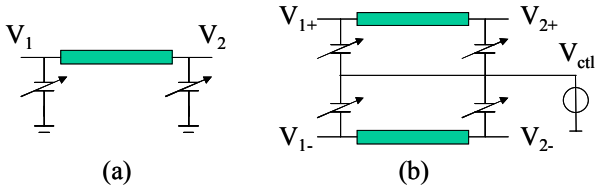

Figure 2. A schematic of (a) a conventional varactor-loaded transmission-line phase shifter; (b) a proposed differential phase shifter consisting of a differential transmission line loaded with a differential varactor at each side.

Figure 2(a) shows a conventional varactor-loaded transmission-line phase shifter [9], [17]. It consists of a transmission line loaded with a varactor at each side. The varactor capacitance can be varied by the DC control voltage and creates a perturbation in the insertion phase and characteristic impedance of the π section.

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In this work, a differential varactor-loaded transmission-line phase shifter (Figure 2(b)) is used. The phase shifter consists of a differential transmission line loaded with and a differential MOS varactor at each side. The cross-sectional view of a differential MOS varactor is shown in Figure 3 [18]. The top and bottom plates of the varactor are formed by the poly gates and n-well. The differential gate terminals of the varactor are connected to the transmission line and the n-well of the varactor is connected to the DC control voltage.

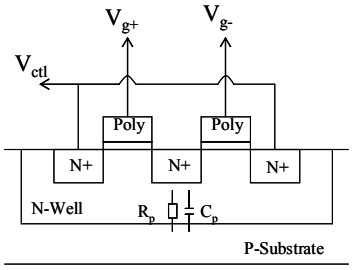

Figure 3. A cross-sectional view of a differential poly/n-well MOS varactor

One advantage of using a differential phase shifter is that the differential path could be swapped to provide a discrete phase step of 180°. Thus the differential phase shifter is only required to achieve a phase control range of another 180°.

Another advantage of using a differential phase shifter is that a differential varactor has better capacitance-control range and better quality factor as compared to a single-ended varactor. This is because that operating in a differential mode, the n-well node of a varactor is a virtual ground and not sensitive to any parasitics. In contrast, it is difficult to create a low-impedance broadband AC ground at the n-well node of a single-ended varactor especially at 60GHz. As a result, a differential phase shifter has better performance as compared to a conventional single-ended phase shifter.

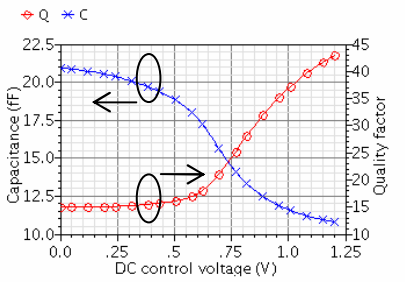

Figure 4. The capacitance and quality factor of a differential MOS varactor at 60GHz in simulation.

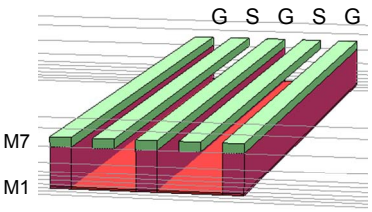

Figure 5. A differential coplanar transmission line with solid metal-1 ground underneath the metal-7 signal lines.

The transmission line in Figure 2 could be replaced by distributed low-pass structures consisting of spiral inductors and capacitors [9]. The advantage of using a transmission line instead of a spiral inductor is that a transmission line is easy to model, scalable and has better isolation between lines.

The phase control range of a phase shifter depends on the capacitance-control ratio of the varactor and the length and characteristic impedance of the transmission line. By using a high-impedance transmission line, a large phase control range can be achieved. A high-impedance transmission line, however, usually has a higher loss. As a trade-off between the phase-control range, insertion loss and return loss, the differential impedance of the transmission line is chosen to be equal to the system impedance (100Ω).

Figure 4 shows the performance of a differential MOS varactor at 60GHz in simulation. The DC bias voltages of the gates are set to 0.6V and the DC control voltage at the n-well is swept from 0 to 1.2V. The CV curve is almost flat when the control voltage is around 0 or 1.2V. By setting the control voltage digitally to either 0 or 1.2V, the varactor has a capacitance-control ratio of about 2 and a quality factor of more than 15 at 60GHz.

The transmission line used in this work is shown in Figure 5. It's a differential coplanar transmission line in ground-signal-ground-signal-ground (GSGSG) configuration with solid metal-1 ground underneath the signal lines. The signal lines are using metal-7 and the ground lines are using metal-7 down to metal-1 by vias. Here the width of the signal lines, ground lines and the gaps between them are all 4μm. The ground walls around the signal lines highly improve the isolation between lines, thus the transmission lines can be closely placed together in the layout to save area.

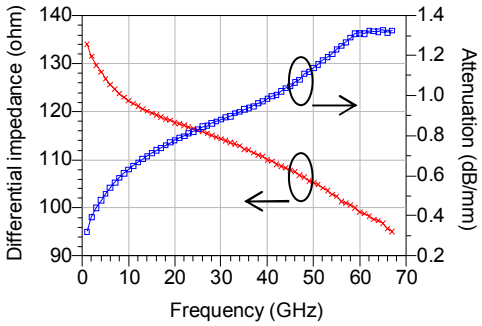

Figure 6. Measured differential impedance and attenuation of the transmission line.

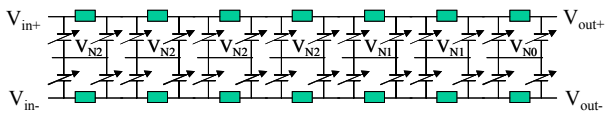

Figure 7. A schematic of 60GHz phase shifter, in which seven π sections are cascaded to realize a phase control range of 157.5°.

Figure 6 shows the measurement results of the transmission line. The measurement procedure is similar to

that in [10]. The transmission line has a differential impedance of 100Ω and an attenuation of 1.3dB/mm at 60GHz.

Due to the limited capacitance-control ratio of a MOS varactor, the phase control range of each section is designed to be about 22.5° at 60GHz. The length of each transmission line is about 0.16 wavelengths at 60GHz. The insertion phase of each section is designed to be about either -101° or -79° when the control voltage is low or high respectively, in order to keep the impedance of each section relatively constant.

Seven π-sections are cascaded to achieve a total phase control range of 157.5° as shown in Figure 7. The DC bias voltages of the transmission lines are 0.6V. There are 8 different phase states by setting the control voltage of a certain number of π-sections to logic low or high according to 3 digital control bits (V_{N2}, V_{N1} and V_{N0} in Figure 7).

The phase shifter is implemented in the 65nm CMOS technology and occupies an active area of 0.2mm^2. Figure 8 shows the photograph of the phase shifter. Open and short de-embedding structures are used to correct for the bondpad and ESD parasitics. The total chip area is 1mm^2.

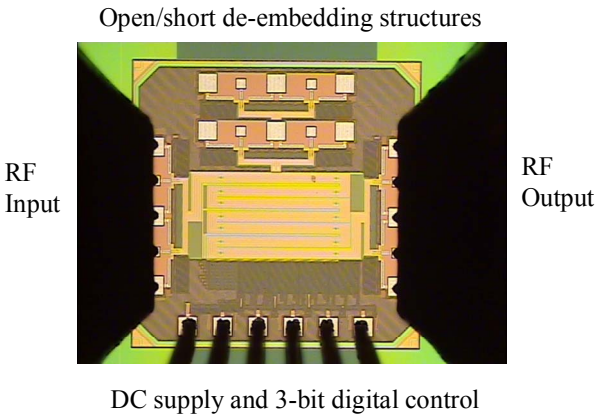

Figure 8. The photograph of the phase shifter including open and short de-embedding structures.

III. Measurement Results

Four-port on-wafer S-parameter measurements were conducted in a frequency range extending from 100MHz up to 67GHz using an Agilent E8361A combined with an N4421B H67 test-set together providing four-port measurement capability. The HP4155B parameter analyzer combined with a 41501B expander box was used for biasing of the test structures. Furthermore a 4-port probe-tip calibration was performed to place the measurement reference plane at the tips of the dual signal RF probes and finally on-wafer open and short structures were available for de-embedding purposes.

Two-port differential-mode S-parameters are derived from the four-port S-parameters [11]. The bondpad and ESD parasitics are de-embedded by the open and short de-embedding structures.

Figure 9 shows the insertion phase of the 8 different phase states over frequency. At 60GHz the phase resolution is 22° and the phase control range is 156°. The RMS phase error of the 8 phase states is less than 9.2°, as compared to an ideal phase shifter with a phase resolution of 22.5°, for all the frequencies from 50 to 65GHz.

Figure 10 shows the relative phase shift of the 8 different phase states referred to state 000 (N_2=N_1=N_0=0). The phase shifter provides an almost linear phase shift from 1 to 67GHz.

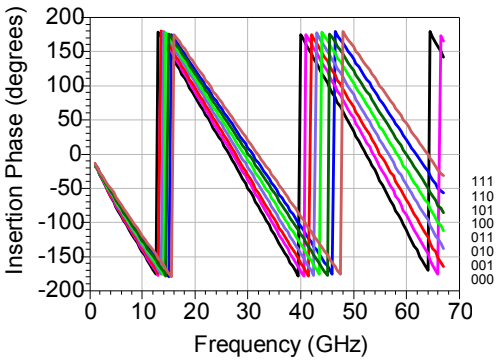

Figure 9. The insertion phase of 8 different phase states over frequency.

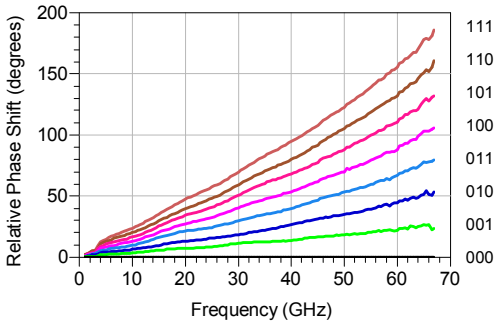

Figure 10. The relative phase shift of 8 different phase states over frequency.

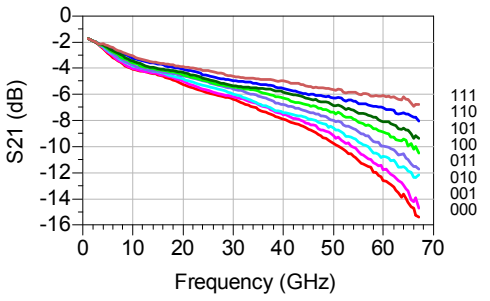

Figure 11. The insertion loss of 8 different phase states over frequency.

Figure 11 shows the insertion loss of the 8 different phase states over frequency. The insertion loss is 9.4±3.1dB over the 8 phase states at 60GHz. This loss variation is due to the low Q and large capacitance of a varactor when the DC control voltage is low (as shown in Figure 4). The average insertion loss is between 8.5dB and 10.3dB from 55 to 65GHz, and is between 1.7 to 11dB from 1 to 67GHz. Variable gain amplifiers could be used in each RF path to equalize the loss variation of the phase shifters and avoid array pattern degradation.

Figure 12 shows the input and output return loss of the phase shifter, which are better than 10dB from 55 to 65GHz and better than 9dB from 1 to 67GHz.

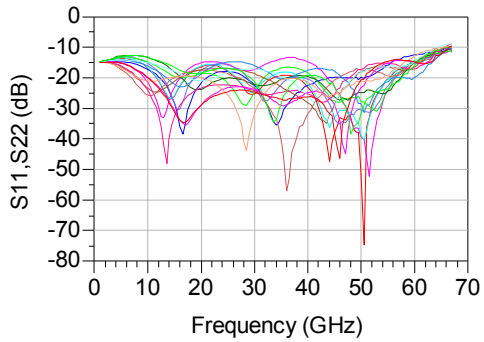

Figure 12. The return loss of 8 different phase states over frequency.

In Table 1, the key results of this work are summarized and compared with other passive [9], [12], [15] and active [13], [14], [16] phase shifters in compound semiconductors and silicon. The phase shifter presented in this work has a low insertion loss (among passive phase shifters) and a high phase resolution at 60GHz.

TABLE1. BENCHMARK OF PHASE SHIFTERS

Reference	Frequency (GHz)	Phase range / Resolution (degrees)	Gain (dB)	DC power (mW)	Technology
This work	60	180 diff./22.5	-9.4	Passive ~0	65nm CMOS
Ellinger [9]	5.5	360/analog	-3.9	Passive ~0	0.6µm GaAs MESFET
Kang [12]	12	360/11.25	-14.5	Passive ~0	0.18µm CMOS
Maruhashi [15]	34	360/22.5	-13.1	Passive ~0	0.15µm GaAs HJFET
Kang [13]	12	360/22.5	3.5	Active 26.6	0.18µm CMOS
Koh [14]	26	360/22.5	-3	Active 12	0.13µm CMOS
MIN [16]	34	360/22.5	1	Active 5.4	0.12µm SiGe BiCMOS

IV. CONCLUSION

The phased array technique is highly beneficial to 60GHz wireless communication. Phase shifters are essential components in a phased array. This work presents the design of a 60GHz digitally controlled phase shifter in the 65nm CMOS technology. Using a differential varactor-loaded transmission-line architecture, the phase shifter has a phase resolution of 22.5°, an average insertion loss of between 8.5 to 10.3dB and a return loss of better than 10dB from 55 to 65GHz. The phase shifter occupies an area of only 0.2mm^2. Thanks to its low cost, simple design, low insertion loss and high phase resolution at 60GHz, the phase shifter is well suited for a 60GHz phased array.

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