On the design and implementation of a wafer yield editor

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identical terminals in horizontal and vertical directions necessary tracks and vias are inserted and the final solution is obtained. The final routing is shown in Fig. 9, which minimizes the number of vias ($= 13$).

Corollary 1: The complexity of the via-minimization algorithms in a four-way switch-box routing problem is $O(N \log N)$.

Proof: Follows immediately from Theorem 2.

IV. CONCLUSION

We describe a unified graph-theoretic approach for minimizing the number of via holes for a generalized two-layer routing problem where terminals are freely movable without changing the relative order. The algorithm is equally applicable to two-row channel routing and to three- and four-sided switch-box routing models.

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On the Design and Implementation of a Wafer Yield Editor

JOSE PINEDA DE GYVEZ AND J. A. G. JESS

Abstract—An interactive environment for the analysis of yield information required on modern integrated circuit manufacturing lines is presented. The system estimates wafer yields and wafer yield variations, quantifies regional yield variations within wafers, identifies clusters in wafers and or in lots, and is also able to predict wafer yields via simple simulation tools. An analysis approach based on site yields makes the system also independent of the product and of the technology. The analysis technique investigates the effect of both correlated

and uncorrelated sources of yield loss. The statistical information obtained can be used to study the changes in the technological process. Graphical displays in the form of wafer maps are used to represent the spatial distribution of dice in the wafer. Facilities such as radial and angular distribution analyses, among others, are provided to examine data, and hypothetical wafer maps are created to visualize and predict simulated wafer yields.

I. INTRODUCTION

The yield associated with individual process steps like etching, metallization, etc., as well as the spatial distribution of random and systematic sources of yield loss [1]-[3], [19] have a different impact on each of the IC's of a wafer, such that yield variations and even sometimes severe product yield losses arise.

Such yield variations can be investigated by examining batches of wafers in order to correlate non-functional circuits and to find their contributions to yield loss. Interaction with these yield variations can be aided by analyzing the wafer maps where functional, nonfunctional and partially functional regions can easily be observed. Considering this, a tool is necessary to manage the data coming from the manufacturing lines and to condense it in useful information for whom yield prediction and estimation are very important issues for the IC design and process development.

Such a CAD tool should be able to analyze the yield variations, to quantify them, and to allow the interpretation of data in several forms as to draw conclusions about the problems. Furthermore, it should not only analyze data but also simulate the effects of density variations in a single wafer and between wafers, as to be able to predict yield. For such a system, *technology independency* and *product independency* are two mandatory properties. The former one concerns the analysis of data coming from GaAs, MOS, BI-POLAR, etc., technologies, and, for any given wafer diameter and dice configuration. The latter property means that the system should interpret data such as distribution of defects, process parameters, test structures, memories, etc.

This paper describes the *Wafer Yield Editor ALWAYS* (Analyzer of Wafer Yields). ALWAYS is a user friendly interactive environment created to be used as an integral and systematic tool for wafer yield analysis. The system provides means for estimation and prediction of yield. It uses graphical representations in the form of wafer maps, curves, and charts for user interface. Facilities such as to create wafer frames and dice of different dimensions, as well as several miscellaneous tools such as hardcopy, overlapping of extracted wafer maps, etc., are also provided.

II. DATABASE AND WAFER CHARACTERISTICS DESCRIPTION

The starting data are a set of wafer maps of working and non-working dice of individual wafers produced from the process of interest.

A set of wafers is defined as a *lot* and a set of *lots* as a *project*. This classification allows to have the information in a hierarchical style. Hence, the database description follows a tree structure where the parent is the product itself, the children represent each one of the lots of the product, and the grandchildren represent the individual wafers for each lot. Each individual wafer contains the input data of the yield editor, and it consists of all the die positions and their status, ON, or OFF.

Since product independency is one property of the editor, the data supplied may concern linewidths, resistivities, oxide thicknesses, etc., or, defect distributions, distribution of opens and shorts in different layers, distribution of good and bad chips, etc. This flexibility allows to set the status of each die according to the convenience of the analysis to be performed. For instance, consider that a project consists of a memory chip where the status of each die can be set as ON for functional chips and as OFF for defective ones. In this case any analysis performed will reveal the yield of the memory chip. On the other hand, if the project represents a

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defect monitor where a die is set ON when the monitor detects defects and OFF when it does not, then any analysis will project the places where the defects occurred and the yield computed will correspond to the yield of the failing monitors. In any case, the use of process windows [4] is a good technique to accept or to reject the functionality of the project in question. Besides, it leaves the user with the freedom of determining the ON or OFF status of the die according to the range of parameters prevailing in the manufacturing line.

Input data do not have to represent the absolute die coordinates in the wafer. Assume that the test monitor detects defects of several different sizes. Instead of providing the monitor coordinates, a die partitioning can be performed such that each subdie represents a defect size. Then the status of each subdie can be given now as ON for a defect present and as OFF for its absence, and furthermore, the analyses will project the occurrences of defects classified by their sizes.

Dice are placed on an imaginary square which represents the photolithographic *mask* of the fabrication process. The wafer size, die shape, and mask size are interactively controlled. The geometrical median of the mask is used as a reference point to center the wafer frame. For simplicity the representation of the flat side of the wafer is approximated to $0.04 R$ [5], where R is the wafer radius, and it is always oriented towards the bottom side of the mask.

Fixing the wafer's center with the center of the mask does not always achieve the maximum number of dice in the wafer, or simply it does not look like the "real life" wafer. However, the availability of a mask with all the dice allows to "move" the wafer frame in order to obtain the "real life" dice configuration. Thus the wafer can be shifted up, down, left or right along the mask at user's will.

In addition to the normal dice it is also possible to specify *dead dice*. The locations of these dice are considered *dead* and are not taken in account for analyses or simulations. This feature allows to activate and deactivate specific regions in the wafer, making it possible to analyze let us say half of a wafer, or to eliminate a single row of dice, etc. For example, in production wafers the dead dice may represent test sites.

III. THE MAP AND DISTRIBUTION ANALYSES

The analysis is based on cumulative results by doing the boolean AND on a set of wafers. The result is a composite wafer map which contains the cumulative yield by site location as shown in Fig. 1. This methodology and its benefits were already reported for a specific application in [6] and for a spatial analysis in [7]. We extend it by considering not only the individual wafer variations but also by taking in account the lot and project variations of the project.

This kind of wafer convolution also allows consideration of the mean and standard deviations between lots and between product, a well-known problem [8]. Furthermore, the methodology exploits the fact that wafers have statistically dependent yield patterns for certain processing steps, and also that wafer yields are usually correlated when processed in the same lot or under similar conditions.

The within wafer yield variations are inspected by using the concept of *site yield*. A site yield shows how many times in the complete set of wafers involved in the analysis a particular die accomplished the function. For instance, if our analysis consists of a lot of ten wafers and one die in the composite wafer was only five times ON, then its functional site yield is of 50 percent. If the die represents a functional chip it means that only five out of ten chips were good in that particular position. If the die represents a defect it means that five wafers have defects in the same location. Thus given a die τ we can write its site yield as

$$Y_{\text{site}}(\tau) = \frac{F_{\text{site}}(\tau)}{N_A} \quad (1)$$

where F_{site} is the *site frequency*, in other words, the number of times that the die was projected, and N_A is the number of wafers involved in the analysis.

Fig. 1. The Boolean AND of wafers.

Fig. 2. Graph representing the dice interconnection in a wafer map.

ALWAYS can execute two kinds of analyses on data. One is called the *map analysis* and the other the *distribution analysis*. The map analysis displays the composite wafer map with the projected dice that accomplished the function, and its purpose is mainly intended to see the correlated spatial behavior of the input data. The distribution analysis, on the other hand, quantifies the behavior of the input data by showing the curves of different types of distributions of the final composite wafer map.

Let $H = I \times J$ be a two-dimensional array of size $n \times n$ with the abscissa represented by the set of reals $I = \{0, 1, \dots, n\}$ and the ordinates by $J = \{0, 1, \dots, n\}$.

Let $x(v)$ and $y(v)$ denote the x and y coordinates of the center of a die v , respectively, and let us represent the horizontal and vertical magnitudes of every die by a and b , respectively. The wafer map can be seen as a graph $G = (V, E)$ (see Fig. 2) with V the set of dice contained in the composite wafer and E the set of edges relating any two consecutive dice, expressed as

$$V = \{v | x(v) \in I \wedge y(v) \in J \wedge \text{the four corners of } v \text{ within the wafer}\}$$

$$E = \{(v, w) | v \in V \wedge w \in V \wedge (|x(v) - x(w)| \leq a \wedge |y(v) - y(w)| \leq b)\}.$$

The map analyses are explained next. All the examples are referred to the history map shown in Fig. 3(d).

1) *Functional Map*: The functional map shows all the die locations which were ON all the time in the whole set of wafers selected for the analysis. We can express this formally as the set F

Fig. 3. (a) Zero map. (b) High-range map for site yield ≥ 60 percent. (c) Low-range map for site yield ≤ 40 percent. (d) History map. (e) Information map. (f) Cluster map for site yield = 50 percent and $N \geq 3$.

whose elements are the dice π such that their site yield is equal to 1

$$\Gamma = \{ \pi | \pi \in V \wedge Y_{\text{site}}(\pi) = 1 \}.$$

This map is useful to determine which are the dice that systematically contribute to the project yield.

2) *Zero Map*: The zero map shows all the die locations which were OFF all the time in the whole set of wafers selected for the analysis (see Fig. 3(a)). Thus the map is defined as the set

$$\Omega = \{ \pi | \pi \in V \wedge Y_{\text{site}}(\pi) = 0 \}.$$

The analysis projects immediately which are the dice detractors and systematic contributors to yield loss.

3) *Up-Range Map*: This map shows the dice, in the composite wafer, that have a specific site yield, or above it (see Fig. 3(b)). The specific site yield is a user entry. The map can be expressed as the next set

$$\Phi(y) = \{ \pi | \pi \in V \wedge Y_{\text{site}}(\pi) \geq y \}.$$

The map is useful to investigate the general behavior of a particular process step along the whole lot of wafers by finding out which are the most correlated regions.

4) *Low-Range Map*: This map is similar to the previous one, only that it displays the site locations with the specific site yield, or below it (see Fig. 3(c)), and can be represented by the set

$$\Lambda(y) = \{ \pi | \pi \in V \wedge Y_{\text{site}}(\pi) \leq y \}.$$

The results can be interpreted as a map of the least correlated sectors in the wafers involved in the analysis.

5) *History Map*: This analysis shows numerically the site frequency of each die location (see Fig. 3(d)). This map is simply the set V . The numerical information is useful to quantify each site yield of the composite wafer in order to evaluate the regional wafer variations.

6) *Informative Map*: This is a contour informative map, it displays, in a color code fashion, the dice with the average, and the above and below average, site frequency, (see Fig. 3(e)). Zero frequency locations are distinguished from the rest of the dice. The analysis allows visualization of the uniformity of the distribution of the input data in question.

7) *Cluster Map*: We define a cluster as a group of n or more contiguous dice that have the same site yield ξ (see Fig. 3(f)). Therefore, clustered elements can be in the horizontal, vertical or even diagonal directions. In general, a cluster can be defined as the maximal connected induced subgraph $H(U, E_U) \subseteq G$ [22], where

$$U = \{ \pi | Y_{\text{site}}(\pi) = \xi \}$$

$$E_U = \{ (v, w) \in E | v \in U \wedge w \in U \}.$$

From our definition a cluster exists only if $|U| \geq n$. Hence, the cluster map is the union of all the $H(U, E_U)$ with $|U| \geq n$.

Let us turn now to the distribution analysis.

8) *Radial Distribution*: This distribution projects the different yield variations found in several concentric regions of the wafer starting from the center to one of the extremes [9]–[11]. A threshold yield ξ representing the minimum site yield is searched in each die. This user entry allows to project the different regional deviations from a specific site yield used as a mark of reference (see Fig. 4(a)).

Before the distribution is formulated it is necessary to define the set N_{r_1, r_2} as the set of dice that lie on the concentric region of radius (r_1, r_2) with origin at the center of the wafer, by

$$N_{r_1, r_2} = \{ \pi | \pi \in V \wedge r_1^2 \leq x(\pi)^2 + y(\pi)^2 \leq r_2^2 \}$$

and also the set $Y_\xi \subseteq N_{r_1, r_2}$ which is the set of those dice that have a site yield bigger or equal to the specified

$$Y_\xi = \{ \kappa | \kappa \in N_{r_1, r_2} \wedge Y_{\text{site}}(\kappa) \geq \xi \}.$$

Fig. 4. Distributions shown are extracted from the wafer map in Fig. 3(d). (a) Radial distribution for two threshold yields. (b) Yield versus area distribution for two different threshold yields.

Now the radial distribution is presented as

$$Y_R(\xi, r_1, r_2) = \frac{\sum_{n \in Y_\xi} Y_{\text{site}}(n)}{|N_{r_1, r_2}|}.$$

9) *Angular Distribution*: Clustering [15], [16] can be studied in more detail with the previous distribution complemented by a distribution that finds angularly the yield [12]. This distribution projects the yield contained in circle segments of the wafer. As with the radial distribution the threshold yield ξ represents the minimum site yield which is searched in each die. In this case different angular deviations from a given site yield used as a mark of reference are projected.

The set of dice N_θ that lie on the circle segment of angle θ and origin the center of the wafer is represented by

$$N_\theta = \{ \pi | \pi \in V \wedge \frac{y(\pi)}{x(\pi)} = \tan \theta \}$$

and the subset $Y_\xi \subseteq N_\theta$ the set of dice with site yield bigger or equal to ξ as

$$Y_\xi = \{ \kappa | \kappa \in N_\theta \wedge Y_{\text{site}}(\kappa) \geq \xi \}.$$

The distribution is evaluated as

$$Y_\theta(\xi, \theta) = \frac{\sum_{n \in Y_\xi} Y_{\text{site}}(n)}{|N_\theta|}.$$

10) *Site Yield Frequency Distribution*: This distribution shows the number of times that the different site yields appeared in the

wafer. For instance, 5 dice with site yield of 0.3, 20 dice with site yield of 0.7, etc.

11) *Cumulative Frequency Distribution*: This distribution projects the probability of occurrence of the different site frequencies found in the composite wafer. This is an easy way to infer the process correlation among all the wafers. [13], [14], [17].

12) *Yield versus Area Distribution*: This distribution shows the effective area utilization of the wafer [18] (see Fig. 4(b)). The distribution is "extracted" from the composite map by means of a multiple-die analysis method. Again, a threshold yield is searched in order to predict the area utilization for yields above or equal to the specified value. To achieve this, each super-die's site yield is computed as the average of the individual site yields of every die with nominal area contained in the boundaries of the super-die. Then the yield of the new super-die map is evaluated as if it were a high-range map.

IV. THE WAFER YIELD STATISTICS

The wafer maps standing alone are a good means to display the distribution of the input data on wafers. Although they are a good tool they are usually not enough. One is generally interested in quantifying the results in order to make conclusions of the analysis, i.e., to know the yield of ON dice, the variations of ON dice between wafers, etc.

The first information is the yield of the map, i.e., the yield of ON dice, the yield of OFF dice, etc.

This yield is evaluated as

$$Y_F = \frac{N_f}{N_c}$$

where N_f is the number of dice that accomplished the function and N_c is the total number of dice of the composite wafer, excluding the dead dice. For each map, information about the mean yield per lot, and per project, with their corresponding variances is provided. Each partial yield is taken as an independent random variable and altogether constitute a random sample for whose mean $\bar{x}_p$ and variance s_p^2 are calculated. These two quantities estimate the conformance of the map per lot and per project. Furthermore, a 95-percent degree of confidence of the mean yield value is evaluated. This means that if we had more lots, or projects, we could assert with $(1 - \alpha)$ 100-percent degree of confidence that the true average lot yield is between the two boundaries.

Since the methodology exploits correlation of wafers, an expected site frequency of the dice μ_w and its standard deviation σ_w is also provided for each map. This expected value is the mean of the distribution of dice that accomplished a specific function.

The statistics mentioned so far are for correlated functions. The history map has a set of uncorrelated statistics. The yield is evaluated as

$$Y_U = \frac{N_g}{N_i}$$

where N_g is the total number of dice that were ON during the analysis, and N_i represents the total number of dice in the analysis. The variation among wafers, among lots, and among projects is inspected by evaluating the yield of ON dice in each case.

Cluster statistics are considered in a similar way. First we find the number of clusters C and their total number of elements G in the composite wafer. Then the mean number of clusters $\bar{x}_c$ and the mean number of clustered elements $\bar{x}_G$, with their respective variances s_c^2 , s_G^2 , per lot and per project are evaluated.

V. SIMULATIONS

ALWAYS provides two kinds of simulations. The first kind simulates the yield versus area. Such a simulation allows to predict the efficiency in area utilization of the wafer. The second kind concerns the creation of wafer maps, and it is mainly intended to discover the tendency of defect and yield distributions within and between wafers, given the conditions of the manufacturing environment.

The yield versus area is evaluated using a distribution of the normalized frequency of occurrence of the number of defects per chip. The yield equation employed for the simulation is the one presented in [14] expressed as

$$Y = \left[\left(AD \left(\frac{\sigma}{\mu} \right)^2 + 1 \right) \right]^{- (\mu/\sigma)^2} \quad (3)$$

where A is the area of the die, D is the average defect density, and σ/μ the coefficient of the defect density variation.

The wafer map simulation is only for one lot. The number of wafers in the lot is a user entry, and the characteristics of the wafer correspond to the prototype wafer. The input data to simulate wafer maps consists of the relative radial distribution of site yields, expressed as follows:

$$Y_R = \frac{N_g}{N_R} \quad (4)$$

where N_g is the number of ON dice at radius R and N_R is the total number of dice at radius R . It is clear that the within wafer variations are considered with a radial distribution. Now, in order to consider the variations between wafers, one has to bear in mind that some wafers exhibit a higher radial yield and some a lower. Therefore, the input data consist in fact of two radial distributions, one for the upper bound and the other for the lower bound. The regional variation of the simulated wafers lies between these two limits as

$$\delta = Y_{R_u} - Y_{R_l} \quad (5)$$

where Y_{R_u} is the upper radial yield and Y_{R_l} is the lower radial yield, both at radius R . Hence, the simulation is left to the task of generating a random number of ON dice for whose relative radial yield at wafer radius R lies between these two boundaries.

VI. YIELD DIAGNOSIS THROUGH ALWAYS

The aim of this section is to give an example of the usage of a wafer yield editor for yield loss diagnosis. We outline a series of steps based on the framework presented in [4] but emphasizing the tools existing in ALWAYS. The proposed framework tries to cover all the categories of defect and process instabilities. Its methodology uses a hierarchical classification of the reasons of yield losses allowing the user to build yield diagnosis procedures that are general and capable of solving problems. An overview of the basic categories of processing errors and disturbances that cause parametric fluctuations and functional errors is also covered in the same paper.

Disturbances of the process of interest manifest themselves as local and global disturbances. The former ones are likely to result in a functional failure of one die or a group of dice. The latter ones affect entire areas of the wafer.

There are two reasons for yield losses: *systematic* and *random*. If the yield is always low and some specific dice always fail then the reason for yield loss is systematic, otherwise it is random. The history map provides the uncorrelated yield of the whole set of wafers in analysis. The zero map provides information about the dice that always fail, thus we can postulate the first step as the following.

Step 1: If the yield of the *history* map is **low** and the yield of the *zero* map is **high** then the yield loss is *systematic*.

If the yield is zero on some of the wafers then *gross manufacturing errors* can be assumed. On the other hand, if the yield is not zero but it is low on all of the wafers then the errors are due to *local* or *global* reasons.

Step 2: If the yield of the *functional* map of some of the wafers is **zero** then the reason is a *gross manufacturing error*. If the yield of the *low-range* map is **high** for certain low yield threshold then the reason is due to *local* or *global* disturbances.

Local disturbances manifest themselves in the form of functional failures, while global disturbances cause either malfunctions on all IC elements or shiftings in the IC performance. Hence, if the majority of the failing dice of the project are functionally incorrect

but only a few of the tests fail then the reason is *local* otherwise it is *global*.

Step 3: If the yield of the *up-range map* of the project is **lower** than the yield of the *up-range map* of the test monitors, both for the same high yield threshold value, then the disturbances are *local*.

The reasons for local yield losses are classified as *random* when the placement of defects does not have any regularity, as *clustered* when there are groups of defects in certain regions with randomly located centers, as *patterned* when the proportion of defects is high in some areas of the wafer, and, as *repeating* when defects occur always in the same location. It is likely that the product dice will present the same behavior as the defects.

Step 4: The *low-range map* shows the *random* type of local yield losses, the *cluster map* shows the *cluster* type, the *informative map* shows the *pattern* type, and the *zero map* shows the *repeating* type.

Global disturbances can be classified as *design-process miscentering* and as *excessive fluctuations*. The former is manifested when the majority of the dice have a performance outside an acceptability region. The latter one is manifested when the performance has a very wide spread, which also results in a low number of dice located inside of the acceptability region. These kind of evaluations are carried on through performance measurements.

Step 5: If the *frequency distribution* shows a **spread** of the number of dice along the different site yields then the disturbances are of the kind of *excessive fluctuations*. If the *cumulative distribution* has a **steep slope** at a low site frequency then a *design-process miscentering* is present.

It is also interesting to conclude about the *correlation* of wafers and *yield area* estimation for the current trends of the process.

Step 6: Find the *radial* and *angular yield maps* for a range of site yields, for the whole set of wafers. Each one of the curves displays information about the correlated wafer area utilization. Extract the *yield versus area* curve of the composite wafer to estimate the efficiency in area utilization.

VII. CONCLUSIONS

We presented a simple, yet complete, package for wafer yield analysis. As in every beginning, things are not often easy. When there were no layout editors, people used to do their designs by hand, or by creating isolated programs to ease this enormous task. Then suddenly the first layout editors appeared and became more and more popular up to the point where today it is an indispensable and easy to obtain tool. Similarly, the idea of the *Wafer Yield Editor* demonstrates that it is easy to build a system specifically for yield analysis. Sophisticated CAM tools [20], [21] that provide statistical process and quality control, and, analysis and simulation of yield management are also available. However, these systems are oriented to automate the wafer processing in silicon foundries and their scope differs from yield analysis.

The most significant features of ALWAYS are summarized as follows.

1) The concept of site yields makes the system independent of the product, and/or of the technology. The interpretation of the results is according to the kind of data supplied to the editor.

2) A simple database structure allows to examine projects, lots, and individual wafers. By using process windows the user can determine whether the input information of the die is ON or OFF.

3) Full flexibility to edit the characteristics of the prototype wafer. Not only the size of the dice or of the wafer can be modified, but also it is possible to activate and deactivate regions within the wafer for analysis or simulation conveniences.

4) The analysis technique allows the estimation of the contributions of both correlated and uncorrelated detractors to the total yield. The statistical information obtained from the analysis can be used to study the effect of process changes on the product yield.

5) Simple simulation tools allow not only to estimate but also to predict the wafer yields and also to study the effect of site yield distribution changes on wafers.

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Addendum to "A Kernel-Finding State Assignment Algorithm for Multi-Level Logic"

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Abstract—This paper presents new two new sets of results extending work on state assignment for multi-level logic implementation reported earlier [8]. First, we compared several state assignment algorithms

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