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Interleaved Switching of Parallel ZVS Hysteresis Current Controlled Inverters

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Abstract—A robust self-interleaving mechanism for parallel hysteresis current controlled inverters is proposed, with sustained switching under all load conditions. A fast interleaving technique that can be applied for normal load conditions is combined with a self-interleaving mechanism, which ensures correct switching during voltage clamping operation. A minimum switching frequency and maximum duty cycle is guaranteed under all load conditions enabling the use of low-cost bootstrap circuits to drive the high-side switches. The interleaving approach results in reduced volume of the passive components and better dynamic response. The self-interleaving mechanism was analyzed using the state-plane method, extended to multiple parallel modules. Simulations were conducted to verify the combined operation of both methods and measurements were performed on a 3 kW prototype zero-voltage-switching inverter with a discrete hysteresis current controller.

I. INTRODUCTION

With respect to the switching losses, voltage stress, and natural commutation of the switching node voltage, Zero Voltage Switching (ZVS) inverters have significant advantages over conventional hard switched inverters. A disadvantage is the large circulating current, at least two per unit current stress, that is required to achieve ZVS. This high current results in a large volume of the passive components for high power inverters. Interleaving reduces the input and output current ripple significantly and results in better dynamic response and smaller volume of passive components. The advantages of both techniques can be exploited by combining ZVS and interleaving techniques [1].

ZVS hysteresis current controlled inverters, also referred to as Resonant Pole Inverters (RPI) [2], normally stop switching under voltage clamping conditions (i.e., no voltage difference across the inductor) because the desired current level is not reached. This precludes the use of a low-cost bootstrap circuit to drive the high-side MOSFETs in the switching legs because of the possibility of very long on time. To enable the use of simple bootstrap circuits, a minimum on time of the low side switch and a maximum duty cycle has to be guaranteed. Parallel connected modules, with interleaved switching and guaranteed minimum on time of the low side switch, must maintain interleaved switching under all output conditions to make volume reduction of the passive components possible.

This paper proposes a method to guarantee a minimum on time of the low side switch and maximum duty cycle, together with a novel self-interleaving technique that guarantees interleaved switching under voltage clamping conditions. Both are combined with an improved interleaving technique for normal output condition, based on [3], [4]. The methods together guarantee interleaved ZVS under all output conditions, enabling the use of a low-cost boot strap circuit to drive the high-side switches and a reduced volume of the passive components.

In Section II the basic topology of the RPI is presented. Section III introduces a mechanism to guarantee a minimum on time of the lower switch and a maximum duty cycle, based on additional turn-off criteria. In Section IV the topology is extended to operate in parallel and the advantages of interleaved switching are analyzed. Section V presents the proposed improved interleaved switching method for hysteresis current controlled inverters under normal load conditions. Section VI introduces a novel self-interleaving technique with sustained interleaved switching during voltage clamping. Finally, theory and simulations are compared to measurements of a 3 kW zero voltage switching resonant pole inverter prototype with its control implemented in an FPGA.

II. BASIC TOPOLOGY

Figure 1 shows a single RPI switching leg as presented in [5], where all voltages are referenced to ground. Zero voltage turn-on is guaranteed by ensuring that $i_{LF}$ commutes to the anti-parallel diode before the corresponding switch is turned on. Zero voltage turn-off is achieved by fast turn-off of the switches in combination with limited $du_{sn}/dt$ of switching node voltage $u_{sn}$ during commutation. The limited $du_{sn}/dt$ is accomplished by charging or discharging the switching node capacitance $C_r$, using the energy stored in the filter inductor $L_f$, during the dead-time between switching. A minimum current in $L_f$ is required to guarantee complete commutation of the switching node voltage [2], given by

$$i_{LFmin} = \frac{2}{Z_t} \sqrt{\frac{U_{DC}}{u_{out}}}, \quad (1)$$

where $Z_t = \sqrt{L_f/C_r}$. When applying hysteresis current control to the RPI topology, the rules that have to be applied to guarantee Zero Voltage Switching (ZVS) and generation of the requested output current $i_{out}$ are the following:

1) Turn-off of S1 shall only occur if $i_{LF} \geq i_{LFmin}$.
2) Turn-off of S2 shall only occur if $i_{LF} \leq -i_{LFmin}$.
3) Turn-on of a switch shall only occur when the body diode (D1 or D2) of the corresponding switch starts conducting.

4) The average filter current $i_{LF}$ equals the set-point current $i_{set}$.

Rule 4 is accomplished by setting the turn-off levels such that $i_{set} = (i_{hi} + i_{lo})/2$, where $i_{hi}$ and $i_{lo}$ are the high and low turn-off levels of the hysteresis current controller (see Fig. 2).

Different types of hysteresis current control have been proposed for the RPI topology [6], [7]. Most of them make use of fixed minimum current to guarantee commutation of the switching node voltage over the full output voltage range, given by

$$i_{LF_{\min}} = \max (i_{LF_{\text{min}}}(u_{\text{out}})) = \frac{2}{z_U} U_{DC}. \quad (2)$$

Fixed hysteresis current control [6] results in variable switching frequency, depending on $u_{\text{out}}$, with high circulating current, at least 2 p.u. current stress, over the full range of $i_{set}$. Variable hysteresis current control can be used to minimize the circulating currents. Figure 2 depicts the variable hysteresis current control strategy proposed in [6], where $i_{th}$ has to be set such that commutation of $u_{sn}$ is guaranteed ($\geq i_{LF_{\min}}$) and that the maximum switching frequency is limited. The maximum switching frequency can be approximated by

$$f_{sw_{\text{max}}} \approx \frac{1}{\min (T_{on_{s1}} + T_{sn_{s2}} + T_{on_{s2}} + T_{sn_{s1}})}, \quad (3)$$

where $T_{on_{s1}}$ and $T_{on_{s2}}$ are the time of the corresponding switches, and $T_{sn_{s1}}$ and $T_{sn_{s2}}$ are approximations of the time required to commutate the switching node voltage $u_{sn}$ to the positive or negative supply voltage rail. The maximum switching frequency occurs when $i_{set}$ and $u_{\text{out}}$ are 0, resulting in $T_{on_{s1}} = T_{on_{s2}}$ and $T_{sn_{s1}} = T_{sn_{s2}}$, which leads to

$$f_{sw_{\text{max}}} \approx \frac{1}{4 \left( 2 \frac{L_f}{C_f} i_{th} + 2 \frac{i_{th}}{C_f} U_{DC} \right)} = \frac{\frac{1}{2 \pi} \frac{U_{DC} i_{th}}{2 \frac{L_f}{C_f} i_{th} + \frac{C_f U_{DC}^2}{L_f i_{th}}} \frac{1}{U_{DC} i_{th}}} \quad (4)$$

The switching frequency is limited by the resonance frequency of $C_f$ and $L_f$, resulting in the following upper bound for guaranteed ZVS:

$$f_{sw_{\text{max}}} \leq \frac{1}{2 \pi \sqrt{L_f i_{th}}} \quad (5)$$

Variable hysteresis current control results in a switching frequency that is dependent on both $i_{set}$ and $u_{\text{out}}$, but it leads to less current stress for $|i_{set}| \leq i_{set}$ compared to fixed hysteresis current control, where $i_{set}$ is the maximum set-point current. Also, more sophisticated hysteresis current control schemes have been proposed [7], which include the sign of $u_{\text{out}}$ to reduce the current stress even more under certain output conditions. The approach depicted in Fig. 2 is used in this paper. Table I shows the corresponding turn-off levels.

### Table I

<table>
<thead>
<tr>
<th>$i_{set}$</th>
<th>$i_{hi}$</th>
<th>$i_{lo}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\geq 0$</td>
<td>$2i_{set} + i_{th}$</td>
<td>$i_{th}$</td>
</tr>
<tr>
<td>$&lt; 0$</td>
<td>$-i_{th}$</td>
<td>$2i_{set} - i_{th}$</td>
</tr>
</tbody>
</table>

### III. Sustained Switching

A minimum on time of the lower switch (S2) and a maximum duty cycle is required when a low-cost bootstrap circuit is used to drive the high side switch (S1). This minimum on time is not guaranteed when using hysteresis current control. Normally, hysteresis current controlled inverters stop switching when voltage clamping occurs, that is, when there is no voltage difference left across $L_f$ to change the current ($u_{\text{out}} = \pm U_{DC}$). This halted switching can be prevented by adding additional turn-off criteria to the hysteresis current controller. Such an additional turn-off criterion can be based on $di_{LF}/dt$ or $u_{\text{out}}$.

Figure 3 shows simulated data and the corresponding state-plane for clamping of $u_{\text{out}}$ to the positive supply voltage $U_{DC}$ using variable hysteresis current control on the RPI topology (Fig. 2) combined with the following additional turn-off criteria:

1) $di_{LF}/dt \leq 0$ and $S1$ is conducting then turn off $S1$.
2) $di_{LF}/dt \geq 0$ and $S2$ is conducting then turn off $S2$.

From $t_0$ to $t_1$ in Fig. 3, S1 is conducting and $i_{LF}$ is increasing. When assuming no losses in the resonant circuit and constant $i_{out}$ during the on time of S1, the state...
variables in this interval can be described as follows,

\[ u_{\text{out}}(t) = u_{\text{out}}(t_n) - U_{\text{DC}} \cos(\omega t - t_n) + Z_L i_L(t_n) - i_{\text{out}} \sin(\omega t - t_n) + U_{\text{DC}} \]

where \( Z_L = \sqrt{L_f/C_t} \) and \( Y_L = 1/\sqrt{L_f C_t} \). At \( t_1 \), \( Z_L i_L/dt \leq 0 \) occurs and \( S_1 \) is turned off. The switching node voltage \( v_n \) commutates to the negative supply and \( D_2 \) starts conducting. After that, \( S_2 \) is turned on and \( i_{\text{out}} \) decreases. To ensure that the minimum current required to commutate \( i_{\text{th}} \geq i_{\text{fmax}} \) is reached at \( t_3 \) and \( t_5 \), the radius \( R \) of the circular path in Fig. 3(b), that occurs when \( S_1 \) is conducting, should satisfy \( R \geq R_{\text{min}} = Z_f (i_{\text{th}} - i_{\text{out}}) \). To guarantee ZVS during, or just before, voltage clamping of \( u_{\text{out}} \) to the positive supply, \( i_{\text{f}} \) has to be adjusted to \( i_{\text{f}} = 2i_{\text{out}} - i_{\text{th}} \) if \( i_{\text{out}} < i_{\text{set}} < 0 \) and

\[ u_{\text{out}} - U_{\text{DC}} \geq Z_f i_{\text{f}} - 2i_{\text{th}} \] (8)

To reduce computational load or to allow implementation in an analog circuit, (8) can be simplified to a conservative bound as

\[ 0 \geq (u_{\text{out}} - U_{\text{DC}}) - Z_L (i_{\text{th}} - i_{\text{out}}) \] (9)

Equation (9) triggers the clamping operation in a conservative way, resulting in a reduced slew rate during one switching cycle.

In the state-plane of Fig. 3(b) during voltage clamping operation (6) and (7) describe a half circle with radius \( R \) centered around \((U_{\text{DC}}, Z_f i_{\text{out}})\). This cycle repeats until clamping stops, which occurs when \( i_{\text{out}} \geq i_{\text{set}} \). The above derived equations are valid for clamping of \( u_{\text{out}} \) to the positive supply rail. Similar equations can be derived for clamping to the negative rail. Also a different \( d(i_{\text{th}})/dt \) can be chosen to optimize the minimum on time of the lower switch and the maximum duty-cycle \( (\delta_{\text{max}}) \).

When using the above presented method for sustained switching under voltage clamping conditions, the minimum switching frequency of the RPI topology depicted in Fig. 1, can be approximated as

\[ f_{\text{sw min}} \approx \frac{1}{\max (T_{\text{on}1} + T_{\text{of}1})} \]

when neglecting the influence of the commutation time of \( v_n \). Also the maximum duty cycle can be determined, resulting in

\[ \delta_{\text{max}} \approx \max \left( \frac{T_{\text{on}1}}{T_{\text{on}1} + T_{\text{of}1}} \right) \]

The maximum duty-cycle and minimum on time of the lower switch depend on \( L_f, C_t, i_{\text{th}}, \) and \( i_{\text{out}} \), and are well defined, making it easy to design a low-cost bootstrap circuit to drive the high side switch.

IV. PARALLEL CONNECTION

Figure 4 depicts the parallel connection of modules as proposed in [3]. Every module has its own filter inductance \( L_f \) but the filter capacitor \( C_f \) is shared. This should be compared to simply paralleling switches to achieve the desired output current/power specification, in which case the output filter consists of only one inductor and capacitor.

Parallel modules with interleaved switching present advantages over paralleling of switching devices. The
effective switching frequency of the system is \( N \) times higher. As a consequence the response time to a change of \( t_{set} \) is on average \( N \) times faster than for single modules, resulting in a better dynamic response. Each module supplies only \( N^{-1} \) of the current to the load resulting in less stored energy per filter inductor. When assuming the same number of switches used for both \( N \) parallel modules and a single module, and that \( i_{th} = i_{th_{min}} \) for \( t_{set} = t_{set} \), the ratio between total stored energy in \( N \) parallel inductors and a single inductor becomes

\[ \frac{E_{L_{N,sh}}}{E_{L_{sh}}} = \frac{N + 1}{2} \left( 2N^{-1}i_{set} + 2N^{-1}i_{th} \right)^2 = 1. \]  

(12)

Due to the \( N \) times smaller ripple current with \( N \) times higher frequency that occurs due to interleaved switching, the capacitance, and consequently the volume of \( C_{tr} \), can be reduced compared to paralleling of switching devices. For equal maximum voltage ripple on \( U_{out} \), the ratio between the filter capacitance required for \( N \) parallel modules with interleaved switching \( C_{tr,N} \) and a single module \( C_{tr} \) becomes

\[ \frac{C_{tr,N}}{C_{tr}} = \frac{1}{N^2}. \]  

(13)

The current ripple through \( C_{tr} \) is reduced significantly compared to a single module, leading to a significant total volume decrease of the passive components compared to a single module with parallel switching devices. This is at the cost of \( (N-1) \) more circuits to sense the individual filter inductor currents.

V. INTERLEAVED SWITCHING

In [3] a master-slave interleaving scheme is presented based on correcting ramps that are added to the turn-off current levels. The approach is improved in [4] to operate in a ring configuration. Ramps can be used to steer the time shift between the filter inductor current ripples \( (i_{L,f}) \) of the individual modules. Figure 5 depicts the current waveform \( i_{L,f} \) for a single module, together with the desired current waveform and the correcting ramps \( r_p \) and \( r_n \). The correcting ramps are added to both turn-off levels, \( i_{hi} \) and \( i_{lo} \), to improve the dynamic response [4]. To steer the actual current waveform to the desired current waveform, the control ramps are positioned such that they intersect \( i_{hi} \) and \( i_{lo} \) at the time of desired turn-off of the corresponding switch [3]. This results in a time shift and, as a consequence, convergence of the actual \( i_{L,f} \) to the desired waveform.

The interleaving scheme, using correcting ramps, can be analyzed from the time-shift between the actual and desired waveform before \( \Delta T_{sh}[k] \) and after \( \Delta T_{sh}[k+1] \) each switching cycle (see Appendix). The time-shift is given by

\[ \Delta T_{sh}[k+1] = \left( \frac{di_{L,f1}}{dt} - \frac{dr_p}{dt} \right) \left( \frac{di_{L,f2}}{dt} - \frac{dr_n}{dt} \right) \Delta T_{sh}[k], \]  

(14)

where \( di_{L,f1}/dt \) is the slope of \( i_{L,f} \) when \( S1 \) is conducting, \( di_{L,f2}/dt \) the slope of \( i_{L,f} \) when \( S2 \) is conducting, and \( dr_p/dt \) and \( dr_n/dt \) are the slopes of the ramps that are added to \( i_{hi} \) and \( i_{lo} \). Equation (14) results in stable convergence to the desired waveform if

\[ \left( \frac{di_{L,f1}}{dt} - \frac{dr_p}{dt} \right) \left( \frac{di_{L,f2}}{dt} - \frac{dr_n}{dt} \right) < 1, \]  

(15)

and in dead-beat control if the numerator of the polynomial equals 0. If the denominator becomes zero, switching is halted. This cannot occur if (15) is satisfied.

By substituting \( dr_p/dt \) with \( \kappa di_{L,f1}/dt \) and \( dr_n/dt \) with \( \kappa di_{L,f2}/dt \) the speed of convergence can be set by choosing \( \kappa \) between 0 and 1, resulting in

\[ \Delta T_{sh}[k+1] = \left( \frac{di_{L,f1}}{dt} - \kappa \frac{di_{L,f2}}{dt} \right) \left( \frac{di_{L,f2}}{dt} - \kappa \frac{di_{L,f1}}{dt} \right) \Delta T_{sh}[k]. \]  

(16)

The slope of the ramps can be calculated from the measurement of \( U_{out} \) for a given \( U_{DC} \) and \( L_f \), leading to a simple adaptive interleaving control scheme compared to the scheme proposed in [3], where the slope of the ramps is fixed.

The time-shift between the inductor currents of \( N \) individual parallel modules can be controlled by adding ramps to the turn-off levels of the \( N-1 \) slave modules. The steady-state time shifts \( T_{sh} \) between the inductor currents and consequently the positive and negative ramps can be determined from the steady-state switching time of the master module \( T_{sw} = T_{sw}[k] = T_{sw}[k-1] \) as

\[ T_{sh} = T_{sw} \frac{x}{N}, \]  

(17)

where \( x \) is the number of the corresponding slave module \([1, 2, \ldots, N-1]\).

The time shifts in (17) are used for the positioning of the correcting ramps \( r_p \) and \( r_n \), which are added to \( i_{hi} \) and \( i_{lo} \) of the slave modules. This can be seen from Fig. 6, where \( T_{sh1} = t_f - t_6, T_{sh2} = t_8 - t_6, T_{sw} = t_9 - t_6, N = 3, \) and \( d_i \) is the positive turn-off level after a step on \( t_{set} \) is applied. In [3] the time-shifts of the positive ramps \( r_p \) are determined from the previous switching period of the high-side switch of the master module.
T_{sw1} [k−1], eg. (t_{2}−t_{0}) for the ramps r_{p}, positioned in the interval (t_{2},t_{4}), when using this method with positive and negative ramps. The time shifts of r_{n} would be determined from the previous switching period of the low-side switch (T_{sw2} [k−1]), eg. (t_{3}−t_{1}) for the ramps r_{n}, positioned in the interval (t_{3},t_{5}). However, faster dynamic response can be obtained by using the newest available switching time of both the high-side and the low-side switch of the master module to position both r_{n} and r_{p}. This can be seen from the bottom graph of Fig. 6 (i_{CS}), where both the original (based on [3]) and the proposed methods are applied for Δi_{set} = 5 A and κ = 0.5. For clarity, the individual inductor currents are only plotted for the proposed method.

Component variation of L_{f} results in different steady-state switching times of the individual parallel modules. As a consequence sub-optimal time shifts and small steady-state current differences between the individual parallel modules will occur. Also a ripple component with frequency equal to 1/T_{sw} will appear. Component variation between the filter inductors of the individual modules should be kept low. The disturbance can be seen in Fig. 7 where the simulated step response is depicted under the same conditions as in Fig. 6 but with 5% variation of the individual filter inductors (L_{f}). Simulations were conducted with the parameters and component values shown in Table II.

VI. INTERLEAVED SWITCHING UNDER VOLTAGE CLAMPING CONDITIONS

During voltage clamping operation of parallel modules (u_{out} = ±U_{DC} in Fig. 1), (16) is not valid and the interleaving approach using correcting ramps is not effective. The ramps, used for interleaving during normal operation, have to be disabled during voltage clamping operation. Under voltage clamping conditions, no voltage is left across L_{f} to change the current. Because the filter capacitor C_{f} is shared, this occurs for all parallel connected modules simultaneously, and synchronization, not interleaving, of i_{Lf} will occur if one of the additional turn-off criteria is satisfied. To prevent this the additional criteria are extended to the following,

1) If di_{Lf}/dt ≤ 0 and S1 is conducting, then only turn off S1 of the module carrying maximum i_{Lf}.
2) If di_{Lf}/dt ≥ 0 and S2 is conducting, then only turn off S2 of the module carrying minimum i_{Lf}.

To analyze the behavior during voltage clamping, the state-plane of Fig. 3(b) was extended to multiple parallel modules. Figure 9 depicts the time waveform and the corresponding state-plane of the filter inductor current for N = 3 parallel modules, when applying the extended additional turn-off criteria, and for voltage clamping to the positive supply rail. During time intervals (t_{4},t_{6}), (t_{6},t_{8}), and (t_{8},t_{10}), S1 of all modules is closed until di_{Lf}/dt ≤ 0 occurs. This can be modeled as in Fig. 8(a), when assuming i_{out} constant over one switching cycle. For this condition the state-plane for the sum of the filter inductor currents (Σi_{Lf}) can be defined using impedance Z_{i}, depicted in the right graph of Fig. 9(b). The resonance that occurs during conduction of S1 of all parallel modules describes a half circle with radius R', centered round (U_{DC}, Z_{i}i_{out}) in the state-plane. This can be translated to a state-plane representation for individual filter inductor currents using impedance Z_{i} = N Z_{f}, which is depicted in the left graph of Fig. 9(b). At times t_{5}, t_{7}, and t_{9}, turn-off occurs of S1 of the module carrying maximum i_{Lf} due to di_{Lf}/dt ≤ 0. As a consequence commutation of the corresponding switching node voltage u_{out} occurs, after which S2 is turned on. The filter inductor current i_{Lf} of the commutating module decreases until t_{10} is hit in intervals (t_{1},t_{4}), (t_{5},t_{6}), (t_{7},t_{8}), and (t_{8},t_{10}). This can be modeled as in Fig. 8(b). During the current commutation u_{out} remains approximately constant due to the relatively short time of the resonance that is completed during commutation. The current in the filter inductors that are not commutating will therefore be approximately constant during current commutation. This can be seen from the left graph of Fig. 9(b). After current commutation, S2 is turned off again and transition of u_{out} occurs. The cycle repeats until clamping of u_{out} stops. From Fig. 9 it can be seen that self-interleaving occurs when using the suggested additional turn-off criteria.

For clamping of u_{out} to the positive supply U_{DC}, when assuming i_{Lf} constant for the modules that are not commuting, the filter inductor currents of the N−1 modules
that are not commutating at $t_4$, $t_6$, $t_8$, and $t_{10}$ can be determined from $i_{io}$, together with the current increase in each cycle, which equals $2R'_f/Z_N = 2/N \sum i_{Lf} - i_{out}$. A discrete-time description for the transient behavior of the inductor currents is given by

$$i_{Lf}[k+2] = G i_{Lf}[k] + H u[k]$$  \hspace{1cm} (18)

where $i_{Lf}$ is a vector containing the $N-1$ inductor currents of the modules that are not commutating, sorted from high to low, and $u$ is a vector containing the output current $i_{out}$ and the negative turn-off level $i_{lo}$, that is,

$$i_{Lf}[k] = \begin{bmatrix} i_{Lf_1} \\ \vdots \\ i_{Lf_{N-1}} \end{bmatrix}, \quad u[k] = \begin{bmatrix} i_{out} \\ i_{lo} \end{bmatrix}.$$  \hspace{1cm}

$G$ is of size $(N-1)\times(N-1)$ and $H$ of size $(N-1)\times2$ and are found to be

$$G = \begin{bmatrix} 0 & I \\ 0 & 0 \end{bmatrix} - \frac{2}{N} J, \quad H = \frac{2}{N} \begin{bmatrix} 1 & -1 \\ \vdots & \vdots \\ 1 & -1 + \frac{N}{2} \end{bmatrix},$$

where $I$ is an identity matrix of size $(N-2)\times(N-2)$ and $J$ a unit matrix of size $(N-1)\times(N-1)$. A consequence of (18) is that an addition of $2R'_f/Z_N$ to the corresponding $N-2$ inductor currents occurs, where the lowest current is defined by $i_{lo} + 2R'_f/Z_N$. Stability of the self-interleaving mechanism can now be determined by examining the eigenvalues of $G$. The approach results in stable interleaved switching if all eigenvalues are within the unit circle. Interleaved switching occurs only when $N$ is odd, for an even number of parallel modules, $G$ has one eigenvalue on the unit circle at $-1$, see Fig. 11. No convergence to interleaved switching for $N$ is even occurs when using $di_{Lf}/dt = 0$ as additional turn-off criterion, shown in Fig. 10. The eigenvalues will be closer to the unit circle for increasing $N$, resulting in decrease of speed of convergence for an increasing, odd, number of parallel modules (see Fig. 11).

For parallel connected modules also other measures are required to ensure that commutation of $u_{sn}$ is possible. To guarantee ZVS during, and just before, voltage clamping to the positive supply, $i_{lo}$ has to be adjusted to $i_{lo} = 2i_{out}/N - i_{th}$ if $i_{out} < i_{set} < 0$ and

$$0 \geq (u_{out} - U_{DC})^2 + Z_f^2 \left( \sum i_{Lf} - i_{out} \right)^2 - \frac{1}{4} N^2 Z_f^2 \left( i_{th} - \max (i_{Lf}) \right)^2,$$  \hspace{1cm} (19)

where $\max (i_{Lf})$ represents the highest of the $N$ filter inductor currents. To reduce computational load or to allow implementation in an analog circuit, (19) can be simplified to a conservative bound as

$$0 \geq (u_{out} - U_{DC}) - \frac{1}{2} NZ_f \left( i_{th} - \max (i_{Lf}) \right).$$  \hspace{1cm} (20)

The above derived equations are valid for clamping of $u_{out}$ to the positive supply rail. Similar equations can be derived for clamping to the negative supply rail.

Fig. 8. Equivalent schematics for voltage clamping to $U_{DC}$.

Fig. 9. Interleaved switching during voltage clamping, $N=3$.

Also a different $di_{Lf}/dt$ can be chosen as an additional turn-off criterion. When choosing $di_{Lf}/dt < 0$ for clamping to the positive supply rail $U_{DC}$ and $di_{Lf}/dt > 0$ for clamping to the negative rail $-U_{DC}$, this results in steady-state interleaved switching for any number of parallel connected modules. This is not treated in this paper and will be discussed elsewhere.

VII. EXPERIMENTAL RESULTS

The proposed interleaving method was implemented in the FPGA of a digitally controlled 2.8 kW RPI prototype, based on an existing 12 kW 3 phase hysteresis current controlled ZVS inverter. The related parameters, supply voltage and component values are presented in Table II.

The threshold current $i_{th}$ was chosen at 5 A to limit the maximum switching frequency to approximately 30 kHz, although 1.2 A is sufficient to guarantee commutation of $u_{sn}$ over the full output voltage range of the converter. Fig 12 shows the measured step response of the proposed
interleaving method, which is in good agreement with the simulation results presented in Fig. 7, and confirms the fast dynamic response of the approach.

Measurements with sinusoidal excitation were made to verify the achieved ripple cancellation, the results are depicted in Fig. 13. A ripple current amplitude of 2.5 A is achieved for $i_{\text{set}} = 5 + 5 \sin(2\pi50t)$ A. This is in good agreement with the factor $N$ reduction of the ripple current that can be expected from odd interleaved triangular current waveforms.

![Image](image_url1)

![Image](image_url2)

![Image](image_url3)

![Image](image_url4)

![Image](image_url5)

**TABLE II**

<table>
<thead>
<tr>
<th>item</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{DC}}$</td>
<td>70 V</td>
</tr>
<tr>
<td>$i_{\text{th}}$</td>
<td>5 A</td>
</tr>
<tr>
<td>$N$</td>
<td>3</td>
</tr>
<tr>
<td>$C_f$</td>
<td>9 nF</td>
</tr>
<tr>
<td>$L_f$</td>
<td>120 $\mu$H</td>
</tr>
<tr>
<td>$C_f$</td>
<td>100 $\mu$F</td>
</tr>
<tr>
<td>$L_t$</td>
<td>4.5 mH</td>
</tr>
<tr>
<td>$R_t$</td>
<td>1.4 $\Omega$</td>
</tr>
</tbody>
</table>

![Image](image_url6)

Figure 14 shows the step response with voltage clamping, demonstrating fast convergence to interleaved switching when moving back and forth between voltage clamping and normal operation.

**VIII. CONCLUSION**

An all-digital interleaving method is suggested in this paper, aiming to improve the system dynamic response. The effectiveness of the method is analytically demonstrated. Simulations done on models with component variation confirm the effectiveness of the approach. The suggested interleaving method shows significant improvements on ripple current cancellation, dynamic response, and total volume of the passive components, compared to a single module. A self-interleaving mechanism for odd number of modules is proposed and is demonstrated analytically and with simulations. This results in a maximum on time of the high side switches during voltage clamping operation, enabling the use of low-cost bootstrap circuits for ZVS hysteresis current controlled converters. A 3 kW...
can be expressed as follows,

\[ \Delta T_{sh}[k] = \Delta T_{sh}[k] - \Delta T_{sh}''[k], \] (21)

where

\[ \Delta T_{sh}''[k] = \delta i_p \frac{d i_{lid1}}{dt} - \frac{d i_{lid1}}{dt}, \] (22)

and

\[ \delta i_p = - \frac{d r_p}{dt} \frac{d i_{lid1}}{dt} - \frac{d r_p}{dt} \Delta T_{sh}[k]. \] (23)

Combining (21) to (23) results in

\[ \Delta T_{sh}'[k] = \frac{\frac{d i_{lid1}}{dt} - \frac{d i_{lid1}}{dt}}{\frac{d i_{lid1}}{dt} - \frac{d i_{lid1}}{dt}} \Delta T_{sh}[k]. \] (24)

Figure 15(b) depicts the negative correcting ramp with the corresponding current waveforms. \( \Delta T_{sh}[k+1] \) represents the time difference between the actual and desired inductor current after turn-off of S2. The time shift of \( i_{LF} \) that occurs due to \( r_n \) can be expressed as follows,

\[ \Delta T_{sh}[k+1] = \Delta T_{sh}'[k] - \Delta T_{sh}''[k], \] (25)

where

\[ \Delta T_{sh}''[k] = \delta i_n \frac{d i_{lid2}}{dt} - \frac{d i_{lid2}}{dt}, \] (26)

and

\[ \delta i_n = - \frac{d r_n}{dt} \frac{d i_{lid2}}{dt} - \frac{d r_n}{dt} \Delta T_{sh}[k]. \] (27)

ACKNOWLEDGMENT

The authors would like to thank Jan Coenders for the valuable discussions on non-interleaved zero-voltage-switching hysteresis current controlled inverters and sustained zero-voltage switching under all load conditions. Special thanks go to Han Severt for his help writing and debugging the amplifier’s firmware.

REFERENCES


