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Limits to Performance Spread Tuning using Adaptive Voltage and Body Biasing

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Abstract— In this paper we examine technology constraints on tuning active power and delay using adaptive voltage scaling (AVS) and adaptive body biasing (ABB) design techniques. To serve this purpose, a test circuit was fabricated in a 90nm triple-well low-power CMOS technology. The analysis hereby presented is based on a ring oscillator running at 488MHz and a circular shift register with 8K flip-flops and 50K gates. Measurement results indicate that it is possible to reach 24.4x power savings by 6.1x frequency downscaling using AVS, $\pm 24\%$ power and $\pm 22\%$ frequency tuning at nominal conditions using ABB only, 127x power savings with 37.4x frequency downscaling by combining AVS and ABB.

I. INTRODUCTION

Manufacturing variations of fundamental design parameters and the search for optimum low-power designs have opened avenues to the application of adaptive techniques to control the power supply (V_{DD}) and threshold voltage (V_{th}). Design technologies such as AMD's PowerNow! [1], Transmeta's LongRun [2], Intel's Enhanced SpeedStep [3] are vivid examples of commercial ICs that use power management based on power supply scaling. In addition, chip demonstrators with V_{DD} and V_{th} scaling capabilities have also been reported in the literature archival [4]-[8]. Other reported uses of V_{DD} and V_{th} scaling, besides power management in processors, are in testing [9], product binning [10], and yield tuning [11].

In this paper we investigate technology constraints on active-power and delay tuning. In particular we are interested in finding what power-delay tradeoffs can be made, how V_{DD} and V_{th} scaling relate to circuit activity and investigate how far can process-dependent performance spread be tuned.

Our test chip consists of a clock generator unit (CGU) and a circular shift register in a triple-well low-power (LP) 90nm CMOS technology with a nominal power supply of 1.2V. The CGU consists of seven independent ring-oscillators and corresponding selection circuitry. The ring-oscillators use minimum sized inverters as delay elements, a 2-input NAND gate for enabling control, and a divide-by-2 circuit for duty cycle recovery. The shift register contains 8K flip-flops and 50K logic gates. The logic gates are connected

as delay lines between two consecutive flip-flops, which have an average logic depth of 6. One can emulate the activity of a core with this circular shift register by shifting in a sequence of zeros and ones. The design was laid out with a commercial place-and-route tool using constrained area-routing features for both circuit blocks. The circuit has independent bias control over its PMOS and NMOS transistors by properly adjusting the N-well and P-well voltages, respectively. Measurements were performed using an Agilent 93K SoC test system in a controlled temperature (25degC) environment enabled by a Temptronic thermostream. The fastest measured oscillator runs at a frequency of 488MHz. In the remainder of this paper, we will refer to the ring oscillator as "ringo".

In [13] we have already shown the results for the CGU when fabricated in a general-purpose (GP) 90nm CMOS technology with a nominal supply of 1V. The results shown in this paper extend the results in [13] in two ways: (i) we will show results for a power-optimized 90nm CMOS technology, and (ii) we will report V_{DD} and V_{th} scaling ranges to tune process-dependent performance spreads.

Section 2 introduces the voltage conventions we used for AVS and ABB. In section 3 we will focus on frequency scaling as well as frequency tuning. Section 4 deals with the use of AVS and ABB for reduction of power demand. Section 5 explores the potential of AVS and ABB for online performance compensation.

II. SCALING OPERATIONS

We will now briefly describe the adaptive voltage scaling (AVS) and adaptive body bias (ABB) schemes. An AVS operation consists in sweeping the power supply while maintaining the body bias constant. ABB is essentially the contrary approach: V_{DD} is kept constant and the body bias is swept. Finally, AVS+ABB is the case when both body biasing and power supply are swept. Table 1 presents the voltage ranges we have employed during our measurements. Observe that the wells were forward biased for at most 0.6V and reverse biased by 1.2V, independently of the power supply value. Forward biasing is constrained by the turn-on

voltage of the transistors' body-to-source junction diode. Essentially, reverse biasing is unconstrained, but high reverse biasing voltages result in increased (junction) leakage. We will now illustrate how these techniques can be used to alter the performance of integrated circuits.

TABLE I. VOLTAGE CONVENTIONS FOR SCALING OPERATIONS

Operation	Description	Variable	Range
AVS	Adaptive Voltage Scaling	V_{DD}	[0.6, 1.2]V
ABB	Adaptive Body Biasing	V_{nwell} V_{pwell}	$[V_{DD}-0.6, V_{DD}+1.2]$ V $[-1.2, 0.6]$ V
AVS+ABB	Adaptive Voltage and Body Biasing	V_{DD} V_{nwell} V_{pwell}	$[0.6, 1.2]$ V $[V_{DD}-0.6, V_{DD}+1.2]$ V $[-1.2, 0.6]$ V

III. FREQUENCY SCALING AND TUNING

Let us first investigate the dynamic range of the ring oscillator. To a first order approximation the frequency can be calculated as $f \approx K \cdot V_{DD}^{-1} (V_{DD} - V_{th})^\alpha$ [12], where f is the frequency of operation, K is a proportionality factor and α is a process dependent parameter that models velocity saturation. In the case of velocity-saturated devices, α is close to 1. Because of the low α factor, it follows then that frequency scales almost linearly with V_{DD} .

Figure 1. Frequency scaling and tuning for the ringo.

Figure 1 shows the ringo frequency as function of power supply. Each cloud of dots is associated to a unique V_{DD} value. Each dot in a cloud corresponds to a unique N-well and P-well bias combination, and the line joining clouds indicates the nominal trend. Observe that the frequency increases by 6.1x when V_{DD} is scaled up from 0.6V to 1.2V.

We can now analyze the impact of ABB as a frequency tuning mechanism at each V_{DD} point. Notice from Figure 1 that the relative tuning range is not the same for all V_{DD} values. In particular, we measured frequency spans of approximately $\pm 80\%$ at $V_{DD}=0.6$ V and $\pm 22\%$ at $V_{DD}=1.2$ V w.r.t. their nominal frequencies. This unbalance is because

the effective gate drive of the transistors is smaller at low V_{DD} values. For the measured silicon, ABB gives an absolute tuning range of 241MHz for the chosen well voltages operating at a nominal power supply of 1.2V.

IV. POWER AND FREQUENCY TUNING

The ultimate goal of the AVS and ABB schemes is performance tuning with performance being the optimal combination of frequency and power, i.e. the lowest power for a fixed frequency. Figure 2 presents a plot of frequency as function of the total power of the CGU, e.g. both CGU-static and dynamic power consumption of the ringo.

Figure 2. Frequency versus total power.

The plot of Figure 2 puts us in state to evaluate power savings and tuning range control of AVS and ABB. Measurement results of the ringo indicate a 24.4x power savings by 6.1x frequency downscaling using AVS over half of the entire V_{DD} range. The use of ABB at $V_{DD} = 1.2$ V results in $\pm 24\%$ power and $\pm 22\%$ frequency tuning w.r.t the nominal operating point. The combination of AVS and ABB yields 127x power savings with 37.4x frequency scaling from the highest possible frequency (minimum V_{th}) to the lowest one (maximum V_{th}). These results show the strength of the combined use of AVS and ABB.

Figure 3. Frequency versus total power trade-off.

Let us now explore possible performance tradeoffs by using AVS and ABB. Figure 3 shows a zoom-in of Figure 2 at $V_{DD}=1.2V$. If AVS and ABB are applied such that the nominal V_{DD} becomes 1.1V instead of 1.2V, and the V_{th} 's are pulled to a smaller value as indicated by the arrow in Figure 3, we see that it is possible to achieve 16% power savings w.r.t. the nominal conditions at no frequency penalty. A more aggressive V_{DD} downscaling to 1.0V, while pulling the V_{th} 's to their minimum value, results in 33% power savings at less than 1% frequency penalty. It is clear, thus, that AVS+ABB can lead to significant power savings without serious performance penalty.

Figure 4. Total power of the core as a function of well biasing.

Next we investigate the properties of ABB on the shift register. Figure 4 shows the core's total power for a given circuit activity, $V_{DD}=1.2V$ and scaling of the P-well biasing; each dot in the clouds is associated to the N-well biasing. The line joining clouds indicates the case when symmetric well biasing is applied. Observe that the well biasing allows a total power tuning range of about 50mW; this represents half of the nominal power consumption.

Figure 5. Total power correlation for the shiftregister and the ringo for different V_{DD} values.

Figure 5 shows a power correlation between the shift register and the ringo for different V_{DD} values. In this plot we have used the same conventions as before, i.e. each cloud is associated to a unique V_{DD} value and each point in the cloud corresponds to a unique N-well and P-well bias combination. The shift register operates at the same V_{DD} as the ringo, while its operating frequency is provided by the ringo. The circuit activity of the shift register is kept constant. The dynamic power dominates the total power in both circuit blocks, and therefore, their total power consumption can be estimated by $P \approx aC \cdot V_{DD}^2 \cdot f$, where aC represents the switching circuit capacitance, V_{DD} is the power supply voltage and f is the frequency of operation. Since both circuit blocks operate at the same V_{DD} and f , their power consumption is linearly related by a ratio determined by the switching circuit capacitance. This can be observed in Figure 5, where the power consumption of the circuit blocks remains linearly correlated while applying AVS and/or ABB.

V. PERFORMANCE COMPENSATION

As the variation of fundamental parameters such as channel length, threshold voltage, thin oxide thickness and interconnect dimensions goes well beyond acceptable limits, “on the fly” performance compensation is becoming necessary. While process spreads are tightly controlled, their impact on circuit design and behavior is higher and higher. For instance, while before a V_{th} variation of say 50mV on a nominal V_{th} of 450mV was not that crucial, in deep sub-micron technologies with a nominal V_{th} of 250mV this variation can make circuit operation quite difficult.

Figure 6. Frequency spread and performance tuning.

Figure 6 shows an example of performance spread in which frequency is plotted against power supply for twelve different samples. Additionally, frequency tuning using ABB for three selected samples is shown as well. Samples were selected as “fast”, “typical” and “slow” with nominal frequencies of 521MHz, 477MHz, and 453MHz, respectively. The total frequency spread of the limited sample set of the ringo is 68MHz. Despite this spread, it is possible to tune its frequency to the “typical” ringo. This gives basically a 100% parametric yield improvement.

Let us investigate now up to what extent the frequency spread can be compensated. When ABB is used while operating at the nominal supply voltage, the frequency range of the “fast” ringo is $399\text{MHz} < f_{\text{fast}} < 629\text{MHz}$, the one of the “slow” ringo is $329\text{MHz} < f_{\text{slow}} < 558\text{MHz}$, while the “typical” ringo operates in the range of $354\text{MHz} < f_{\text{typical}} < 581\text{MHz}$. Notice that the tuning is continuous for all frequencies.

Figure 7. “Fast” to “typical” ringo and “slow” to “typical” ringo performance compensation.

Figure 7 shows a frequency correlation between sample “fast”, sample “slow” and sample “typical”. As an example we use ABB to lower the nominal frequency of the “fast” sample to the one of the “typical” sample as indicated by arrow A. Several combinations of V_{th} ’s can provide the required frequency of 477 MHz. For our limited sample set, performance compensation could be achieved using a symmetric bias for N-well and P-well of value 300mV reverse and 200mV forward bias.

VI. CONCLUSIONS

We presented measurement results that show the extent to which adaptive voltage scaling and adaptive body bias are useful for active-power and delay tuning in a state-of-the-art CMOS technology. Although the results were obtained from this particular 90nm CMOS technology, they are well suited as indices for reference purposes.

This paper shows that AVS renders a wide frequency-scaling control and significant power savings. The index factors are 24.4x power savings by 6.1x frequency downscaling. While the frequency and power tuning range of ABB may look limited (index factors $\pm 24\%$ power and $\pm 22\%$ frequency tuning @ $V_{\text{DD}} = 1.2\text{V}$), the frequency tuning range proves to be effective for process-dependent performance compensation. In fact, we observed a continuous frequency tuning despite the wide frequency spread. With AVS and ABB together it is possible to attain 127x power savings with 37.4x frequency downscaling. These indices show that the combined use of AVS and ABB offers significant performance control.

More work is needed to qualify this design technology in deep sub micrometer technologies, e.g. to assess the implications of V_{DD} and V_{th} scaling on circuit activity, noise margins, power supply noise among other parameters.

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