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Efficient Estimation of Die-Level Process Parameter Variations via the EM-Algorithm

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Abstract— A new approach for efficient estimation of die-level process parameter variations based on the expectation-maximization algorithm is proposed. To estimate the parameters and enhance diagnostic analysis, dedicated embedded sensors have been designed. Additionally, to guide the test with the information obtained through monitoring process variations, maximum-likelihood method and adjusted support vector machine classifier is employed. The information acquired is re-used and supplement the circuit calibration. The proposed estimation method is evaluated on a prototype ADC converter with dedicated sensors fabricated in standard single poly, five metal 0.09- μm CMOS.

I. INTRODUCTION

CMOS technologies move steadily toward finer geometries, which provide higher digital capacity, lower dynamic power consumption and smaller area, which results in integration of whole systems, or large parts of systems, on the same chip. However, due to technology scaling ICs are becoming more susceptible to variations in process parameters and noise effects like power supply noise and cross-talk reduced supply voltage and threshold voltage operation. Likewise, imperfection at the manufacturing stage, with a raw factory yield between 50-95%, depending on the maturity of the process technology, silicon area, and extending the use of 193nm lithography for sub-65 nm CMOS technology, where Resolution Enhancement Techniques are no longer sufficient for accurate device definition, significantly impact circuit performance. With increased system complexity and reduced access to internal nodes, the task of properly testing these devices is becoming a major bottleneck. The large number of parameters required to fully specify the performance of mixed-signal circuits and the presence of both analog and digital signals in these circuits make the testing expensive and a time consuming task. Particularly for nanometer CMOS ICs, the large number of metal layers with increasing metal densities, prevents physical probing of the signals for debug purposes. Since parameter variations depend on unforeseen operational conditions, chips may fail despite they pass standard test procedures.

To enhance observation of important design and technology parameters, such as temperature, threshold voltage, etc., dedicated sensors are embedded within the functional cores [1-3]. To guide the test with the information obtained through monitoring process variations, we employed maximum-likelihood method and adjusted support vector machine (SVM) classifier [4-5], since it simultaneously minimize the classification error and maximize the geometric margin. Although, in statistics several methods, such as listwise [6] and pairwise [7]

deletion and structural equation modelling [8] would provide us with estimates of the selected performance figures (from the incomplete data), imputation method and its special case, multiple imputations based on expectation-maximization (EM) algorithm [9-10] offers maximum likelihood estimates of parameters in probabilistic models, where the model depends on latent variables. The proposed estimation method is evaluated on an analog to digital converter (ADC) as the appropriate representative. Since functional fault in each of the analog component in the multi-step ADC affects the transfer function differently [11], analyzing this property form the basis of our approach.

II. MULTI-STEP ADC

A. Multi-Step ADC Architecture

The input signal is sampled by a three-times interleaved sample-and-hold (S/H), eliminating the need for re-sampling of the signal after each quantization stage. As shown in Figure 1, the S/H splits and buffers the analogue delay line sampled signal that is then fed to three A/D converters (ADCs), namely, the Coarse (4 bits), the Mid (4 bits) and the Fine (6 bits). The quantization result of the Coarse A/D converter is used to select the references for the mid quantization in the next clock phase. The selected references are combined with the held input signal in dual-residue amplifier, which is offset calibrated [12-14].

Figure 1: Block diagram of the Multi-step ADC and part of the test control circuitry.

The Mid A/D converter quantizes the output signals of these mid-residue amplifiers. The outputs from both coarse and mid A/D converters are combined in order to select proper references for the fine quantization. These references are combined with the sampled input signal in, also offset

calibrated, dual-residue amplifier. The amplified residue signals are applied to a Fine A/D converter. In multi-step ADC, high linearity is obtained by extensive usage of correction and calibration procedures. Providing structural DFT and BIST capabilities to this kind of ADCs is difficult since the effects of correction mechanism must be taken into account. Overlap between the conversion ranges of two stages have to be considered, otherwise, there may exist conflicting operational situations that can either mask faults or give an incorrect fault interpretation.

B. Multi-Step ADC error sources

The static parameters are determined by the analog errors in various ADC components and therefore, a major challenge in ADC test is to estimate the contribution of those individual errors to the overall ADC linearity parameters. The overall A/D converter consists primarily of non-critical low-power components, such as low-resolution quantizers, switches and open-loop amplifiers. If timing errors are not considered, the primary error sources present in a multi-step ADC are decision stage offset errors (λ), stage gain errors (η), and errors in the internal reference voltages (γ). Each of these errors is the combined result of two physical effects: noise, which includes charge injection noise in analog switches, thermal, shot and flicker noise, and noise coupled from digital circuitry (via crosstalk or substrate), and on-chip process parameter variation, e.g. device mismatch. The offset errors include offset caused by either component mismatch, self heating effects, comparator hysteresis or noise. The gain error group includes all the errors in the amplifying circuit, including technology variations and finite gain and offset of the operational amplifier. The reference voltage errors are caused by resistor ladder variations and noise, as well as to errors in the switch matrix, which are mainly due to charge injection in the CMOS transmission gate.

Figure 2: Coarse ADC with built-in sensors.

C. Dedicated Sensors

To illustrate the concept of Die-level process monitors (DLPMs) [3], consider only the Coarse ADC, which is a simple four bit flash stage as shown in Figure 2, consisting of reference ladder and sixteen comparators. From the previous analysis one can conclude that the gain, decision and reference ladder are crucial to the proper Coarse ADC's performance. To mimic the DUT behavior, the gain-based DLPM and decision stage-based DLPM are extracted (replicated) from that particular part of the DUT [3]. The DLPM measurements are directly related to asymmetries between the branches composing the circuit, giving an estimation of the offset when both DLPM inputs are grounded or set at predefined common-mode voltage.

Figure 3: Stage gain-based DLPM schematic view.

As shown in Figure 3, the gain-based monitor consists of the circuitry replicated from the observed ADC gain stage, which consists of a differential input pair (transistors T_1 and T_2) with active loading (T_3 and T_4) and some additional gain (transistors T_5 and T_6) to increase the DLPM resolution and transistors T_7 and T_8 to connect to read lines (lines leading to a programmable data decision circuit). Similarly, in the proposed decision stage monitor circuit (Figure 4) the latch (transistors T_{12} to T_{17}) has been broken to allow a DC current flow through the device needed for the intended set of measurements.

Figure 4: Decision stage -based DLPM schematic view.

In addition to these two, internal reference voltages monitoring circuit as shown in Figure 5 sense the mismatching between two of the unit resistors used in the actual resistor ladder design. The current that flow through the resistors (whose values are extracted from the ladder

itself) is fixed using a current mirror. Since the current is fixed, the voltage drop between the nodes labeled V_1 and V_2 is a measurement of the mismatching between the resistors. The chosen current mirror topology is reliable enough to neglect the possible deviations due to transistor mismatch.

Figure 5: Internal reference voltages-based DLPM schematic view.

By extracting the DLPM circuit from the DUT itself, the DLPM circuit accomplishes some desirable properties: *i)* it is designed to maximize the sensitivity of the circuit to the target parameter to be measured, *ii)* it matches the physical layout of the extracted device under test, *iii)* it is small and stand alone, consumes no power while in off state, and *iv)* the design of the DLPM is flexible enough to be applied in several ways depending on the system-on-chip to which it is added.

III. ESTIMATION METHOD

Typical circuit design is based on worst-case process variability conditions to ensure circuit functionality in various process corners. This has as drawback that the circuit is bigger, is power hungry and it is much more difficult to reach the desired specs. Thus, it would be better to choose simply a more “relaxed” design condition. Even though extensive research [15-18] has been done to estimate the various errors in different ADC architectures, use of a dedicated sensors for analysis of multi-step ADC to estimate parameter variations have been negligible. Statistical data extracted through the DLPM measurements allows us to characterize current process variability conditions (process corners) of certain parameters of interest, enabling the optimized design environment.

Consider the classical problem of estimating data from the vector of observations $x_i \in X$, where the hidden state $y_i \in Y = \{1, \dots, c\}$ are assumed to be realizations of random variables which are independent and identically distributed according to the $p_{XY|\theta}(x, y|\theta)$. The parameters $\theta \in \Theta$ involves parameters (μ_y, Σ_y) , $y \in Y$ of Gaussian components and the values of the discrete distribution $p_{Y|\theta}(y|\theta)$, $y \in Y$. The input set T_{XY} is given by $T_{XY} = \{(x_1, y_1), \dots, (x_b, y_b)\}$. To estimate data, widely employed method in statistics is the method of maximum likelihood (ML) defined as

$$\theta^* = \arg \max_{\theta \in \Theta} \sum_{i=1}^l \log p_{XY|\theta}(x_i, y_i | \theta) \quad (1)$$

When a measured parameter distribution on-chip (Figure 6) is derived, next step is to update high and low limit values by adjusting the support vector machine (SVM) classifier [4-5] (Figure 7) in the corresponding functional test specs of the device under test.

Figure 6: Contour plot of the distribution function of multiple runs of DLPM and DUT measurements derived through the Maximum-Likelihood method.

Let $f: X \subseteq \mathbb{R}^n \rightarrow \mathbb{R}$ be a discriminant function trained from the data T_{XY} . The parameters θ of a *a posteriori* distribution $p_{Y|F\theta}(y|f(x), \theta)$ of the hidden state y given the value of the discriminant function $f(x)$ are estimated by the maximum-likelihood method

$$\theta = \arg \max_{\theta'} \sum_{i=1}^l \log p_{Y|F\theta}(y_i | f(x_i) | \theta') \quad (2)$$

Obtaining optimum estimates through ML method thus involves two steps: 1) computing the likelihood function; 2) maximization over the set of all admissible sequences. To evaluate the contribution of random parameters $\theta = (\lambda, \eta, \gamma)$, analysis of the likelihood function require computing an expectation over the joint statistics of the random parameter vector, a task that is analytically intractable. Even if the likelihood function can be obtained analytically off line, however, it is invariably a nonlinear function of θ , which makes the maximization step (which must be performed in real time) computationally infeasible.

Figure 7: Fitting a posteriori probability to the SVM output [4-5].

In such cases, the expectation-maximization (EM) algorithm [9-10, 19-22] may provide a solution, albeit iterative (and possibly numerical), to the ML estimation problem. It has been found in most instances that the EM algorithm has the

advantage of reliable global convergence, low cost per iteration, economy of storage, and ease of programming [19]. The EM algorithm builds a sequence of parameter estimates $\theta^{(0)}, \theta^{(1)}, \dots, \theta^{(n)}$, such that the log-likelihood $L(\theta^{(n)} | T_{XY})$ monotonically increases, i.e., $L(\theta^{(0)} | T_{XY}) < L(\theta^{(1)} | T_{XY}) < \dots < L(\theta^{(n)} | T_{XY})$ until a stationary point $L(\theta^{(n-1)} | T_{XY}) = L(\theta^{(n)} | T_{XY})$ is achieved. In each iteration, two steps, called E-step and M-step, are involved. In the E-step, the EM algorithm determines the expectation of log-likelihood of the complete data based on the incomplete data and the current parameter θ

$$Q(\theta | \theta^{(n)}) = E(\log p(X, Y | \theta) | X, \theta^{(n)}) \quad (3)$$

In the M-step, the algorithm determines a new parameter maximizing Q

$$\theta^{(n+1)} = \arg \max_{\theta} Q(\theta | \theta^{(n)}) \quad (4)$$

The EM algorithm makes use of the log-likelihood function for the complete data in a two-step iterative procedure which under some conditions converges to the ML estimate given in (1) [9,22]. At each step of the EM iteration, the likelihood function can be shown to be non-decreasing [9,22]; if it is also bounded (which is mostly the case in practice), then the algorithm converges.

EM Algorithm

Initialization

- Initialize the data set $T_{XY} = \{(x_1, y_1), \dots, (x_b, y_b)\}$
- Initialize the parameter $\theta^{(0)}$

Data collection

- Collect N samples from the DLPMs

Update parameter estimate

1. Calculate $Q(\theta | \theta^{(n)}) = E(\log p(X, Y | \theta) | X, \theta^{(n)})$ – E step
 2. Re-estimate θ by maximizing the θ -function $\theta^{(n+1)} = \arg \max_{\theta} Q(\theta | \theta^{(n)})$, estimate mean and variance – M step
 3. Increase the iteration index, n
 4. Stop when a stationary point $L(\theta^{(n-1)} | T_{XY}) = L(\theta^{(n)} | T_{XY})$ is found.
-

IV. TEST RESULTS

A prototype ADC converter with dedicated sensors is fabricated in standard single poly, five metal 0.09- μm CMOS with the core area of 1.4 mm^2 . Influence of the coarse ADC offset on the coarse and mid quantization and the transfer characteristics is illustrated in Figure 8. The offset errors introduce transition position error that is easily spotted since the transitions do not coincide with the equally spaced vertical grid. The amplified difference between the input data and output of the converter encompass a scale wider than resolvable by the flash. Outside the dynamic range, the converter is bound to plus and minus one. The impact of transition position errors is easily spotted producing a number of missing codes or strong DNL errors. If the dynamic range of the converter is extended, the impact of the transition position errors will be substantially attenuated. There are no missing codes, although some DNL errors will still be present as shown in Figures 9 - 11. As shown in Figure 12, parameter variation effects of 95 DLPMs fall inside the discrimination window, while 45 results are characterized as faulty ones. In practice,

repetitive single-DLPM measurements are performed to minimize noise errors; the number of measurements depends upon the test time budget. Each measurement is weighted depending upon the DLPM spatial position and its corresponding matching structure in the circuit under test. In general, it holds that measurements of DLPMs spatially closer to their matching structures have a greater weight than measurements of other non matching DLPMs. In other words, the farther the structure from its matching DLPM is, the lower the assigned weight is. The estimation of the parameters based on the EM-algorithm is illustrated in Figures 13-16. The ground truth model (Figure 13) is a Gaussian model with two univariate Gaussian components based on DLPM and Coarse ADC DNL measurements. The plot of the log-likelihood function $L(\theta^{(n)} | T_{XY})$ with respect to the number of iterations is visualized in Figure 14. Finally, in Figures 15 and 16, mean μ and variance σ of decision stage offset errors (λ), stage gain errors (η), and errors in the internal reference voltages (γ) are estimated.

V. CONCLUSIONS

With the use of dedicated sensors, which exploit knowledge of the circuit structure and the specific defect mechanisms, we facilitate early and fast identification of excessive process parameter variation effects at the cost of at maximum 10% area overhead. The sensors allow the readout of local (within the core) performance parameters as well as the global distribution of these parameters. The flexibility of the concept allows the system to be easily extended with a variety of other performance sensors. The implemented maximum-likelihood method and adjusted support vector machine classifier allow us to guide the test with the information obtained through monitoring process variations. Employed expectation-maximization (EM) algorithm for estimation of the selected performance figures offers maximum likelihood estimates of parameters in probabilistic models, where the model depends on latent variables.

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Figure 8: Coarse and Mid ADC quantization points.

Figure 9: Worst-case DNL curve of the Coarse ADC measured from the sample pool.

Figure 10: The ratio of the code density test and code density plot of the ideal analog sine wave input.

Figure 11: Coarse ADC DNL histogram estimated from hundred samples.

Figure 12: DLPM histogram estimated from hundred and forty samples.

Figure 13: Using the EM-algorithm for ML estimation.

Figure 14: Log-likelihood with respect to the number of iterations of the EM.

Figure 15: Estimating λ , η , $\gamma - \mu$ values with respect to the number of iterations of the EM.

Figure 16: Estimating λ , η , $\gamma - \sigma$ values with respect to the number of iterations of the EM.