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Multipath Routing in a Fully Scheduled Integrated Optical Switch Fabric

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Abstract A compact and efficient control plane has been implemented to demonstrate multipath routing for a twenty-electrode photonic integrated circuit with round-robin scheduling. A single slot clock with 3.2 μ s packet period dynamically cycles connections between all input and output ports.

Introduction

Fast reconfigurable optical interconnects are set to play an increasingly important role in high-capacity data links. System level demonstrations, such as DAVID¹, Data Vortex² and OSMOSIS³, have enabled massive bandwidth and high connectivity for switched networks. However, the use of discrete photonic components incurs losses, delays, size and control plane complexity. Considerable photonic integration is now required.

Evaluation of photonic integrated circuits (PICs) has so far been predominantly limited to device level characterization⁴⁻⁶. Full routing control still represents a challenge, due to the large number of electrodes and optical ports requiring high-speed inputs and outputs in a very restricted area.

In this work, the first full routing control protocol implemented on a photonic integrated circuit is demonstrated. We abstract the photonic complexity with a logical control plane which now requires only a single digital slot clock input. The easy-to-interface high-speed electronics performs round-robin scheduling for the first demonstration of multipath routing on a PIC.

Switch Fabric

The experimental control plane to demonstrate multipath data routing is schematically shown in Fig. 1. A dedicated scheduler is designed to enable rotating priority (round-robin) path arbitration. A Johnson decade counter provides the cyclic counting and buffers synchronise and condition the signals for the nanosecond speed current drivers. For convenience, the clock signal at the input of the scheduler is derived from the pulse pattern generator used for data generation. Arbitrary and aperiodic slot clock signals are also feasible. A level control block, shown at the top right of Fig. 1, defines the current signals to each of the twenty electrodes.

Fig. 1: Sophisticated switch fabric highlighting the PIC and its control plane.

Levels are set manually, but self-calibration is also practicable⁷. Electronic switching times of 7 ns are expected from the HC/HCT logic family used. The PIC is shown at the bottom of Fig. 1. The four input and four output optical ports are shown on the left and right side, respectively. The PIC is epoxy-bonded to a copper mount and its operation temperature is fixed at 15°C by a thermo-electric controller. Light is coupled into the circuit with a fibre lens array with 250 μ m pitch, and is then coupled out through individually manipulated lensed fibres. The input wavelength is set at the 1600 nm gain peak and modulated with 10 Gb/s data. The polarization state is aligned. The output optical signal is filtered with a 0.22 nm bandwidth grating for broadband noise rejection for the bit error rate measurements. No external optical amplifiers are used.

Integrated 4×4 Switch

The circuit design is shown in top view in Fig. 2. A four input, four output broadcast-and-select integrated semiconductor optical amplifier (SOA)

switch is fabricated from quantum well active epitaxy. The total area of the integrated circuit measures only $4 \times 1 \text{ mm}^2$, presenting a very high density of optical waveguides and electrodes. This twenty-electrode circuit provides sixteen paths addressable by biasing the appropriate gate SOAs. These are the longest electrodes in the middle of the circuit in Fig. 2. The width and

Fig. 2: Broadcast and select SOA switch, with mask details of input and output shuffle and split networks.

the length of the gate SOA waveguides are $3.0 \mu\text{m}$ and 2.1 mm , respectively. These are adiabatically tapered for mode control and allow improved gain. On-state operating currents are in the range from 120 to 150 mA. Off-state currents are set to 0 mA. Miniaturized shuffle and split networks at the left and right side of the circuit provide the broadcast and combine functions. Mask details are shown as insets in Fig. 2. The shuffle and split networks include two stages of splitters with waveguide crossings. The combiners and splitters are placed in the isolated regions between the SOAs and the shuffle networks and are therefore unbiased. Fibre-to-fibre gain is in the range from -22.5 to -16.6 dB, and it is limited by facet reflections for twelve of the sixteen paths. Therefore the on-chip gain is believed to compensate most of the losses due to the splitters and combiners. The remaining loss is predominantly due to the fibre-to-chip coupling. Antireflective coatings will allow significantly higher gain. There is spectral evidence of waveguide damage for the four lossy paths which are untested in this work.

Photonic Layer Assessment

The crosstalk power assessment is carried out by gating one path at a time and monitoring the power from the remaining outputs. The gate current level required for on-state operation is set to 140 mA for each measurement. The total bias current for the input and output electrodes,

and the input and output shuffle networks is fixed at 240 mA. This injected current is shared between all the paths and could be removed with an active-passive integration scheme. Once the path is selected, the ratios between the corresponding output power and the crosstalk powers at the adjacent outputs are evaluated. The crosstalk power levels are plotted as a function of the selected path in Fig. 3 for an input power of +2.8 dBm. The signal power

Fig. 3: Path dependent crosstalk.

spectral peaks are compared. With the exception of path 4-1, the crosstalk values are within the range from -29.1 to -42.5 dBm.

Bit error rate measurements are performed for data routed over a typical path of average length and are displayed in Fig. 4. A 10 Gb/s pseudo random bit sequence of $2^{31}-1$ bits is routed through this path. Static power penalty measurements are performed using a Finisar receiver preceded by a variable optical attenuator. Error rate measurements exhibit a logarithmic relationship suggesting noise limited operation. A power penalty of 2.7 dB is estimated. An instability in the tunable laser is

Fig. 4: BER measurements for data routed from output 2 to input 3.

observed and this may also impact BER measurements. The optical signal to noise ratio is found to be -31.3 dB/0.07 nm.

Multipath Round-Robin Protocol

The round robin scheduling is implemented to show multipath routing assessment for the PIC. Fig. 5 shows the experimental arrangement. The

optical data signal is broadcast to all the switch inputs with a fibre splitter network and a fibre lens array, as shown in Fig. 5. Each output is assessed sequentially by scanning the output fibre lens. Paths are cycled in time through

Fig. 5: Schematic of multipath routing set-up.

synchronized electronic control of the SOA gates. The dynamic routing of the twelve viable paths allows the full verification of all the ports for the sub-system in use. Fig. 6 shows the time

Fig. 6: Time traces of the multiple routing from all populated inputs to output 1, 2, 3 and 4.

traces of the routed data. For output 1, each packet is routed in order from input 4, 3, 2 and 1, and back to input 4. Operation is also confirmed for outputs 2, 3 and 4 in Fig. 6. The optical signal is modulated with 10 Gb/s $2^{15}-1$ long packets of approximately 3.2 μ s duration time. These are interleaved with 150 and 350 ns guard band durations. The specified guard band durations enable the visibility for the packets traces for two different time-scales. Good equalization of the output powers from the different paths is required to recover data at the receiver. The maximum input power difference at the receiver is estimated to be better than 2.0 dB. The time traces shown in Fig. 6 for all the outputs show well resolved data packets.

The square signal that appears in Fig. 6c is the clock signal at the input of the scheduler. This is the only external signal required to control the full switch subsystem. By investigating the switching transition, the guard band duration may be reduced to 5 ns without incurring visible errors in the sampled time traces.

Conclusions

Multipath routing using round-robin protocol has been demonstrated for the first time for a twenty-electrode integrated switch. The control plane is implemented to dynamically route between four inputs and four outputs with 3.2 μ s duration slot clock. The total functionality of the chip has been demonstrated with a single clock signal input.

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References

- 1 L. Dittman et al., Proc. PIS'01 (2005).
- 2 O. Liboiron-Ladouceur et al., J. Lightwave Technol. **26**, 1777 (2008).
- 3 R. Luijten et al., OFC'09, OTuF3, Invited (2009).
- 4 A. Albores-Mejia et al., Electronic Lett. **45**, 313 (2009).
- 5 H. Wang et al., ECOC'09, 6.2.3 (2009).
- 6 C.P. Larsen et al., J. Lightwave Technol. **15**, 1865 (1997).
- 7 I.H. White et al., J. Optical Network. **6**, 180 (2007).