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A novel temperature and disturbance insensitive
DAC calibration method

Elbert Bechthum, Georgi Radulov, Arthur van Roermund
Eindhoven University of Technology, Department of Electrical Engineering, The Netherlands
Email: E.Bechthum@tue.nl

Abstract—This paper presents a new foreground DAC calibration method that is insensitive to temperature fluctuations and on-chip disturbances.

In the proposed current cell, the same number of unit transistors is always used, guaranteeing matched response for all current cells. These transistors are divided in two groups: a fixed group and a configurable group. The unit transistors in the configurable group can be interchanged with additional redundant unit transistors, such that the mismatch errors of the configurable group compensate the mismatch errors of the fixed group. Together they generate the needed output current. Thus all current cells feature matched temperature coefficients and dynamic response. For an exemplary 6+6 bits segmented current steering DAC, the expected 99% yield INL improves with almost 3 bits while using only 30% additional unit transistors.

I. INTRODUCTION

The static DAC linearity, e.g. INL (Integral Non Linearity), is mainly limited by the finite matching of the DAC current source transistors. The mismatch between identically sized and biased transistors is given in (1) [1].

\[
\frac{\sigma_I}{I} = \left( A_\beta + \frac{4A_{VT}^2}{(V_{GS} - V_T)^2} \right) \frac{1}{2W_L} \tag{1}
\]

Using large devices (W·L) reduces the random mismatch, but increases occupied area and hence increases the systematic mismatch and degrades high-frequency performance. The dynamic linearity, e.g. SFDR (Spurious Free Dynamic Range), is usually limited by the achieved static linearity, and further reduced at high speeds by the parasitic capacitances and resistances of the current source transistors. Therefore, to achieve high linearity at high speed, both small and accurate current source transistors are necessary.

To improve the DAC static linearity and to reduce the size of the DAC current source transistors, calibration of the mismatch errors of the DAC current sources can be used. An example of calibration in a Current Steering DAC (CSDAC) is shown in Fig. 1 [2]. For an analysis of different correction methods, see [3].

Two types of calibration strategies can be distinguished: foreground and background calibration. Background calibration is continuously running while the DAC is actively used [4]. It suffers from increased power consumption during operation and the output signal may be polluted by spurious emissions of the calibration activities. Foreground calibration is only active when the DAC is idle, e.g. at startup, and hence avoids the aforementioned disadvantages. However, discrepancies in the environment between calibration and use, e.g. temperature or supply voltage, can reduce the advantages of the calibration. In addition, the advantages of the existing calibration methods also reduce at high speeds [4].

The proposed foreground calibration method uses identical unit transistors in both the current source and the CalDAC to guarantee matched responses to disturbances and temperature variations. The current cell is calibrated by combining unit transistors with opposite mismatch within one current cell such that their combined mismatch is minimized.

The next section explains the temperature and disturbance sensitivity of the conventional calibration. In section III, a new CalDAC implementation and calibration algorithm is proposed which is insensitive to temperature variations and disturbances. Section IV shows simulation results.

II. TEMPERATURE AND DISTURBANCE DEPENDENCE

An exemplary schematic of a CSDAC using CalDAC calibration is shown in Fig. 1, which is used in [5] and [6]. In the current cell, named Calibrated Unit Element (CUE), transistor \( M_1 \) is the main current source with output current \( I_{\text{main}} \). Due to process spreading and systematic mismatches, the value of \( I_{\text{main}} \) deviates from the nominal designed value \( \bar{I}_{\text{main}} \), i.e. for the n-th current source \( I_{\text{main,n}} = \bar{I}_{\text{main}} + I_{\text{error,n}} \). The CalDAC generates a correction current such that the output of the CUE \( I_{\text{cue,n}} \) equals the value of \( \bar{I}_{\text{cue}} \).

In the example of Fig. 1, the state of transistors \( M_{3,\text{off}} \) and \( M_{3,\text{on}} \) decides if the CUE output current is either used for the normal operation of the DAC or connected to the Calibration circuit and measured for calibration.

An exemplary implementation of a conventional CalDAC is shown in Fig. 2 [6], [7]. The main current source \( M_1 \) consists of \( M \) transistors. The CalDAC, consisting of transistors \( M_{\text{cal,1}} \) to \( M_{\text{cal,N}} \), adds the required correction current.
In the discussed conventional CUE, the mismatch of a main current source is compensated by the nominal value of the CalDAC output current, i.e. $I_{\text{cue,n}} = I_{\text{main}} + I_{\text{error,n}}$. $I_{\text{main}}$ and $I_{\text{error,n}}$ are set by temperature independent references, while $I_{\text{error,n}}$ is temperature dependent. Therefore, the temperature coefficient of $I_{\text{cue,n}}$ depends on the ratio between $I_{\text{cue,n}}$ and $I_{\text{error,n}}$. Fig. 4 shows the buildup of the output current of two exemplary CUEs. The CUEs are calibrated at $T = 25^\circ\text{C}$, but for $T \neq 25^\circ\text{C}$, the CalDAC calibration is not valid.

### A. Temperature response

In CMOS processes, the mismatch between the output current of identically biased transistors is given by (1). For high performance DACs, the main current source transistor is usually much larger than the feature size of modern CMOS processes. Thus, the current mismatch is dominated by the threshold voltage mismatch. This assumption is confirmed by measurements of an existing DAC implementation [8]. Fig. 3 shows the standard deviation of the output current of the 15 unary current cells. The mismatch clearly exhibits a square root dependence on the drain current, which is in conformance with (1) in combination with the drain current relationship of a MOS transistor in saturation, as shown by (2).

$$I_D = \frac{\mu C_{oX} W}{2L} (V_{GS} - V_T)^2$$  \hspace{1cm} (2)

At high temperatures, the mobility of the carriers ($\mu$) decreases. Usually, a temperature independent current controls the output current of the DAC current source transistors. Therefore, at high temperatures, $V_{GS} - V_T$ increases to compensate for the decreasing $\mu$. Together with the matching equation of (1), it is clear that when the temperature increases, i.e. $V_{GS} - V_T$ increases, the relative threshold mismatch decreases. Mismatch measurements of the existing DAC at high temperature confirm this analysis, see Fig. 3.

### B. Disturbance response

To quantify the temperature dependence, a simple transistor level simulation based on [6] is performed. Two calibrated CUEs with threshold voltage mismatch between each other are simulated over a temperature range of $-50^\circ\text{C}$ to $125^\circ\text{C}$. The temperature dependence of the CUEs output current difference, i.e. $error_{\text{low}} - error_{\text{high}}$, can be as large as 8 CalDAC LSBs, which is 1.3% of the CUE output current.

Thus, for foreground calibration, the INL degrades and also the SFDR worsens when temperature changes. This phenomenon is confirmed by INL and SFDR measurements of an existing DAC [8].

### III. Proposed New Calibration Method

To match the response of the correction hardware to temperature and on-chip disturbances, and hence extend the advantages of the foreground calibration, a new calibration method is proposed.

In the proposed CUE, the same number of unit transistors ($M$) is used in every CUE. These $M$ transistors are divided in two groups, $M - K$ unit transistors in the fixed group...
CALDAC made of $P=K+X$ units

which the Least Significant Bits (LSBs) are implemented using source is explained using a segmented DAC architecture, of described separately.

developed method can also be applied to a fully unary or binary implemented with unary coded current cells. Note that the current cells and the Most Significant Bits (MSBs) are coded DAC. Two different calibration methods are used for the mismatch of the configurable group transistors compensate the mismatch of the fixed group and together generate the desired output current.

A novel principle is the use of identical unit transistors for both the fixed group and the configurable group, sharing a common bias voltage, providing a matched response for every CUE in the DAC. Another novel concept is to compensate the mismatch of the fixed group of transistors in the current cell with the mismatch of the configurable group transistors, generating a temperature stable calibration.

A. Hardware

A schematic overview of the new CalDAC implementation is shown in Fig. 6. The $M-K$ main current source transistors provide the fixed current $I_{\text{main}}$. $K$ units in the group of $P$ unit transistors in the CalDAC are switched on to generate the correction current $I_{\text{cor}}$. The value of $X$ defines the added amount of redundant current sources with respect to the $M$-transistor intrinsic current cell. The value of $P$ is an indication of the added layout complexity, since every transistor in the CalDAC is controlled separately.

![Proposed CalDAC](image)

Fig. 6. Proposed CalDAC with common transistor dimensions and biasing

B. Algorithm

The algorithm to find the optimal correction for a current source is explained using a segmented DAC architecture, of which the Least Significant Bits (LSBs) are implemented using binary current cells and the Most Significant Bits (MSBs) are implemented with unary coded current cells. Note that the described method can also be applied to a fully unary or binary coded DAC. Two different calibration methods are used for the unary current cells and the binary current cells, which are described separately.

1) Unary current cells: The principle of the calibrating algorithm of one CUE is to select which transistors of the CalDAC should be switched on such that $I_{\text{cue}}$ is properly corrected. The first step in the algorithm is to sort the transistors in the CalDAC according to their output amplitude and then switch on $K$ of the highest amplitude transistors. Fig. 7 gives an example, where $M=8$, $K=3$ and $X=3$. The top figure shows the output amplitude of the unit transistors (which are named $a$-$k$), and gives the first step.

![Algorithm Diagram](image)

Fig. 7. Example of the calibration algorithm

The second step in the algorithm is to swap transistors between the on-group and the off-group until the total output current becomes less than the reference. The top diagram of Fig. 7 indicates the first three swap actions (named 1-3). The bottom diagram gives the resulting total output current of the CUE for the initial state (named 0) and after each swap action. The algorithm will stop after swap step 3, because the total output current is less than the reference $I_{\text{ref}}$.

For the calibration of the unary current cells, the reference consists of the sum of all binary current cells and one LSB current source as in [7]. Therefore, the binary current cells should be calibrated before the unary current cell calibration. The main hardware component necessary to implement the algorithm for the unary current cells is a comparator to sort the transistors and compare the reference and the CUE total output current. The algorithm can be realized as a simple Finite State Machine (FSM).

2) Binary current cells: The algorithm to calibrate the binary current cells is largely identical to the algorithm for the unary current cells. For the calibration of $N_{\text{LSB}}$ binary current cells in one DAC, $N_{\text{LSB}}$ reference currents are required, with a ratio of 2 between two successive references. Since exact current ratios are difficult to implement in the analog domain, the complete binary calibration algorithm is implemented in the digital domain. Therefore, all unit transistor currents are measured using an Analog to Digital Converter (ADC), and all transistor sorting, swapping and output current calculation can be done digitally. To be insensitive to gain and offset errors of the ADC, the main current source of the binary current cells is omitted ($M-K=0$). Instead, the current cell output current is constructed using the separately measured unit transistors of the CalDAC. The algorithm is insensitive to the ADC offset and gain error since all unit transistors share the same ADC
of 2 transistors, etc. Thus, the unary current cell has a weight of \(2^N_{\text{LSB}}\) LSB current cell consists of 1 transistor, the next current cell of 2 transistors, etc. Thus, the unary current cell has a weight of \(2^{N_{\text{LSB}}}\) LSB, and hence consists of \(M = 64\) transistors.

The necessary hardware to implement the binary current cell calibration is the ADC and a FSM. The ADC does not need to be fast or accurate and is implemented as a Successive Approximation (SAR) ADC \([6], [7]\) with 5 bits linearity.

All current cells are based on the same unit transistor. The Matlab model of a 6+6 (unary + binary) bits segmented DAC is required and 99% yield for the INL specification, the 99% yield INL values, with respect to 12 bits accuracy, are shown in Fig. 8. It is clear that using more transistors in the CalDAC results in more magnitudes lower than the conventional CalDAC, it is expected that the spurious emissions due to on-chip disturbances are significantly reduced.

V. Conclusion

The proposed novel calibration method overcomes the problems with the cell-dependent temperature coefficients of the Calibrated Unit Elements. Also the cell-dependent response to disturbances is reduced. Due to the reduction of these two cell-dependent responses, the spectral purity of the DAC output signal should be improved. The new calibration algorithm provides opportunities to improve the post calibration INL of a DAC. For an exemplary 6+6bits segmented current steering DAC, the expected 99% yield INL improves with almost 3 bits when using only 30% additional current cell area. The proposed new calibration method will obviate the need for background calibration, while also providing calibration advantages to high DAC speeds.

REFERENCES


