VDD ramp testing for rf circuits

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VDD Ramp Testing for RF Circuits

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Abstract

We present industrial results of a quiescent current testing technique suitable for RF testing. The operational method consists of ramping the power supply and of observing the corresponding quiescent current signatures. When the power supply is swept, all transistors are forced into various regions of operation. This has as advantage that the detection of faults is done for multiple supply voltages and corresponding quiescent currents, enhancing in this form the detectability of faults. We found that this method of structural testing yields fault coverage results comparable to functional RF tests making it a potential and attractive technique for production wafer testing due to its low cost, low testing times and low frequency requirements.

1. Introduction

Testing is becoming a substantial barrier to continued RF IC cost reductions because of the additional complexities required by new standards -including multi-band compatibility, higher linearity, lower bit-error rate, and long battery life. BER testing is in fact a preferred functional test method in RF systems [1]. Typical test costs as a percentage of the manufacturing cost are commonly low for most digital products but for RF devices it is projected that this percentage will increase to 50%¹. The overall cost of an RF system consists of manufacturing, testing (wafer sort and final testing) and packaging. The traditional test flow for dc wafer testing is mainly digital. It uses cheap testers and prunes away defective devices. Typically, in this flow RF is bypassed due to the high cost of RF testers. Unfortunately, defective devices in the RF path are packaged before they are thrown away resulting in a significant loss if we consider that packaging can represent 30% of the overall cost. Current test practices are expensive, among other reasons, because of the required tester infrastructure, long test times, cumbersome test preparation, lack of appropriate defect and fault models, and lack of standardized test methods.

The difference between functional testing and structural testing is that the ATPG in structural testing is derived from the circuit implementation rather than from the circuit specification. Given that typically the

transistor count of analog circuits is not large, structural testing can benefit from inductive fault analysis techniques (and alike), e.g. layout inspection tools to map defects to faults [2-4]. In this way the ATPG is targeted to a set of realistic faults. Additionally, it is possible to derive figures of merit such as defect and fault coverage to measure the ATPG effectiveness.

Structural testing focuses on the development of dc and transient testing of analog circuits [5-7]. In transient testing, the circuit under test is excited with a transient test stimulus and the circuit response is sampled at specified times to detect the presence of a fault [8, 9]. The transient waveform can be formed from piecewise linear segments that excite the circuit in such way that the sensitivity of the fault to the specific stimulus is magnified. These waveforms can have a periodic shape, or even arbitrary shapes or as recently proposed they can have a binary shape with distinct duty cycles [10]. It is also possible to structurally test the circuit by testing its dc conditions, e.g. by inspecting quiescent currents [11,12].

A dc-based analog test pattern generator can be derived by appropriately sweeping the power supply and then observing the corresponding behavior of the supply current or any other observable node. This power supply ramp method is a technique developed in the early 90s that showed potential for detecting defects [13]. In this paper we explore further this technique and evaluate its use as a structural test capable of substituting or complementing conventional RF tests. In particular, we carry out an extensive study benchmarking functional and structural fault coverage. The underlying testing approach relies on a defect oriented test analysis that takes into account the spread of the process as well as the presence of resistive (not only catastrophic) defects. We evaluated the power supply ramp technique on a standalone Low Noise Amplifier (LNA). In the next sections the reader will find a description of the LNA, test methodology, fault coverage and measurement results, and conclusions about the work.

2. Low Noise Amplifier

The first stage of a receiver is typically an LNA whose main function is to provide enough gain to overcome

¹ ITRS projections

the noise of subsequent stages (such as a mixer). Besides providing this gain while adding as little noise as possible, an LNA accommodates large signals without distortion, and frequently must also present a specific impedance, such as 50Ω or 100Ω , to the input source. This last consideration is particularly important if a passive filter precedes the LNA, since the transfer characteristics of all filters are quite sensitive to the quality of the termination.

2.1 LNA Jargon

Let us first present some definitions and their meaning about the various parameters used to evaluate the LNA.

Gain: Voltage or power gain ratio between output and input level, expressed in dB.

1dB compression point: expressed in dBm, the maximum output power for which the gain is 1 dB less than the linear extrapolation of its value in weak signals.

IP3: The third-order intercept power point is used as a parameter to describe the intermodulation performance of an RF design. If 'A' is the difference in the power level between the main signal (frequency f_0 or f_1) and the third generated intermod (frequency $2f_0-f_1$ or $2f_1-f_0$), then the input third order intercept point IP3 is defined as

$$\text{Input IP3 (dBm)} = \text{Pin (dBm)} + A/2 \quad (1)$$

Noise Figure: NF is simply the noise factor F expressed in dBs. The noise factor is a measure of the degradation in signal to noise ratio that a system introduces. The larger the degradation, the larger the noise factor. If a system adds no noise of its own then the total output noise is due entirely to the source, and the noise factor is therefore unity.

$$NF = \frac{\text{Total Output Noise Power}}{\text{Output Noise due to Input Source}} \quad (2)$$

2.2 LNA Specs

The schematics of the LNA are shown in Figure 1. The LNA uses a power supply voltage $V_{DD}=1.8V$, and a common voltage $V_{com}=0.8V$ (common voltage at the input and output).

The relationship between the input signal amplitude, A_{in} , and the power P_W in watts delivered by the signal generator and its source impedance R_S is

$$A_{in} = (2 R_S P_W)^{1/2} \quad (3)$$

We can also define the power P_{rf} delivered by the source and its impedance in dBm by

$$P_W = 10^{(P_{rf}/10)}/1000 \quad (4)$$

Figure 1. Low Noise Amplifier

The input frequency f_0 is 2.45GHz and the LNA's input and output impedances are matched to the source R_S and load R_L impedances, respectively. Simulations show that the LNA is linear for $-70\text{dBm} < P_{RF} < 0\text{dBm}$. This means that the input power must be $10^{-10}\text{W} < P_W < 10^{-3}\text{W}$. The LNA seems to be an attenuator. However, when the LNA is used in a complete receive chain, this receive chain will indeed have a gain. In this case, this LNA merely acts as a buffer and driver towards the mixer. The LNA provides isolation between the I and Q paths, to prevent that the two mixers in the receive chain influence each other.

A transient simulation was done to simulate the 1dB compression point and the IP3. To simulate the IP3, the input signal must have two frequencies f_0 and f_1 , such that f_1-f_0 is smaller than f_0 . In our case, the input signal E_g has been defined as:

$$E_g = \text{tone0} + \text{tone1} \quad (5)$$

with

$$\text{tone0} = A_{in} \sin(2\pi f_0 t) \quad (6a)$$

$$\text{tone1} = A_{in} \sin(2\pi f_1 t) \quad (6b)$$

$$A_{in} = (2 R_S P_W)^{1/2} \quad (6c)$$

$$P_W = 10^{(P_{rf}/10)}/1000 \quad (6d)$$

where P_{rf} is the power delivered in dBm. f_0 is taken equal to 2.4GHz and f_1 is taken equal to 2.5GHz, which means that the third intermod generated frequencies are $2f_0-f_1 = 2.3\text{GHz}$ and $2f_1-f_0 = 2.6\text{GHz}$. P_{RF} was swept from -70dBm to 0dBm and the magnitude of the first and the third harmonics of the output $V_{on}-V_{op}$ were measured in dB. Figure 2 gives the method and results to calculate the 1dB compression point. This method is based on the extension of the fundamental transfer line and on the extension of the fundamental transfer line -1dB .

Figure 3 gives a method to calculate the IP3 value. This method is based on the extension of the fundamental transfer line and the third order two tones intermodulation transfer line. We noticed that the simulations of the IP3 and the 1dB compression point take more than one hour of cpu time in an HPPA7300 because of the required high accuracy in combination with the sweep statements. An AC simulation, using the two-port model, has been run using PSTAR (a

Philips proprietary Spice-like simulator) to simulate the noise factor and the noise figure of the LNA. Table 1 gives a general overview of the specs of this LNA.

Figure 2. 1dB point compression value ($R_S=R_L=100\Omega$)

Figure 3. IP3 value ($R_S=R_L=100\Omega$).

Table 1. LNA specs

Parameter	$R_S=R_L=50\Omega$	$R_S=R_L=100\Omega$
Voltage Gain	-29.586dB	-23.595dB
Noise figure	18.443dB	15.512dB
1dB compression	-11.666dBm	-14.414dBm
IP3	2.249dBm	-0.722dBm

3. Power Supply Ramp Test Methodology

The utilized technique is illustrated in Figure 4. It basically consists of ramping up the power supply in discrete steps such that a current signature is generated. When the power supply is discretely ramped up, all transistors in the circuit pass through several regions of operation, e.g. subthreshold (region A), linear (region B), and saturation (region C). The advantage of a transition from region to region is that defects can be detected with distinct accuracy in each of the operating regions, e.g. a bridge drains a distinct current depending upon whether the transistors are saturated or in the linear region. This method provides, thus, multiple observation points. It is simple; it is not a functional test and can easily be implemented in any tester. Observe that the typical

current signature of this analog circuit follows a *tanh* function. It is expected that a defective device will present an abnormal current signature, e.g. a signature that deviates from the golden *tanh* form. Hence, a simple pass/fail test procedure can be put in place by comparing signatures. If fault diagnosis is desired, a fault dictionary database can be built and then the tested current signatures can be matched against signatures in this database [13].

Figure 4. Power supply ramp with corresponding quiescent current signature

For the LNA under test, the power supply was ramped in discrete steps without paying attention to the speed of the ramp. We foresee, that this will not be the general case for all sorts of circuits, particularly for circuits in which dynamic responses are quite important.

Figure 5 shows the LNA's simulated current signature against the power supply voltage sweep and under statistical process variations. The statistical process variations account for inter and intra die variations. Since structural testing assumes that the circuit is properly designed and that it can sustain process variations, one could safely assume a tolerance band for the current signature.

Figure 5. LNA current signatures with process spread.

In other words, any tested signature that falls within this band implies that the circuit is operating correctly. This simple assumption allows us to take into account the effect of process shifts. Assuming that we have a

functional correct design, parametric faults could be identified through current signatures that are slightly out of the tolerance band. For this particular design we can see that for voltages greater than 1V there is a wide I_{DDQ} band. Figure 6 and Figure 7 show the functional behavior of the LNA as a function of the power supply ramp. In both plots we see that the LNA presents a typical behavior for $V_{DD} > 1V$. Observe that process shifts have a negligible effect on both the voltage gain and the noise figure. The voltage gain was simulated at 2.45GHz.

Figure 6. LNA gain vs. power supply ramp

Figure 7. LNA noise figure vs. power supply ramp.

Figure 8 shows a correlation of quiescent current against voltage gain for various power supply values. This plot is useful for identifying I_{DD} limits such that the corresponding voltage gain is within specs. Thus, the power supply method can also be used to capture parametric faults that could be outside the limits or close to the edges using this correlation figure.

Figure 8. Correlation of I_{DDQ} against voltage gain for various power supply voltages.

4. Defect Oriented Test Flow

Our defect-oriented test approach starts at the layout level, over which a vast number of defects is sprinkled in a random way. The size and the probability of the sprinkled defects are defined by their defect density distribution. After that, a defect analysis is performed. It has to be determined whether a defect causes a fault or not. All defects causing faults between two specific net numbers are grouped together and stored in a database. In order to investigate the realistic set of faults we utilized the Carafe IFA tool to introduce defects in the layout. Carafe works by widening and shrinking the layout conducting lines and finds possible intersections of conductors in different process planes to determine how a spot defect of a certain size can affect the layout. Therefore, a list of faults based on the layout sensitivity is generated.

As a start of the fault simulation with the use of the analog circuit simulator, a golden or defect free simulation is performed. The results of this simulation will later on be used as a reference. Next, the faults are introduced and simulated sequentially. The defects causing bridges are modelled as resistors between two nets. The results of the fault simulation are stored in a database and compared with the golden simulation. By providing test limits to the database, it can be determined which faults were detected and which were not. The undetected faults are subject of further research. The simulations were done in DOTSS which is a Philips proprietary environment for fault simulation, testing and grading. This flow is illustrated in Figure 9.

Figure 9. Defect-oriented test methodology.

A total of 147 bridges were detected from this inductive fault analysis. Figure 10 shows the current signatures for the first 50 ones. Actually, this figure illustrates the potential of the method. One can see signatures that are completely different from the golden one. One can also see some signatures whose quiescent values are comparable to the golden's for $V_{DD} > 1V$, but that have entirely different values for

$V_{DD} < 1V$. Conventional techniques that focus on one observation point only, say at nominal V_{DD} , would fail to detect the latter kind of faults. In summary, we have distinct fault observability for each power supply voltage.

Figure 10. Current signatures for the first 50 bridges.

5. Efficiency of Power Supply Ramp Method

Let us consider three power supply intervals, namely $0V < V_{DD} < 0.5V$, $0.5V < V_{DD} < 1V$, and $1V < V_{DD} < 2V$. Let us investigate now how many faults can be uniquely detected in each region. Figure 11 shows the fault distribution per V_{DD} interval. The pie chart shows that from all bridges 17 were undetected and that 67 can be detected in any power supply region. Interestingly enough, there are 10 faults that can be detected *only* in the interval $0V < V_{DD} < 0.5V$ and so on. This proves the usefulness of sweeping the power supply for detecting faults as these faults would not have been detected at nominal V_{DD} .

Figure 11. Number of detected faults per V_{DD} interval.

How easy is it to detect a given fault at distinct V_{DD} values depends on how much the faulty I_{DDQ} deviates from the golden I_{DDQ} at the preselected V_{DD} value. Figure 12 shows this “sensitivity” for the first 50 bridges. The horizontal axis shows the power supply voltage and the vertical axis shows the normalized sum of the absolute current difference between the faulty and golden I_{DDQ} values. This plot shows that it is easier to detect faults at lower power supplies. Of course, this sensitivity results will vary depending upon the circuit under test.

6. Additional dc-voltage Test

These tests are based on a measure of the dc voltage at the outputs of the LNA. According to target specs, these nodes have to keep the common output voltage

at 0.8V. The injection of a fault (bridge) will thus increase or decrease this value on one or both nodes. These tests are applied when the LNA is operating as an amplifier. The values that are used for V_{DD} range from 1V to 2V. The number of the tests is equal in this case to: $2 \cdot 11 = 22$ DC tests. The electrical test limits are set at $\pm 50mV$ according to the golden value (0.8V).

Figure 12. Test sensitivity of power supply ramp method

7. Structural vs. Functional Fault Coverage

Let us now inspect the fault coverage obtained through the power supply ramp method and through evaluation of the LNA’s gain and noise figure. Fault coverage is defined as the ratio of detected faults over the whole set of faults. A weight can be given depending upon whether the faults are ranked or not. The unweighted fault coverage results of the power supply ramp method are shown in Table 2 for a resistive bridge of 100Ω . The current flowing at $V_{DD} = 0V$ is because the LNA biasing current is supplied from an independent source giving the possibility of testing the biasing circuit independent from the core supply of the LNA. Also, the LNA’s input common mode voltage is independent of the power supply and is kept fixed while stepping the power supply. The fault coverage of the voltage gain and Noise Figure evaluated at $V_{DD} = 1.8V$ are 75% and 83%, respectively. Interestingly enough, the fault coverage of the power supply ramp method is better than when the LNA’s gain and Noise Figure are evaluated. The Noise Figure fault coverage gives better results because each bridge is evaluated as a resistor of 10Ω which introduces additional noise to the LNA.

Table 2. Fault coverage of power supply ramp method

VDD	Low limit (A)	High limit (A)	Coverage (%)
0	5.51E-08	2.96E-07	40.136
0.2	6.63E-06	1.46E-05	46.259
0.4	2.70E-05	3.09E-05	53.061
0.5	3.90E-05	4.95E-05	52.381
0.6	6.34E-05	7.64E-05	48.980
0.7	9.39E-05	1.17E-04	47.619
0.8	1.42E-04	1.77E-04	51.020
0.9	2.08E-04	2.53E-04	55.782
1.0	2.57E-04	3.10E-04	58.503
1.2	2.60E-04	3.25E-04	68.707
1.4	2.61E-04	3.27E-04	70.748
1.6	2.62E-04	3.28E-04	68.027
1.8	2.62E-04	3.29E-04	68.707
2.0	2.63E-04	3.29E-04	72.109

Notice that for this LNA, the fault coverage of the power supply ramp method is best when $1.2V < V_{DD} < 2V$. The combined fault coverage of the three methods is about 95%. When the additional dc-voltage test is included we obtain a 100% fault coverage. Fault coverage comparisons are shown in Figure 13 where

- Total1 = FC(IDD, GAIN, NF) 94.6%
- Total2 = FC(IDD, GAIN, NF, DC-Voltage) 100%
- Total3 = FC(IDD, DC-Voltage) 93.9%
- Total4 = FC(NF, GAIN) 85.7%

Worth noting is that the fault coverage of the power supply ramp is even better than the combined fault coverage of the gain and Noise Figure. Using the DOTSS tool it is possible to carry out a test optimization, .e.g. to choose a combination of tests, say gain followed by Noise Figure followed by the power supply ramp test, etc. The advantage of using this test optimization in the power supply ramp method is that it is possible to constrain the number of current measurements to a couple of V_{DD} points. As we saw from Figure 13 it is possible to achieve 100% fault coverage if both functional and structural tests are executed. This can be achieved with only 5 tests as shown in Figure 14. Now, when no functional tests are used the fault coverage of this LNA is 93.9%. Test optimization results show that it is possible to have this fault coverage using only 4 tests as shown in Figure 15.

Figure 13. Comparison of structural and functional fault coverage for bridges

Figure 14. Optimized set of functional and structural tests

Figure 15. Optimized set of only structural tests

Let us reason a bit more about these results. There are basically two lines of thinking; one is fault coverage and the other is test cost. If a low test cost is desired, then the power supply ramp method along with the dc-voltage test is sufficient since its fault coverage is comparable to the functional fault coverage, see Total3 and Total 4. On the other hand, if a better than functional fault coverage is needed, then the dc tests are good enhancements for the conventional functional tests; see Total 4 and Total2.

The Venn diagram in Figure 16 shows more details about the fault coverage of the power supply ramp, Gain, and NF test methods. We notice particularly that

- 8 faults are still undetected by all three tests.
- 13 faults are detected only by the IDD tests.
- 2 faults are detected only by the gain tests.
- 1 fault is detected only by the Noise Figure tests.

Figure 16. Venn diagram of test methods

The previous simulations have been run on bridges with a resistance of 100Ω. The goal of this analysis is to study also the impact of weak resistive bridges. An increase in bridging resistance reduces the quiescent current, hampering, in a way the sensitivity of the power supply ramp method. The corresponding results are displayed in Figure 17. We notice, though, that the fault coverage of the combined dc tests outperforms the functional one for all resistance values.

Figure 17. Fault coverage for "weak" bridges

Figure 18 shows fault coverage results for open defects where

- Total1 = FC(IDD, GAIN, NF) 50%
- Total2 = FC(IDD, GAIN, NF, DC-Voltage) 75%
- Total3 = FC(IDD, DC-Voltage) 62.5%
- Total4 = FC(NF, Gain) 50%

As with the case of bridges, we see here too that the fault coverage is improved when both structural and functional tests are used (Total2). For opens we do not see a difference between the power supply ramp and gain methods. We see though that the fault coverage of dc-voltage test method is higher. Figure 19 shows fault coverage results when weak opens are assumed. We notice here that for weak defects the power supply fault coverage outperforms the functional.

Figure 18. Functional vs. structural fault coverage of opens

Figure 19. Fault coverage for weak opens

8. Experimental Results

The power supply ramp method has been experimentally verified on the LNA. In this case, only eleven samples were tested. Their spatial location in the wafer is shown in Figure 20. LNA3 was not functional at all. Figure 21 shows the measured current signatures. A simple inspection revealed that LNAs 1 and 9 are potentially defective since their quiescent current exceeds the upper limit boundary for $V_{DD} > 1V$. Figure 22 shows measurement results of the output voltage. Labels LNA- and LNA+ indicate the negative and positive output voltages, respectively. The lines out of the tolerance band correspond to LNA5 and hence we can conclude that it is defective. S-parameter measurements were done using a network analyzer and then converted to voltage gain. Four measurements were performed for each frequency of interest. Figure 23 shows the corresponding voltage gain results. From Monte Carlo simulations we found before that the LNA's voltage gain boundaries are $-24.37dB$ and $-22.89dB$ at $2.45GHz$ for $V_{DD} = 1.8V$. Table 3 shows the measured voltage gain at nominal V_{DD} and the measured I_{DD} at $V_{DD} = 1.2V$. One can see that LNAs 1 and 9 exceed IDD_{ref} which is the simulated upper I_{DD} limit of $325\mu A$. Notice also that the voltage gain is slightly above the upper limit of $-22.89dB$. These LNAs are defective suspects. In this case we can say that we have a matching suspect between functional and structural tests. Worth mentioning is that the LNAs were processed in an experimental lot with outcome in the fast corner of the process.

Figure 20. Analyzed set of LNA devices

Figure 21. Current measurement results.

Figure 22. Output voltage measurements

Figure 23. Measured voltage gain of the LNA

Table 3. Experimental results for voltage gain and quiescent current.

LNA	Voltage Gain [dB] @2.45GHz, $V_{DD}=1.8V$	IDD [μA] @ $V_{DD}=1.2V$, IDD _{ref} =325 μA
1	-22.6	337.4
2	-22.97	314.8
4	-22.86	324
5	-25.77	299.3
6	-23.06	315
7	-22.73	326.4
8	-23.02	310.4
9	-22.63	338.8
10	-22.86	327.8
11	-22.84	321.3

9. Conclusions

Results of this study indicate a fault coverage for bridges of 88% using only the power supply ramp test method compared to 75% if only the LNA's voltage gain is measured, or to 83% if the LNA's Noise Figure is observed. If a combined functional gain and noise-figure test is carried out then the corresponding fault coverage is about 86%, while the combined structural test of the power supply ramp and the dc-voltage test gives a better coverage of 94%.

We have shown that the application of low frequency measurements, namely dc in this case, reduces test complexity without sacrificing fault coverage. These techniques can effectively be used at wafer test to do at least a pre-screening of bad devices. Although this

technique was tested on an LNA its applicability is general enough for types of other circuits. For the present circuit a discrete-step ramp was used, but we can foresee that for other types of circuits like PLLs, the type and slope of the ramp are important. The results shown in this paper are encouraging and more work is necessary to mature and implement this technique as a standard production testing method.

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