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12.7 A 0.75V 325 μ W 40dB-SFDR Frequency-Hopping Synthesizer for Wireless Sensor Networks in 90nm CMOS

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A limitation in the use of Frequency-Hopping Spread Spectrum (FHSS) for ultra-low-power Wireless Sensor Networks (WSNs) is the power dissipation of existing solutions. Whereas FHSS would make WSNs very robust and secure in difficult fading (indoor) environments, state-of-the-art solutions based on PLLs and digital frequency synthesizers require supply currents of several milliamperes [1,2]. A solution that consumes significantly less than 1mA is required to enable FHSS in autonomous WSN nodes. Power dissipation should also be independent of the hopping speed, as fast frequency hopping allows for fast synchronization, and results in minimum power overhead in the WSN. Furthermore, a fast hopping speed without power penalty allows designers to reduce the transmitted SNR by trading off hopping speed for transmitted power.

This paper presents a baseband Frequency-Hopping Synthesizer (FHS) architecture that achieves the above requirements, along with its circuit implementation. The system uses a combination of digital techniques, such as CMOS programmable dividers for scalability, low power and robustness, and analog techniques, such as harmonics suppression and filtering, for tight control of the harmonics throughout the frequency-generation chain. The hopping generator allows the generation of 56 accurate channels with a single frequency source, making FCC compliant FHSS possible in the ISM bands (915 and 2400MHz) at a power dissipation of only 325 μ W, which is more than an order of magnitude less than existing state-of-the-art fast-hopping synthesizers [2].

Figure 12.7.1 shows the realized FHS. The Single-Sideband (SSB) upconversion scheme allows doubling the number of channels that can be synthesized [1]. The synthesizer uses a single reference signal, two programmable digital dividers, a double quadrature mixer with SSB selection capability, two Walsh shapers (WS) and a final filtering stage.

A reference signal (f_{ref}) of 288MHz has been chosen and can be derived from an ultra-low-power SAW oscillator or a low-power PLL locked to a crystal-based reference oscillator. Following the equation in Fig. 12.7.1, 28 different frequencies spaced by 0.5MHz are derived. The divide-by-two block (A) in Fig. 12.7.1 generates the differential I/Q signals from the reference signal required to drive the mixer. The same reference signal is digitally divided down by divider M and shaped via the WS (B). The WS removes the 3rd and the 5th harmonics from the input and outputs a quadrature differential signal that drives the mixer. This signal contains, as first unwanted harmonics, only the 7th and the 9th, which are -17dBc and -19dBc, respectively. The output of the mixer contains the sum or the difference of the fundamental tones ($f_{ref}/2$ (from A) $\pm f_{ref}/4M$ according to the sideband selection) plus a number of tones. The highest unwanted tone is >17dB below the fundamental. The mixer output is fed into a limiter and then into a digital divide-by-N block which attenuates all the unwanted harmonics by 20log(2N) resulting in at least 15.5dB extra attenuation for a minimum N division ratio of 3. Finally, the divider output goes into the second WS (C). The largest harmonic of this WS output is at least 17dB below the fundamental and it originates from the 7th harmonics of the divide-by-N output signal. A first-order tunable passive LPF and a tunable notch filter (D) centered around the 7th harmonic of the fundamental remove the unwanted high frequency components and further reduce the unwanted tones more than 30dB with respect to the fundamental [3]. The absence of any feedback loop enables a hopping speed larger than 500khop/s.

The SSB mixer (E in Fig. 12.7.1) is a quadrature differential passive mixer (see Fig. 12.7.2). The wanted SSB is selected by swapping the phase of the LO signal. The output of the mixer is fed to a 2nd-order passive RC filter, which removes unwanted high-frequency components. A limiter reshapes the output signal in a digital fashion and the output signals from the two quadrature mixers are added using digital buffers followed by passive interpolation.

The WS block consists of a $\pm 45^\circ$ generator, a driving stage and a passive interpolator (Fig. 12.7.3). The $\pm 45^\circ$ generator is realized in a digital way by using three divide-by-two frequency dividers. Therefore, the output frequency is $1/4$ of the input frequency. A simple digital feedback provided by a NAND gate assures that, independently from the initial state of the FFs, the output signals (A to C) from the $\pm 45^\circ$ generator are in the correct phase relationship. This is achieved in a maximum of 4 clock cycles. When having a determined phase relation among them, it is possible to linearly interpolate those digital signals, using weighted resistors, in order to obtain the output waveform. Both differential and quadrature signals are accurately obtained in this way. The output waveform has strongly suppressed third and fifth harmonics while the seventh and the ninth harmonics are attenuated by 17dB and 19dB respectively.

The output of the WS (C) in Fig. 12.7.1 is fed to a tunable first-order LPF and then AC coupled to a notch filter (see Fig. 12.7.4). The LPF assures that high-order harmonics (above the tenth) are greatly attenuated. The notch is centered on the 7th harmonics and has the so-called Twin-T configuration. This assures that the notch is not too narrow (given its low Q) and results in good attenuation of both the 7th and the 9th harmonics with a single stage. To avoid any degradation of the notch position due to the LPF loading effect, a buffer is used to decouple the two stages. The buffer is optimized for a low 3rd-order distortion and consumes only 25 μ A. Tunability is achieved by changing the capacitances (MIM caps) of the LPF-notch filter in a thermometer fashion.

The synthesizer has been implemented in a 90nm CMOS technology as shown in Fig. 12.7.7. Figure 12.7.5 summarizes the measurement results of the synthesizer without final filtering (D). The worst case 3rd-harmonic attenuation is 38.5dB while the 5th is attenuated by more than 40dB. 7th and 9th harmonics are attenuated by more than 17 and 19dB respectively. The output signals are in quadrature with a phase error, measured averaging 1000 periods and over all channels, smaller than 0.3° in the worst case. The power consumption is lower than 250 μ W from a 0.75V supply. For three frequencies the power consumption is around 200 μ W because in those cases the output signal is derived directly from the reference signal without any mixing action.

Figure 12.7.6 summarizes the measurements of the tunable LPF-Notch filter and gives an overview of the system performances. Considering the harmonics in a bandwidth of around 80MHz (i.e. the 2.4GHz ISM band), the filter attenuates the 7th and 9th harmonics by more than 20dB while having a worst-case 3rd-order distortion lower than -45dBc with a 200mV_{pp} input signal. The tunability of the I/Q filter is around 5 octaves while dissipating 75 μ W from a 0.75V supply.

The measured SFDR of the total system, capable of generating 56 frequency hopping channels, is better than 40dBc. Power consumption is 325 μ W from a 0.75V supply, thus enabling new robust fast hopping sub-mW transceiver architectures for WSNs.

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Figure 12.7.1: Transmitter architecture and FH baseband synthesizer block diagram.

Figure 12.7.2: SSB mixer block diagram and circuit level implementation.

Figure 12.7.3: Walsh shaper schematic block diagram. The circuit implementation of the $\pm 45^\circ$ phase generator is depicted on the left and the passive interpolator schematic on the right.

Figure 12.7.4: Schematic block diagram of the LPF-Notch filter and its circuit level implementation. The tunable LPF is on the left, the decoupling buffer on the top and the Twin-T notch filter on the right.

Figure 12.7.5: Measured performances of the FH baseband synthesizer prior to the I/Q filter: 3rd, 5th, 7th and 9th harmonic level below the fundamental (upper left corner) versus the channel frequency; the measured output spectrum and the measured output waveform for the 0.5MHz synthesized channel (upper right and lower left corners respectively); the measured power consumption versus the synthesized channel (lower right corner).

Figure 12.7.6: Measured performances of the I/Q LPF-Notch tunable filter and summary of the overall system performances: I/Q filter attenuation characteristics for all the possible filter settings (upper left corner); I/Q filter attenuation with respect to the fundamental frequency component for all the synthesized channels (upper right corner); filter 3rd order harmonic distortion versus channel frequency at 200 mV_{pp} input signal (lower left corner); overall system (baseband + I/Q LPF-Notch tunable filter) performance.

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Figure 12.7.7: Micrograph of the FHS in 90nm CMOS. SPI is the digital interface which allows to program the baseband synthesizer and the I/Q LPF-Notch filter. The active chip area is $400 \times 700 \mu\text{m}^2$ for the I/Q LPF-Notch filter and $500 \times 300 \mu\text{m}^2$ for the FH synthesizer.