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A 44.5 GHz Differentially Tuned VCO in 65nm Bulk CMOS with 8% Tuning Range

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Abstract — This paper presents a low power, low phase noise mm-wave voltage controlled oscillator. The VCO can be tuned from 41 to 44.5 GHz (8% tuning range) and utilizes a differential tuning mechanism based on varactors and fixed MIM capacitors. Fabricated in a bulk CMOS 65nm technology, it consumes 3.6 mW and exhibits a phase noise of 106 dBc/Hz at 1 MHz offset from a 41.2 GHz carrier. The resulting FOM is –192.7 dBc/Hz, which is the best reported value for VCOs operating above 40 GHz.

Index Terms — CMOS integrated circuits, Millimeter wave oscillators, Phase locked loops, Phase noise, Voltage controlled oscillators.

I. INTRODUCTION

Voltage-controlled oscillators (VCOs) are essential building blocks of wireless transceivers. Low power consumption, high output power, low phase noise, wide tuning range and reliability are key requirements of VCOs. These requirements become even more challenging as new applications emerge at mm-wave frequencies. Broadband WPAN at 60 GHz ISM band, automotive radar sensors at 76 GHz and imaging applications at 94 GHz are some examples of mm-wave applications.

The design of mm-wave VCOs poses numerous challenges. At these frequencies, varactors, which are invariably used for tuning LC-VCOs, become the limiting factor for the overall tank quality factor. Furthermore, the value of the required passives is of the same order as parasitic capacitances and inductances. Therefore, accurate models of passives are vital for achieving correct oscillation frequency. In addition, layout dependent parasitics, which could deviate the VCO from its intended frequency range, also become a critical problem.

Many integrated CMOS VCOs operating above 40 GHz have been reported in recent years [1]-[5]. In order to boost the oscillation frequency and improve quality factor of passives, high-resistivity substrates and SOI CMOS is being used [1]-[2]. However, these technologies require extra processing steps, thereby increasing the cost. Similarly, special layout techniques for transistors and passive devices, to minimize parasitics, have been demonstrated [4]. In this paper, a 44.5 GHz complementary cross-coupled LC VCO is presented. MIM capacitors are used to improve the quality factor of the capacitive part of the tank. Differential tuning is adopted to improve phase noise performance. Chip layout has been carried out carefully to avoid unnecessary parasitics. The VCO has been implemented in a 65nm bulk CMOS LP (low power) technology. In combination with a divider, the proposed VCO can be used, firstly, for a 60-GHz double-conversion zero-IF (sliding-IF) receiver and secondly, for a 60-GHz transmitter using a harmonic frequency tripler.

II. VCO ARCHITECTURE

The schematic of the VCO is shown in Fig. 1 (a). A complementary cross-coupled architecture is chosen for this design. As compared to NMOS-only VCO, the complementary structure provides higher transconductance at a given current, which results in faster switching and larger output amplitude. In addition, it demonstrates superior rise- and fall-time symmetry resulting in less upconversion of 1/f noise [6].
The transistors M1 to M4 form the active part of the VCO. A ratio of two is chosen between negative transconductance and losses of the tank, to ensure reliable startup. In order to match the transconductance of PMOS and NMOS transistors, the former has twice the width. The resonator is composed of a single turn octagonal shaped inductor and a combination of varactors and fixed MIM capacitors. The VCO is tuned differentially. This minimizes common-mode noise from voltage supplies and other sources and improves the phase noise performance. An output buffer is included for measurement purposes. The differential outputs use 50 Ω transmission lines to the bond-pads.

III. Resonator and Output Buffer Design

At mm-wave frequencies the required inductors are small and exhibit a reasonably high quality factor (Q). In contrast, quality factor of the capacitive part, i.e. the varactors becomes the dominant factor. The quality factor of a LC tank ($Q_{tank}$) is given by,

$$\frac{1}{Q_{tank}} = \frac{1}{Q_L} + \frac{1}{Q_C}$$

where $Q_L$ and $Q_C$ are quality factors of the inductor and capacitors that make up the tank. In case, $Q_L$ is much lower than $Q_C$, which is generally the case for frequencies up to a few gigahertz, improving $Q_L$ leads to a higher $Q_{tank}$. However, at mm-wave frequencies and with introduction of modern CMOS processes, the quality factor of the capacitor ($Q_C$) is significantly lower than $Q_L$ [3]. Thus, more design effort should be invested in improving $Q_C$ at mm-wave frequencies rather than improving $Q_L$.

A. Inductor design

The on-chip integrated inductor is a single turn octagonal shaped coil. It utilizes the thick top metal, to reduce series resistance, thereby increasing the quality factor. The inductor metal width and inner radius are 6µm and 15µm, respectively. The simulated inductance value is 95 pH, with a quality factor of 20 at 40 GHz. The area occupied by the inductor is 60x60 µm.

B. Varactor design

The tuning of VCO is achieved by combination of accumulation MOS (AMOS) varactors and fixed MIM capacitors (see Fig. 1 (b)). Metal-insulated-metal (MIM) capacitors exhibit high Q-factors (above 20) at mm-wave frequencies due to low intrinsic losses. Thus, using them in series with varactors improves the quality factor, at the expense of reduced tuning range. The simulated tank capacitance and quality factor are shown in Fig. 2. The $C_{var}/C_{tot}$ ratio of this setup is 2.1 and $Q_c$ varies between 8.5 and 14.3. The reduced capacitance ratio due to MIM capacitors is not an issue, as the desired frequency tuning range is still successfully achieved. The advantage on the other hand is that $Q_c$ improves by approx. 40% as compared to a stand-alone varactor implementation.

In addition, some flexibility is achieved by connecting the lower terminal of the biasing resistors (Vb in Fig. 1(b)) to an external supply instead of grounding them. This provides an extra control voltage to cater parasitics and process variation. Fig 2. shows the capacitance and $Q_C$ variation as a function of differential tuning voltage ($V_{bias+} - V_{bias-}$) for three biasing voltages.

Differential tuning is adopted for the capacitive part of the LC-tank [2]. Common-mode noise can modulate the varactors, if the VCO is tuned from a single node. This noise appears as jitter and phase noise at the VCO output. Differential tuning alleviates this problem by reducing the common-mode noise, thus improving phase noise.

C. Output buffer

A common-source differential stage is designed as an output buffer, to make on-wafer measurements possible. In order to avoid loading of the VCO, the buffer is biased independently. This also helps in measuring the power consumption of VCO and buffer separately. The load resistance (silicided poly-silicon based) is 50 Ω, to match it with the transmission lines as well as the measurement equipment.
IV. LAYOUT AND TECHNOLOGY

As mentioned earlier, layout is done carefully and compactly to reduce parasitics. The RF signal paths between the inductor, capacitive tuning part and transistors are kept as short as possible. Narrow connecting lines are avoided to minimize resistive losses. Ground meshing is used underneath the RF paths. Decoupling capacitors are included for the voltage supplies. The differential outputs use 50 transmission lines (TL’s) to the bond-pads. These TL’s are coplanar waveguide based with lateral ground-plane consisting of all metal layers. The width of the TL is 5µm and spacing from the ground plane is 4.22µm.

The VCO is fabricated in TSMC bulk CMOS 65nm LP (low-power) process having six metallization layers. The process offers MIM capacitors and poly-silicon resistors. The measured fT of NMOS and PMOS transistors is 140 GHz and 80 GHz, respectively. Due to bond-pad limitation the total chip area is 700 x 400 µm. However, the VCO core only occupies 100 x 100 µm. The chip micrograph is shown in Fig. 3.

![Chip micrograph](image)

Fig. 3. Chip micrograph

The frequency tuning range (FTR) of the VCO is shown in Fig. 4, where output oscillation frequency is plotted versus differential tuning voltage for three bias voltages (Vb). It can be seen that tuning curves follow the tank capacitance curves of Fig. 2. The minimum and maximum measured frequencies are 41 GHz and 44.5 GHz (see Fig. 5), respectively, giving a tuning range of 8.1 %.

![VCO frequency tuning range](image)

Fig. 4. VCO frequency tuning range

The VCO and output buffer consume 3mA and 5mA from a 1.2V supply, respectively. The total loss from the wiring cables, connectors and hybrid was measured between 6 and 8 dB over the entire frequency tuning range. After de-embedding this loss, the average differential output power delivered to a 50 Ω load is between -2 and -6 dBm as shown in Fig. 6.

![VCO output spectrum at 44.4 GHz](image)

Fig. 5. VCO output spectrum at 44.4 GHz

V. MEASUREMENT RESULTS

The VCO was measured on-wafer using a high frequency differential probe (GSGSG) and a 180° hybrid coupler. An Agilent PSA series spectrum analyzer with phase noise functionality was used for spectral measurements. The measurement equipment generates considerable external noise, which can potentially degrade the measured results. In order to suppress the noise coming from power supplies, dedicated filters are employed. In addition, common-grounds between the supplies and spectrum analyzer are eliminated. The lighting of the viewing optics is turned-off during measurement [2]. It is noticed that central alignment of the infinity probes (on the bond-pads) and good probe contact yield stable and repeatable measurements.
The measured phase noise of the VCO at 41.2 GHz is shown in Fig. 7. At 100 kHz and 1 MHz offsets, the measured values are -98 and -106 dBc/Hz, respectively. The commonly used FOM for VCOs is defined as $\text{FOM} = \text{L}\{f\} - 20 \log(f_0/f) + 10\log(P_{dc}/1 \text{ mW})$, where $\text{L}\{f\}$ is the measured phase noise at frequency offset $f$ from the carrier at $f_0$, and $P_{dc}$ is the DC power consumption [1]. Using the above expression and measured phase noise at 1-MHz offset, a FOM of -192.7 dBc/Hz is achieved, which is the best reported FOM for VCOs operating above 40 GHz. Table I compares published state-of-the-art VCO's operating at mm-wave frequencies. The presented VCO has the lowest power-consumption (excluding output buffers) while achieving a reasonable frequency tuning range. The phase noise is better than reported SOI implementations in [1], [2].

<table>
<thead>
<tr>
<th>Ref. &amp; Tech.</th>
<th>Freq. (GHz)</th>
<th>$P_{dc}$ (mW)</th>
<th>FTR (%)</th>
<th>PN@1MHz (dBc/Hz)</th>
<th>FOM (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1] 0.13µm SOI CMOS</td>
<td>40.7</td>
<td>11.3</td>
<td>15</td>
<td>-89</td>
<td>-170.6</td>
</tr>
<tr>
<td>[2] 0.12µm CMOS SOI</td>
<td>44</td>
<td>7.5</td>
<td>9.8</td>
<td>-101</td>
<td>-185</td>
</tr>
<tr>
<td>[3] 0.13µm CMOS</td>
<td>43</td>
<td>7</td>
<td>4.2</td>
<td>-90</td>
<td>-174.2</td>
</tr>
<tr>
<td>[4] 0.13µm CMOS</td>
<td>59</td>
<td>9.8</td>
<td>10.2</td>
<td>-89</td>
<td>-174.5</td>
</tr>
<tr>
<td>[5] 0.18µm CMOS</td>
<td>50</td>
<td>4</td>
<td>2</td>
<td>-96</td>
<td>-184</td>
</tr>
<tr>
<td>This work 65nm CMOS</td>
<td>44.5</td>
<td>3.6</td>
<td>8.1</td>
<td>-106</td>
<td>-192.7</td>
</tr>
</tbody>
</table>

V. CONCLUSION

We have presented a 44.5 GHz complementary LC cross-coupled VCO implemented in a 65nm bulk CMOS LP technology. The use of MIM capacitors to improve Qc, differential tuning to reduce phase noise and compact layout to minimize parasitics yields good measured results. The VCO has a FTR of 8% and dissipates 3.6mW. The measured phase noise at 1MHz offset from a 41.2 GHz carrier is -106 dBc/Hz resulting in an excellent FOM of -192.7 dBc/Hz.

REFERENCES