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Topology Comparison and Design Optimisation of the Buck Converter and the Single-Inductor Dual-Output Converter for System-in-Package in 65nm CMOS

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Abstract- Portable electronic devices, such as laptop computers and personal portable electronic devices are battery-powered and need power-electronics converters as an interface between the battery and the load. To ensure a long battery life, it is important that the power-electronic converters operate at high efficiency. The volume available for power electronics is limited which necessitates the use of integration technologies to achieve high-power-density converters. Integrating passive components in silicon makes monolithic integration of power converters in system-on-chip difficult and hybrid integration in the form of system-in-package where passive components are implemented in alternative technologies and integrated in the package seems to be a more feasible option at present.

High operating frequencies, necessary for the reduction of the passive components size results in the increase of switching losses in the power semiconductors which negatively influences the efficiency. Furthermore, power semiconductor losses are directly dependent on the chip size which in turn influences the cost of the converter. Also, the losses are dependent on the time waveforms of electrical currents and voltages which in turn depend on the chosen circuit topology. The paper presents a topology comparison and a design optimization procedure for the implementation of a DC-DC converter (V_{in} 3V– 4.2V from Li-ion battery, V_{out} 0.6V– 1.2V, load current < several 100mA). It is assumed that the active part of the converter is implemented in 65nm CMOS technology. A high-level topology evaluation based on several criteria such as efficiency, cost, technology feasibility and size is presented. The design procedure for maximum integrated DC-DC converter efficiency by means of finding optimum transistor widths is presented and illustrated on two topologies.

I. INTRODUCTION

Current trends in portable consumer electronics demand progressively lower voltage supplies. Portable electronic devices, such as laptop computers and personal portable electronic devices are battery-powered and need power-electronic converters as an interface between the battery and the load. The number of features implemented in mobile devices increases dramatically leading to a large number of

different supply voltages, all of which need to be generated from a single battery voltage. To ensure a long battery life, it is important that the power-electronic converters operate at high efficiency. Furthermore, the volume in the devices available for power electronics is normally very limited which necessitates the use of integration technologies to achieve small volumes and high power densities of power electronics. Integrating passive components in silicon makes monolithic integration of power converters in system-on-chip difficult [1] and hybrid integration in the form of system-in-package (SiP) where passive components are implemented in alternative technologies [2], [3] and integrated in the package seems to be a more feasible option at this point in time.

In order to make the integration of passive components in the package possible they have to be reduced in size, which is achieved by operating the converter at high switching frequencies and thus reducing the volume of passive components required for energy storage. However, the switching frequency increase results in the increase of switching losses in the power semiconductors, which negatively influences the efficiency. Furthermore, the power semiconductor losses are directly dependent on the chip size which in turn influences the cost of the converter. Also, the losses in all components are dependent on the time waveforms of electrical currents and voltages, which in turn depend on the chosen circuit topology. All these factors need to be taken into account in order to come to an optimum design that fulfills the high-efficiency, small-size and low-cost requirements.

In this paper, a design procedure for achieving highest efficiency for a chosen topology will be presented. Firstly, a literature study on feasible converter topologies was carried out and the topologies were evaluated on the basis of several criteria. The topology choice will be limited to inductive topologies due to their ability to enable good control of the output voltage over input voltage and output-load variations by means of controlling the duty cycle of the power switches using fewer passive components than capacitive converters. Two most promising topologies, namely the conventional buck converter and the single-inductor dual-output converter, will be considered and the two-step design procedure for achieving the

highest efficiency will be demonstrated on these two topologies. It is assumed that the active part of the converter is implemented in 65nm CMOS technology with the intention to integrate the load and converter in the later stage.

II. TECHNOLOGY PLATFORM

The available technology largely influences the topology choice in particular concerning the integration of passives. In this work, the proprietary silicon-based process Passive-Integration Connective Substrate (PICS™) that provides a platform for the integration of resistors, capacitors and inductors [4][5] is used. It offers several advantages for realizing integrated DC-DC converters. First, it achieves large capacitance densities by utilizing trench-MOS capacitors. The typical values used in demonstrated prototypes is 80 nF/mm² [2][6] and the recent results go as high as 400 nF/mm² [7]. Secondly, an 8-μm thick copper top-metal layer available in this technology in addition to the first aluminium metal layer enables the design of spiral air-core inductors with reasonable performance. Figure 1a shows a two-die SiP approach. The drivers and power transistors are implemented in a CMOS die. The passive components, on the other hand, are realised on a

Figure 1a. Two die SiP approach: passive PICS die and CMOS active die
b. SiP DC-DC converter demonstrator (input 1.8V, output 1.1V@100mA, 80MHz)

PICS die, which is connected to the CMOS die by means of flip-chip solder bumps. Figure 1b shows a technology demonstrator showing the feasibility of this concept on an integrated DC-DC down converter [2]. The figure shows the active die flip chipped onto the passive die containing the planar 20nH air-core inductor and input and output capacitors. The realized SiP converter fits inside a standard QFP64 package.

The boundary conditions of this technology and the SiP approach will be used as inputs to the design optimization procedure. The design with both an air core inductor and a magnetic core inductor will be investigated and compared.

III. FIRST LEVEL TOPOLOGY SELECTION

The specifications of the chosen case study DC-DC converter are: input voltage 3V– 4.2V from a Li-ion battery, output voltage 0.6V– 1.2V, load current up to several hundreds of mA. The primary selection of topologies was based on the results of the previous developments made in the field of integration of low-power converters including the authors’ knowledge and literature. These topologies were then qualitatively evaluated on the basis of several criteria: efficiency, size, cost, transient response and technological feasibility. The details of the topologies are available in the literature and will not be given here [8]-[14]. A weighing factor was assigned to each criteria depending on how important the criteria is for this application. The total score is not intended to give an absolute result of which topology is the most optimal, but rather to help eliminate the worst scoring topologies. Table 1 shows the results of the evaluation with some explanation to justify the scores.

Based on the results of the evaluation two topologies were evaluated further, the buck (in CCM and DCM) and the Single Inductor Dual-Output (SIDO) converter.

IV. CIRCUIT TOPOLOGIES AND LOSS MODEL

The synchronous buck converter is widely used in industry due to its simplicity and low number of components. Both Continuous-Conduction Mode (CCM) and Discontinuous-Conduction Mode (DCM) of operation will be modelled and compared.

TABLE 1
FIRST LEVEL TOPOLOGY EVALUATION

Criteria	FoI	Synchronous Buck	Interleaved Buck	Class- E	Inductor Multiplier	Single Inductor Dual-Output
Efficiency	3	2/3 (integr. inductor)	3/3	2/3 (circulating currents in res. tank)	1/3 (losses almost 2X that of off-chip inductor)	2/3 (additional switches)
Size	3	3/3	2/3 (multiple stages)	1/3 (multiple conversion stages)	3/3	3/3
Cost	3	3/3	2/3 (add. control circuitry)	1/3 (large silicon area)	3/3	3/3
Transient Response	2	3/3	3/3	2/3 (size of RF input inductor)	1/3 (ripple cancellation)	2/3 (regulation of different outputs)
Feasibility	3	3/3	3/3	3/3	3/3	3/3
Total		39/42	36/42	25/42	32/42	37/42

Figure 2 Circuit schematics a. synchronous buck converter b. Single-Inductor Dual-Output (SIDO) converter

The SIDO converter was chosen due to its capability to supply two outputs with different voltage levels which is required in many applications. The performance of the SIDO converter will be compared to the performance of two buck converters. Figure 2 shows the circuit schematics of both topologies.

Analytical models of the circuit operation of both topologies were made (in Matchad) and the losses in the components were calculated using the relevant voltage and current waveforms and component physical characteristics. The calculation of the converter losses includes the inductor loss, the input and output capacitor losses and the losses in the switches. The losses in the gate drivers have not been included.

A. Inductor loss

The losses in the inductor are obtained by using the following equation:

$$P_{L,loss} = I_{L,RMS}^2 ESR_L \quad (1)$$

where ESR_L is the equivalent series resistance of the inductor (representing the conductor losses and additional core losses in the case of an inductor with a magnetic core). Two particular inductor designs were used in the following optimisation procedure; a spiral air-core inductor with the inductance value of $L_{air} = 18.9\text{nH}$ and a thin-film electroplated magnetic core inductor with the inductance value of $L_{core} = 190.9\text{nH}$. The prototypes of these inductors were already available and the ESR and L for both inductors was obtained by means of curve fitting

of the experimental results.

B. Power MOSFET losses

The MOSFET losses in both PMOS and NMOS consist of conduction losses and switching losses. The conduction losses in the PMOS and NMOS can be obtained by the following equations [15][16]:

$$P_{con,PMOS} = D \times I_{L,RMS}^2 \times R_{ds,ON,PMOS} \quad (2)$$

$$P_{con,NMOS} = (1-D) \times I_{L,RMS}^2 \times R_{ds,ON,NMOS} \quad (3)$$

where $R_{ds,ON}$ is the on-resistance of the transistor dependent on the transistor width and can be calculated as:

$$R_{on} = \frac{R_{ds,ON}^0}{Width_{Opt}} \quad (4)$$

where $R_{ds,ON}^0$ is the normalized ON-resistance of the switch [$\Omega\mu\text{m}$]. The switching losses of integrated power transistors are the losses due to charging and discharging of the equivalent parasitic capacitances [17]-[19]:

$$P_{sw,PMOS} = C_{eq,PMOS} \times V_{dd}^2 \times f_s \quad (5)$$

$$P_{sw,NMOS} = C_{eq,NMOS} \times V_{dd}^2 \times f_s \quad (6)$$

These equations give a simplistic representation of the MOSFET losses as they do not consider any dependency of the switching losses on the inductor current during the switching transitions as well as the switching interval duration. As a consequence, the loss reduction due to potential soft switching conditions is not included. The capacitance values C_{gs} , C_{ds} and C_{gd} of the MOSFET are proportional to the size of the transistor, and they are non-linear (depends on the working region of the transistor). For the simplicity sake, the non-linearity effect is neglected, and the capacitance values are considered to be constant for a given width and equal to the values valid when the transistor is operating in linear region. The equivalent capacitance of the MOSFET under hard-switching conditions is given as follows:

$$C_{eq} = C_{gs} + 2 \times C_{gd} + C_{ds} \quad (7)$$

and can be calculated as the function of the transistor width as:

$$C_{eq} = C_{eq}^0 \times Width_{Opt} \quad (8)$$

where C_{eq}^0 is the normalized switch equivalent capacitance [$\text{F}/\mu\text{m}$].

V. DESIGN PROCEDURE AND OPTIMISATION STRATEGY

The tradeoffs involved in increasing the switching frequency were discussed in Section I. In this section, a design procedure for finding optimal width of the transistors to achieve the best efficiency will be presented. The design procedure will be performed in two steps, coarse and fine optimisation. Figure 3 shows the flow diagram of the complete procedure.

A. Coarse optimisation stage

In the first step, an analytical model of the topology is derived and implemented in Matchad. The model gives the time waveforms of currents and voltages assuming the ideal

components characteristics, which means that they do not include the voltage drops caused by the on-resistance of the switches and the ESR of the inductor. The width of the transistor that offers the minimum power dissipation can be found by differentiating the total loss of the power switch as follows:

Figure 3 Design procedure flow chart

$$\frac{d(P_{Tot,PMOS})}{d(Width)} = (C_{eq}^0 \times V_{dd}^2 \times f_s) - (D \times I_{L,RMS}^2 \times (R_{ds,ON}^0 \times \frac{1}{Width_{PMOS}^2})) = 0 \quad (9)$$

The optimum PMOS and NMOS width for minimum total losses can be expressed as:

$$Width_{PMOS}(f_s) = \sqrt{\frac{I_{L,rms}^2(f_s) \times D \times R_{ds,ON,PMOS}^0}{C_{eq,PMOS}^0 \times V_{dd}^2 \times f_s}} \quad (10)$$

$$Width_{NMOS}(f_s) = \sqrt{\frac{I_{L,rms}^2(f_s) \times (1-D) \times R_{ds,ON,NMOS}^0}{C_{eq,NMOS}^0 \times V_{dd}^2 \times f_s}} \quad (11)$$

Once the optimum transistor width is calculated, $R_{ds,ON}(f_s)$ and $C_{eq}(f_s)$ are obtained from the equations (4) and (8), which are then used to calculate the losses in the converter as presented in Section II. From the graph showing efficiency vs. switching frequency, the frequency giving maximum efficiency, $f_{s,opt}$, is identified. This frequency corresponds to the optimum transistor width $Width_{opt}$, which is then used as an input for the fine optimisation stage.

A. Fine optimisation stage

To validate the design solution, system-level simulations have been performed in Cadence using real transistor models. The cross-check of the results obtained in the analytical model (in Mathcad) with the results obtained from simulations (Cadence) is performed in this stage. When the two results match it can be concluded that the computational model is accurate enough to model the behaviour of the converter and, therefore, the model can be validated. In the fine optimisation stage, the converter parasitic resistances obtained from the coarse stage are then included in the converter model. Consequently, a new set of formulas has to be derived which consider the voltage drop caused by the circuit parasitic series resistances. However, adding the circuit parasitic in the model may shift the optimum switching frequency value (since the parasitics are frequency-dependent). Therefore, by sweeping the frequency in the fine model, a new optimum frequency value $f_{s,opt,fine}$ is obtained. Note that the transistor widths remain fixed during the fine optimisation stage, whereas in reality these widths are frequency-dependent. It will be shown later that changing the width slightly around the optimum value will not have a significant impact on the converter efficiency, which means that the assumption above is valid.

VI. MODELLING AND SIMULATION RESULTS

Following the optimisation procedure described in Section III, the performance optimisation of the buck converter operating in CCM and DCM and the SIDO converter has been carried out. The procedure has been performed for both the air-core inductor and the magnetic-core inductor described in section IV A.

A. Buck converter in CCM

Figure 4a shows the converter efficiency as a function of the switching frequency. It can be seen that maximum efficiency ($\eta = 61.1\%$) is achieved at $f_{s,opt} = 145$ MHz. Figure 4b shows the total loss as a function of the transistors' widths. It can be seen that there is a relatively large area where the total losses remain low for different values of the transistors' width. This means that a slight change of the transistors' widths around the optimum size will not have a significant impact on the efficiency. This is important since the width of the transistor will be fixed for the fine optimisation stage, as explained in Section V. Now that the transistor widths have been fixed the voltage drops caused by the on-resistances of the switches and the inductor ESR will be included in the model. When the PMOS is on, the inductor voltage is given by the following equation:

$$V_L = V_{in} - V_{out} - I_{out} \times (R_{on,PMOS} + ESR_L) \quad (12)$$

When the NMOS is on, the inductor voltage is:

$$V_L = -V_{out} - I_{out} \times (R_{on,NMOS} + ESR_L) \quad (13)$$

Applying the volt-second-balance principle, the modified duty cycle value is given by:

$$D_{ccm}(f_s) = \frac{V_{out} + I_{out} \times (R_{on,NMOS}(f_s) + ESR_L(f_s))}{V_{in} - I_{out} \times (R_{on,PMOS}(f_s) - R_{on,NMOS}(f_s))} \quad (14)$$

Figure 4 Buck converter in CCM with air-core inductor – coarse optimisation
a. Efficiency vs. frequency b. Losses in the switches vs. transistors' width

Applying the modified expressions of the duty cycle and current ripple, the total losses of the converter are calculated. Figure 5a shows the individual components loss contributions and the total loss versus frequency. The inductor losses at low frequencies are dominated due to a high current ripple. As the operating frequency increases, the inductor parasitic resistance ESR_L becomes dominant resulting in an increase of the inductor loss. Similarly, the loss mechanism related to the power switches is characterized by the fact that at low frequencies, conduction losses are dominant due to the high inductor current ripple. As the operating frequency increases the switching losses become dominant, since these are directly proportional to the switching frequency. Figure 5b shows the analytically calculated efficiency and simulated efficiency. A new optimum operating frequency is found to be $f_{s,opt,fine} = 140$ MHz resulting in the converter efficiency of 59.3%.

The procedure has been repeated on the converter with the magnetic core inductor resulting in the maximum efficiency of 72.3% at 10MHz. The lower operating frequency is due to the higher inductance value (190nH compared to 18.9nH of the air core inductor). Figure 6 shows clearly that the converter that uses an inductor with magnetic core has better efficiency than the converter with air-core inductor. It can be concluded that the converter performance depends strongly on the quality of the magnetic component. The magnetic-core inductor used has a

higher inductance value and lower series resistance. As a result, the inductor current ripple remains lower than in the case of inductor with air-core.

(a)

(b)

Figure 5 Buck converter in CCM with air-core inductor – fine optimisation
a. Loss vs. frequency b. Calculated and simulated efficiency

Figure 6 Buck converter in CCM – air core vs. magnetic core efficiency comparison

B. Buck converter in DCM

A similar procedure has been performed for the converter operating in DCM. The optimum operating frequency that is obtained in the coarse stage is $f_{s,opt} = 95$ MHz. In the fine

optimisation stage the voltage drops caused by the parasitic series resistances of the inductor and switches are included. The expressions for the modified duty cycle $D_{dm}(f)$ and the interval in which the inductor current decreases to zero $\Delta_{dm}(f)$ become as follows:

$$D_{dm}(f_s) = \sqrt{\frac{I_{out} \cdot f_s \cdot 2L}{V_{out}}} \times \left[1 + \frac{V_{in} - V_{out} - I_{out} \times (R_{on,P}(f_s) + ESR_L(f_s))}{-V_{out} - I_{out} \times (R_{on,N}(f_s) + ESR_L(f_s))} \right] \quad (15)$$

$$\Delta_{dm}(f_s) = D_{dm}(f_s) \times \frac{V_{in} - V_{out} - I_{out} \times (R_{on,P}(f_s) + ESR_L(f_s))}{V_{out} + I_{out} \times (R_{on,N}(f_s) + ESR_L(f_s))} \quad (16)$$

Figure 7 shows the efficiency graphs derived from the analytical model and simulations. A new optimum operating frequency is found to be $f_{s,opt,fine} = 120$ MHz resulting in the converter efficiency of 66%.

Figure 7 Buck converter in DCM with air-core inductor– fine optimisation a. Loss vs. frequency b. Calculated and simulated efficiency

C. Single-Inductor Dual-Output Converter

For the sake of simplicity, it is assumed that the two outputs of the SIDO converter require equal power level (1V@100mA). In practice, however, the loads may require different power levels. Figure 8 shows the voltage and current waveform of the SIDO converter.

Figure 8 SIDO converter time waveforms

Figure 9 shows the total power loss and efficiency of the SIDO converter as a function of switching frequency when

using an air-core inductor. A behavior similar to the regular buck converter is noticed here. At low frequencies and high inductor current ripple, the inductor RMS current loss and conduction losses in the switches are dominating. At high frequencies the switching losses in the switches and eddy current losses in the inductor are the main loss contributors. The optimum operating frequency is found where the losses have the lowest value. The optimum frequency for the maximum efficiency in DCM mode is $f_{s,opt,fine} = 160$ MHz and the border frequency between CCM and DCM is $f_{CCM,DCM} = 227$ MHz.

Figure 9 SIDO converter with air-core inductor (a) components loss contribution and (b) efficiency vs switching frequency

D. Comparison

Table 2 shows the main design parameters of the two topologies, the synchronous buck and the Single-Input Dual-Output (SIDO) converter.

For the buck converter, the design parameters for the converter operating in CCM and DCM with the air-core inductor and CCM with the magnetic-core inductor are presented. It can be seen that the option with the magnetic core achieves the highest efficiency. The main reason for this is lower switching losses due to a lower operating frequency (10 MHz vs. 140 MHz). The inductor losses are also somewhat lower in the case of the magnetic-core inductor due to the lower ESR_L for the similar current ripple value (the product of the inductance value and operating frequency for both cases is similar: 18.9 nH and 140 MHz for the air-core inductor and 190 nH and 10 MHz for the magnetic-core inductor). The footprint area of the magnetic core used in this case is 5.7mm² compared to 3.3mm² of the air-core inductor. The design values of the transistor widths of the converter with the magnetic core are several times larger than in the case of the air-core inductor converter (3.08mm PMOS and 2.2mm NMOS).

Looking at the design parameters and results for the dual-output topologies, namely the SIDO converter and two buck two outputs (TBTO) converters it can be seen that the efficiency of the TBTO design is higher than that of the SIDO converter. This is primarily a consequence of the higher switching losses due to the higher operating frequency of the SIDO converter (160 MHz vs 120 MHz). However, the SIDO

converter has only one inductor compared to the TBTO solution with two inductors which substantially increases the footprint of the complete converter.

It can be seen that in both cases there is a clear trade-off

between efficiency and size so when choosing the optimum topology and design parameters the boundary conditions of the particular application have to be taken into account.

TABLE 2
DESIGN PARAMETERS AND COMPARISON

	Single-Input Single-Output Converter			Single-Input Dual-Output Converter	
I _{out} = 100mA V _{out} = 1V V _{in} = 3.6V	Buck CCM Air-Core Inductor	Buck DCM Air-Core Inductor	Buck Magnetic Core Inductor in CCM	SIDO (DCM, Air-core inductor)	TBTO (DCM, Air-core inductor)
L [nH]	18.92	18.88	190	18.96	18.88(x2)
ESR _L [Ω]	1.40	1.25	1.05	1.03	1.25(x2)
R _{ON PMOS} [Ω]	2.01	1.82	0.48	0.86	1.82
f _{s,opt} [MHz]	140	120	10	160	120
R _{ON NMOS} [Ω]	0.97	0.88	0.23	0.42	0.88
η [%]	59.35	66.05	72.29	56.75	66.05

VII. CONCLUSIONS

In this paper a systematic design procedure for highly SiP integrated DC-DC converters for portable applications is presented. The procedure is implemented in two steps, a coarse and fine stage, for a time-efficient design. The optimisation criterion is conversion efficiency since this is crucial for a long battery life. The design procedure is demonstrated on the chosen case study, for a single and two-output converter. In both cases, a clear trade-off between efficiency and size is observed. The converter footprint is another crucial aspect in portable electronics due to the ever-increasing trend for miniaturization. If one takes into account the importance of cost in these applications, it is clear that the presented approach should be extended to a multi-criteria design-optimization procedure in order to get to the most optimum solution for the particular application.

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