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A 40-GHz Phase-Locked Loop Front-End for 60-GHz Transceivers in 65nm CMOS

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Abstract — A phase-locked loop front-end including a LC voltage controlled oscillator and an I-Q injection locked frequency divider is presented. The operation ranges of the VCO and ILFD are aligned by co-designing the tank, specifically the tunable varactors. The total locking range of the front-end is 37.6 to 42.2 GHz which corresponds to a down-conversion range from 56.4 to 63.3 GHz at 60 GHz, thus covering the complete ISM band. The front-end phase noise for a VCO frequency of 39.8 GHz is -102 dBc/Hz at 1 MHz offset. The DC power consumption of the VCO and Q-ILFD is 6mW and 9mW from a 1.2 V supply, respectively. Implemented in a bulk CMOS 65nm technology, the circuit occupies an area of 0.7x0.5 mm².

Keywords — injection locked frequency divider, voltage controlled oscillator, phase locked loop.

I. INTRODUCTION

The ever increasing demand for higher data rates for wireless personal area networks (WPAN) has motivated research and development of 60 GHz transceivers in recent years. The 7 GHz of contiguous bandwidth available at 60 GHz, though very useful, poses circuit design challenges especially for components like VCOs, prescalers and PLLs in a direct conversion transceiver [4-7]. Therefore, alternative synthesizer friendly architectures based on double-heterodyne, sliding-IF, low-IF and half-RF architectures are being investigated [1-3].

The PLL front-end, including the voltage controlled oscillator (VCO) and the first divider stage which in many cases is an injection locked frequency divider (ILFD), is the most challenging part as it operates at the highest frequencies in a PLL. Fig. 1 shows a 60 GHz receiver architecture which is based on a two step down-conversion using outputs from the VCO and the ILFD of a 40 GHz PLL. In order to support the complete 7 GHz bandwidth from 57 to 64 GHz, the PLL front-end needs an operation range from 38 to 42.6 GHz. In this paper, we present a 40 GHz PLL front-end (highlighted portion in Fig. 2) satisfying the above frequency range with low power consumption and good phase noise performance.

Fig. 1. The highlighted PLL front-end as part of the a 40 GHz PLL

The paper is organized as follows. Section II explains the circuit design of the VCO and ILFD followed by details of layout and technology in section III. The measurement results are present in section IV and conclusions are drawn in section V.

II. CIRCUIT DESIGN

The complete schematic of the PLL front-end is shown in Fig. 2. The 40 GHz VCO shown on the left hand side is an only-NMOS cross coupled architecture. The aim in the VCO design is to maximize tuning range so that in case of any frequency shift the measured tuning range still covers the desired frequency band. The enhancement of tuning range can be achieved by decreasing the fixed capacitance from the total tank capacitance. This provides more “room” for the variable capacitance from the varactors whose $C_{\max}/C_{\min}$ can be raised to achieve a wider tuning range. In order to reduce the fixed capacitance, a number of modifications are made. Firstly, an only-NMOS topology is chosen which removes the capacitance

Fig. 2. Circuit schematic of the PLL front-end including VCO, I-Q injection locked frequency divider and output buffers

contribution from the PMOS devices present in a complementary structure. Secondly, a simple tuning circuit is employed by connecting two varactors back to back and avoiding use of MIM capacitors which are sometimes included to improve quality factor.

The VCO inductor is a single-turn top-metal inductor of 95pH with a Q-factor of ~ 20 at 40 GHz. Each varactor is composed of 30 multi-fingers, having a length and width of 300 nm and 2 μm per finger, respectively. The maximum and minimum capacitances are 106 fF and 30 fF resulting in a $C_{\text{max}}/C_{\text{min}}$ ratio of 3.53. The Q-factor of the single-endedly tuned varactor setup is between 6 and 20, for a tuning voltage of 0 to 1.2 V. The post-layout simulation of the VCO yields a FTR from 38 to 45 GHz. This 16% tuning range is sufficient to support the complete 60 GHz band with some margin. The VCO consumes 5 mA from a 1.2 V supply and due to the only-NMOS topology the output differential swing of the VCO is larger as compared to a complementary structure. The simulated peak-to-peak amplitude is about 1.5 V.

A quadrature ILFD, shown on the right hand side of Fig.2, forms the second component of the PLL front-end. Two identical ILFD stages are coupled in anti-phase to generate quadrature outputs. The differential outputs of the VCO are injected to the input transistors M3 and M6

present in the two separate stages of the ILFD. The tanks of the ILFD stages are identical and oscillate at roughly half the VCO oscillation frequency. As the output swing of the VCO is sufficiently large, buffers are not required between the ILFD and VCO, which greatly simplifies the routing during layout and decreases the power consumption of the overall system. The injection transistor requires a different biasing voltage as compared to the DC-level of the VCO output, thus AC-coupling capacitors are used and the ILFD is biased independently. The value of the coupling capacitor is important as a capacitive divider is formed between the coupling capacitor and the gate-source capacitance of the injection transistor. If the former is chosen of the same order as the latter, part of the injection signal will be lost in the gate-source capacitance. Therefore, the coupling capacitor of 50 fF is chosen which is seven times the gate-source capacitance of 7 fF. At simulation level, some intentional loss is introduced in the injection signal to model the layout losses.

The synchronization of the tuning range of the VCO and locking-range of the divider is of utmost important. Therefore, the varactor setups of both components are co-designed such that the FTR of the VCO coincides with double the free-running FTR of the ILFD. Thus, the tuning voltages (V_{tune}) of both components can be tied

together for synchronized operation. This approach ensures that for each tuning voltage minimum power is required by the frequency divider for injection locking. In addition, for utilization in a complete PLL, the output of the loop-filter can be connected to both components for optimum operation.

III. LAYOUT AND TECHNOLOGY

The chip micrograph of the 40 GHz front-end, implemented in a 65nm bulk CMOS process, is shown in Fig. 3. The VCO, visible at the top, is placed as close as possible to the ILFD. All the transistors including VCO, ILFD and the output buffers are located in the encircled area. The buffered ILFD offers quadrature outputs but only one of these is measured and the other is terminated on-chip. The output transmission lines are 50 ohm matched for measurement purposes. The total chip area is $700 \times 500 \mu\text{m}^2$ where as the active core area occupies $80 \times 100 \mu\text{m}^2$.

IV. MEASUREMENT RESULTS

The front-end is measured on-wafer with the output from the ILFD observed on a spectrum analyzer. At first, the VCO is kept switched-off to measure the free-running frequency range of the ILFD. The tuning voltage is varied between 0 and 1.2 V. Shown in Fig. 4, the minimum and maximum free running frequency of the ILFD is 17.6 GHz and 21 GHz. The VCO is then switched ON with a supply voltage of 1.2V. At $V_{\text{tune}}=0$, the output is observed to lock at 18.8 GHz, which implies that the VCO is oscillating at 37.6 GHz (400 MHz lower than the corresponding

simulated frequency). The tuning voltage is then incremented and having a common V_{tune} for both components, moves them towards higher frequency in a synchronized manner. At 0.6 V, a locked spectrum at 19.9 GHz and at the maximum V_{tune} of 1.2, a peak at 21.1 GHz is observed. Thus, the total locking range referred to the input of the ILFD is from 37.6 GHz to 42.2 GHz (Fig. 4). The measured operation range of the front-end is very close to the target range of 38 to 42.3 GHz. A spectrum screen shot of a locked PLL front-end at 40.84 GHz is shown in Fig. 5. The locking is also observed for lower supply voltage of the VCO. However, as the output amplitude of injection signal decreases with the supply voltage, the locking range is correspondingly smaller. The DC-power consumption of the VCO and ILFD is 6 mW and 9 mW, respectively and the two common-source differential output buffers consume 12 mW.

Fig. 4. 40 GHz PLL front-end operation range and ILFD free-running frequency

Fig.3. Chip micrograph of the PLL front-end, the complete active core is placed between the three inductors

Fig. 5. Spectrum screenshot of a locked PLL front-end at 40.84 GHz

Fig. 6. Phase noise of the front-end in the locked and unlocked conditions

The phase noise of the synthesizer front-end is measured in two situations. First, in the free-running state of the ILFD and second in the locked state. In the former case, the phase noise is expected to be higher than the locked state. Fig. 6 shows the free-running and locked phase noise for a 19.9 GHz output frequency which falls in the center of the locking range. At 1 MHz offset the locked phase noise is 3.8 dB better than the free-running case whereas at lower offsets the difference is more profound. The variation of phase noise over the complete operation range of the front-end is ± 3.2 dB. The output power, after de-embedding the losses of the cables and other measurement equipment lies between -5 dBm and -8 dBm. The measured output power is an important parameter as the next divider stages in a PLL need to operate correctly with this (or even lower) power level. The variation of phase noise and output power is shown in Fig. 7.

Fig. 7. Variation of output amplitude and phase noise of the PLL front-end

V. CONCLUSIONS

We have presented a 40 GHz PLL front-end, comprising of a VCO and an ILFD, as an enabling component for a 40 GHz PLL. Such a PLL can be utilized in a sliding IF 60 GHz transceiver. Implemented in a bulk CMOS 65nm process, the front-end can lock from 37.6 to 42.2 GHz which corresponds to a down conversion range of 56.4 to 63.3 GHz, thus covering the complete 7 GHz bandwidth at 60 GHz. The front-end consumes 15mW from a 1.2 V supply and demonstrates a phase noise in the locked condition of -102.43 dBc/Hz at 1 MHz offset.

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