A CMOS Current Sensing Interface with Sub-pA DC Uncertainty

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Lin He, Hengzhuang Shi, Junhui Zhang, Mingxiang Wei, Ping Wang, Shunming Li, Hao Gao, *Member, IEEE*, and Zhikuang Cai

***Abstract*—This brief presents a CMOS current sensing interface with a dedicated analysis on dc uncertainty, especially the relationship among averaging, standard deviation and Allan variance. The dependence of the Allan variance on various noise sources is analyzed. The noise leakage mechanisms due to circuit nonidealities that lead to dc uncertainty are presented. A general design strategy toward a low dc uncertainty is drawn in this brief. An auto-zeroing (AZ) capacitive transimpedance amplifier (CTIA) is reported for near-zero signal loss and near-perfect noise cancelation to achieve a low dc uncertainty. A prototype design implemented on 180nm CMOS process is presented and the measurement result shows a 73fA dc uncertainty.**

***Index Terms*—Allan variance, current sensing interface, transimpendance amplifier, low noise.**

I. Introduction

BIO-SENSORS typically need to detect current signals ranging from pAs to nAs. In each bio-application, there is a dedicated current sensing interface circuit [1], such as whole cell patch-clamp recordings [2], [3], nanopore based DNA analysis [4], [5], [6], [7], [8], and pH detection based on ion sensitive field effect transistor (ISFET) [9]. Additionally, characterization of gate leakage current in CMOS technologies also needs sensing of small current [10].

Current sensing interface can be categorized into current-mode or transimpedance methods. A typical current-mode sensing interface includes current conveyors [1] and current-mode A-D converters [11]. A typical transimpedance sensing interface includes resistive transimpedance amplifiers (RTIA) [12] and capacitive transimpedance amplifiers (CTIA) [13], [14], [15]. In an RTIA scheme for picoampere detection, the feedback resistance must be large enough (i.e., $G\Omega$) to ensure high gain and low noise. A pseudo-resistor implemented by active devices is widely used to achieve such a huge resistance [6] with a reasonable die area. However, this pseudo-resistor is susceptible to process-voltage-temperature (PVT) variation. A linearization technique was reported in [6] to mitigate this issue.

CTIA contributes less noise and does not require a large chip area. However, for demanding applications such as gate leakage characterization or photodiode dark current measurement, where an extremely small dc current change has to be resolved, a simple CTIA is not sufficient. There might be dc measurement errors caused by amplifier offset, clock feedthrough, charge injection, and most importantly, flicker noise. Correlated double sampling (CDS) or auto-zeroing (AZ) is very effective in eliminating dc errors and is reported to be applied in a few CTIA based current sensing interface [10], [15]. A limitation of AZ is its increased white noise due to noise-folding. Averaging [14] can be used to narrow the signal bandwidth and obtain a higher resolution, but the ultimate limit of dc measurement remains an issue for the CTIA based current sensing interface employing AZ.

A systematic methodology is presented in this brief for a current sensing interface design flow for an optimized low dc measurement uncertainty. This brief is organized as follows. Section II briefly explains how the averaging method affects the Allan deviation and dc uncertainty. Section III presents the operation principle of the proposed AZ-CTIA, and analyzes the impact of the circuit nonlinearities on the dc uncertainty. Details of the circuit implementation is presented in Section IV. Section V gives the simulation and measurement result and the conclusion is drawn in Section VI.

II. Averaging and Dc Measurement Uncertainty

The mechanism of how the low frequency noise affects the averaged results can be explained in frequency domain. Averaging is essentially a cascaded integrator-comb (CIC) filter followed by a down-sampler. The transfer function of the CIC filter is given as

$$H_{CIC}(z) = \frac{1 - z^{-N}}{1 - z^{-1}} \tag{1}$$

where N is the number of averaging. The standard variance of the averaged sample is thus given as

$$\sigma^2(\overline{X}) = \int_0^\infty S_x(f) \frac{\sin^2(\pi N f T_s)}{sin^2(\pi f T_s)} df \tag{2}$$

where X is the discrete-time sample of signal x, $\overline{X}$ is the average of N consecutive samples of X, $S_x(f)$ is the PSD of X,

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Lin He, Hengzhuang Shi, Junhui Zhang, and Zhikuang Cai are with the College of Integrated Circuit Science and Engineering, Nanjing University of Posts and Telecommunications, Nanjing 210003, Jiangsu, China (e-mail: whczk@njupt.edu.cn).

Mingxiang Wei, Ping Wang, and Shunming Li are with the College of Energy and Power Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing, Jiangsu, China.

Hao Gao is with the Department of Electrical Engineering, Eindhoven University of Technology, 5612 AZ Eindhoven, The Netherlands.

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and T_s is the sampling period. If X is a white noise and $S_x(f)$ is flat, $\sigma^2(\overline{X})$ will scale with $1/N$. However, if $S_x(f)$ contains a $1/f$ component, the integral will go unlimited, which means averaging alone is not enough to get rid of the uncertainty. This is why precision measurements are usually done after real-time calibration. Multiple measurements with zero input are averaged and then subtracted from the subsequent measurements as an offset. The measurement error Y_i is therefore simplified as

$$Y_i = \overline{X_i} - \overline{X_{i-1}} \tag{3}$$

The standard variance of Y_i is thus given as

$$\sigma^2(Y) = \frac{\sum_{i=1}^{N} Y_i^2}{N-1} = \frac{\sum_{i=1}^{N} (\overline{X_i} - \overline{X_{i-1}})^2}{N-1} = 2\sigma_{Al}^2(X) \tag{4}$$

where $\sigma_{Al}^2(X)$ is the Allan variance of X. σ_{Al} is the Allan deviation, which is also known as the dc measurement uncertainty [16].

The Allan sequence $\overline{X_i} - \overline{X_{i-1}}$ is the discrete-time difference of $\overline{X_i}$. The transfer function of the discrete-time differentiator is given as

$$H_D(z) = 1 - z^{-N} \tag{5}$$

Allan variance can be derived from the power spectrum density as following

$$\sigma_{Al}^2(X) = \frac{1}{2}\int_0^\infty S_x(f)|H_{CIC}|^2|H_D|^2 df = 2\int_0^\infty S_x(f)\frac{\sin^4(\pi N f T_s)}{sin^2(\pi f T_s)} \tag{6}$$

If $S_x(f)$ is expressed as a sum of power-law dependent terms [17]

$$S_x(f) = h_{-2}f^{-2} + h_{-1}f^{-1} + h_0 \tag{7}$$

where the first term $h_{-2}f^{-2}$ is known as 'random walk', the second term $h_{-1}f^{-1}$ is known as 'flicker noise' or '$1/f$ noise', and the last term h_0 is the white noise.

the Allan variance calculated from (6) and (7) is given as [17]

$$\sigma_{Al}^2(X,N) \approx \frac{2NT_s\pi^2 h_{-2}}{3} + h_{-1}2\ln 2 + \frac{h_0}{2NT_s} \tag{8}$$

This is a V-shape curve (Fig. 1) with a minimum value given as

$$\sigma_{Al,min}^2(X) = 2\pi\sqrt{\frac{h_{-2}h_0}{3}} + h_{-1}2\ln 2 \quad (@N = \frac{1}{2T_s\pi}\sqrt{\frac{3h_0}{h_{-2}}}) \tag{9}$$

As (9) shows, $h_{-1}f^{-1}$ contributes a constant Allan variance. AZ is known for $1/f$ noise cancelation, which is suitable for Allan variance rejection. $h_{-2}f^{-2}$, which contributes to the square root term in (9), is also canceled through AZ. However, due to the circuit nonidealities, the noise cancelation is imperfect, resulting in a residue Allan variance. Additionally, suppose the second term in (9) dominates, consuming more power might not be effective for stability improvement, as the first term is inversely proportional to the square root of the power consumption.

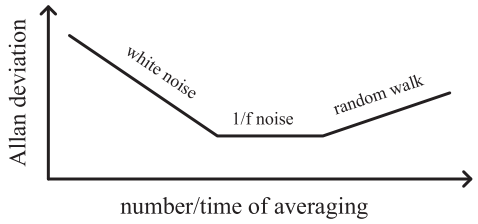

Fig. 1. Allan variance as a function of averaging number/time.

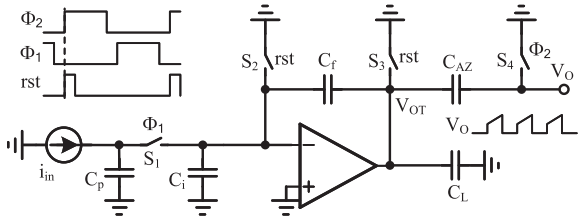

Fig. 2. Simplified schematic and timing diagram of proposed AZ-CTIA.

III. Circuit Principle and Noise Analysis

A. Proposed Operation Principle

A modified AZ-CTIA scheme is proposed, as in Fig. 2. A switch S_1 is inserted at the input of the CTIA to disconnect I_{in} from the CTIA during the auto-zeroing phase. The operation of the proposed CTIA is described as follows. At the reset phase (rst=1), I_{in} is disconnected and C_f is discharged through switch $S_{2,3}$. At the auto-zeroing phase (rst=0 & ϕ_2=1), $S_{2,3}$ turn off. The offset and the flicker noise are amplified and stored on C_{AZ}. During ϕ_1, I_{in} is reconnected to the CTIA and integrated on C_f. The stored error on C_{AZ} is subtracted from the final output of the amplifier which results in a clean output V_O at the right side of C_{AZ}.

In the proposed AZ-CTIA, I_{in} is no longer lost during ϕ_2, but is temporarily stored on C_p, the parasitic capacitance at the input node, as a form of charge accumulation which is transferred to C_f during ϕ_1. The signal power is thus increased.

B. Noise Leakage Due to Circuit Nonidealities

A switched-capacitor circuit will experience a settling process. If the settling errors differ from phase to phase, the calibrated output V_O at the end of ϕ_1 will contain a residue error.

At the end of phase ϕ_2 ($t = (n+0.5)T_s$, where T_s is the clock period, in the presence of the amplifier offset voltage V_{os}, the amplifier output V_{OT} is given as

$$V_{OT}(n+0.5) = -\frac{A(C_i + C_f)}{C_i + C_f + AC_f}V_{os}(n+0.5) \tag{10}$$

where A and C_i are the gain and input capacitance of the amplifier. During phase ϕ_1, C_p is reconnected to the amplifier and the charge stored in previous period is redistributed. At

the end of phase ϕ_1 ($t = nT_s$), the z transform of the amplifier output associated with V_{os} is given as

$$V'_{OT}(z) = -\frac{A[(C_i + C_f) + (1 - z^{-1})C_p]}{C_i + C_f + (1 - z^{-1})C_p + AC_f} V_{os}(z) \quad (11)$$

At dc ($z = e^{j0}$),

$$V'_{OT}(e^{j0}) = -\frac{A(C_i + C_f)}{C_i + C_f + AC_f} V_{os}(e^{j0}) \quad (12)$$

Eq. (12) has the same scale factor as that in (10). In other words, despite of the difference in feedback factors, both ϕ_1 and ϕ_2 have the same static settling error and a close-to-ideal cancelation can be realized. This condition is achieved by the compensation effect of the charge stored in C_p in the previous period.

The flicker noise can be treated as a slow-varying offset and will be rejected through AZ. The above analysis is under a practical boundary condition that the dynamic settling errors are sufficiently small so that the static error will dominant.

C. Noise Analysis

As (9) shows, the minimum Allan variance is proportional to the square root of the white noise. At the end of phase ϕ_1, The z-transform of the output noise at node V_o is given as

$$V_{on}(z) = (1 - z^{-0.5})\frac{C_i + C_f}{C_f} V_{nop}(z) + (1 - z^{-1})\frac{C_p}{C_f} V_{nop}(z) - z^{-1}\frac{C_p}{C_f} V_{n,p}(z) + z^{-0.5} V_{n,AZ}(z) \quad (13)$$

where V_{nop} is the input referred noise of the amplifier, $V_{n,AZ}$ is the kTC noise frozen on C_{AZ} due to the switching of S_4, and $V_{n,p}$ is the kTC noise frozen on C_p due to the switching of S_1.

Based on the analysis in [18], the noise power spectrum (PSD) of V_{on} is given as

$$S_{on}(f) \approx [\frac{V_{n,AZ}^2 T_s}{2} + \frac{V_{n,p}^2 C_p^2 T_s}{2C_f^2}]\frac{\sin^2(\pi f T_s)}{(\pi f T_s)^2} + \frac{(C_i + C_f)^2 + C_p^2}{2C_f^2}\pi f_{-3} T_s S_{n,w} + \frac{(C_i + C_f)^2 + 9C_p^2}{16C_f^2}(\pi f T_s)^2 S_{1/f}(f) \quad (14)$$

where $S_{1/f}$ is the PSD of the $1/f$ noise component at the amplifier input, $S_{n,w}$ is the PSD of the white noise component at the amplifier input, f_{-3} is the -3dB noise bandwidth of the amplifier, and T_s is the sampling period. The first two terms in (14) correspond to white noise, and the last term is the high-passed $1/f$ noise, which will result in a noise with its PSD proportional to f. The last term can be practically ignored.

The variance of $V_{n,p}$ is calculated by integrating the noise PSD over the entire frequency range [19] and approximated as

$$V_{n,p}^2 \approx \frac{kT}{C_p}\frac{C_i + C_f}{C_i + C_f + C_p} \quad (15)$$

It shows that the kTC noise frozen in C_p is significantly smaller than a typical kTC noise from a simple switch-capacitor circuit. The feedback loop following S_1 serves as a low-pass filter for both the amplifier noise and the thermal noise of the switch on-resistance. However, this thermal noise is usually much smaller than the amplifier noise due to the settling consideration, and is practically ignored.

In the proposed AZ-CTIA, the noise performance is almost unaffected and the signal gain is increased. The introduction of switch S_1 reduces the input referred current noise without sacrificing the dynamic range performance.

IV. Circuit Implementation

A. Design Strategy

Both the residue low frequency noise and the white noise have to be minimized for designing a current sensing interface with extremely low dc uncertainty. A low noise, high gain and fast-settling amplifier is required to take full advantage of the proposed AZ-CTIA for low-frequency noise rejection.

B. Pseudo-Differential AZ-CTIA

In this design, a pseudo-differential AZ-CTIA (shown in Fig. 3) is adopted for single-ended current sensing to take advantage of differential structure and therefore suppress the common-mode (CM) errors such as charge injection and clock feedthrough.

The total parasitic capacitance at the input node varies from case to case and is nearly impossible to perfectly match it using an on-chip capacitor. To avoid common-mode to differential conversion due to capacitance mismatch, an extra input common-mode feedback (ICMFB) circuit is added, as shown in the dashed box in Fig. 3. The auxiliary amplifier G_{m2} in this ICMFB loop senses the input common mode using two split negative inputs, and feeds-back to the main amplifier inputs through $C_{ifb\pm}$ to stabilize the input CM. A dummy capacitor C_{dum} is placed at the symmetrical position to partially balance C_p.

Because of the mismatch between C_{dum} and C_p, the noise from the auxiliary amplifier will undergo a CM to DM conversion with a ratio given by $(C_{dum} - C_p)/(C_{dum} + C_p)$. The converted noise is added directly to the AZ-CTIA input and will be processed by AZ. Given a G_{m1}/G_{m2} ratio of 4, a 30% mismatch between Cdum and Cp leads to a 6.8% increase on the input referred noise power.

C. Low-Noise Main Amplifier

A folded cascode gain-boosted topology is adopted in the G_{m1} design for large input common-mode range and high gain. PMOS input differential pair is adopted for low input referred noise. The four cascoded current sources were resistively degenerated to further suppress the low frequency noise. Compensation capacitors are placed at the outputs of the gain-boosting auxiliary amplifiers to optimize the location of pole-zero doublets and therefore ensure a fast settling.

D. Leakage Control

The off-state leakage current of S_1 is critical. In this design, S_1 is implemented as two stacked NMOS transistors with an internal capacitor C_{IT} [20] (Fig. 3) for leakage reduction. While S_1 switches off, I_{in} charges C_p, and the leakage current

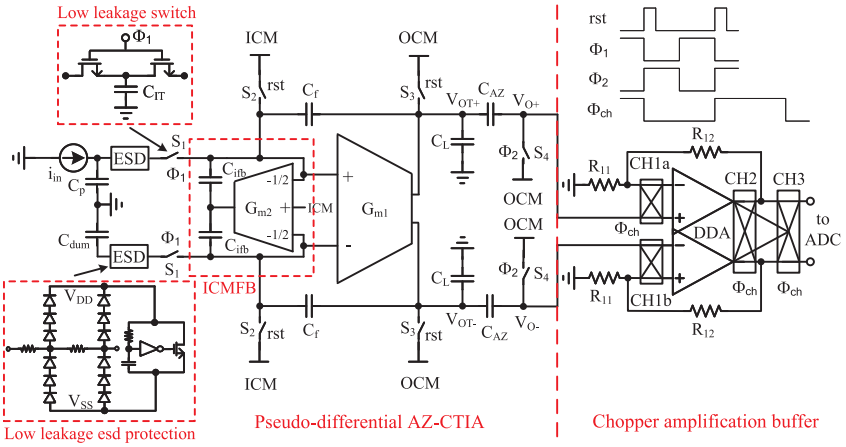

Fig. 3. Schematic diagram of the current sensing interface, including a Pseudo-differential AZ-CTIA and a chopper amplification buffer.

affects the voltage of C_{IT} first. The off-resistances of the two transistors in S_1 and C_{IT} form a T-shape ladder filter, which delays the leakage charge transfer to the amplifier. With proper sizing of C_{IT} (10fF in this design), the total charge leaked to the right side of S_1 can be significantly reduced.

A dedicated low leakage ESD protection circuit [21](Fig. 3) based on stacked diodes is used in this design. The voltage across each diode and the leakage current are both reduced. The ESD circuit consists of two stages of stacked diodes. Resistor R_1 and R_2 are used to limit the current during an ESD event. The same ESD circuit is added to the dummy input node for common-mode leakage rejection.

E. Chopper Amplification Buffer

A chopper amplification buffer is introduced to amplify the differential output signal from the AZ-CTIA and suppress the common-mode transients. Moderate low-frequency noise cancelation is required for this module to maintain the performance of the AZ-CTIA. The amplification buffer is configured as a non-inverting one around a chopper differential difference amplifier (DDA), as is shown in Fig. 3. The DDA is a variant of two-stage miller compensated operational amplifier with class-AB output stage. The first stage is a folded cascode transconductor with two pairs of PMOS inputs. The second stage is a rail-to-rail output stage with floating class-AB control. The output of the chopper amplification buffer is chopped again before AD conversion. Demodulation is performed in the digital domain to remove the low-frequency noise from the ADC itself.

V. Measurement Results

A prototype is fabricated using a 180nm CMOS process, and its main parameters are shown in Table I. This prototype is designed for the device characterization application with a target dc measurement uncertainty below 0.1pA. The die microphotography is in Fig. 5. The core area of the chip is $300\times310\mu m^2$. The clock generator receives a LVDS input and converts it into a rail-to-rail multiphase clock. The power and noise breakdown is shown in Fig. 4. In the measurement setup, the chip under test is covered by a shielding box to eliminate electromagnetic interference. A 50mV_{p-p} 200Hz ac

TABLE I
Main Parameters of the CMOS Current Sensing Interface

Device	value	device	value	device	value
C_f	0.2pF	C_p,C_{dum}	4pF	C_{in}	55fF
C_{AZ}	1pF	C_{ifb}	0.4pF	C_L	0.5pF
R_{11}	10kΩ	R_{12}	50k Ω	G_{m1}	1.6mS
A_{Gm1}	120dB	A_{DDA}	90dB	G_{m2}	0.4mS
ESD diode	$100um^2$	$\phi_{1,2}$	15kHz	ϕ_{ch}	7.5kHz

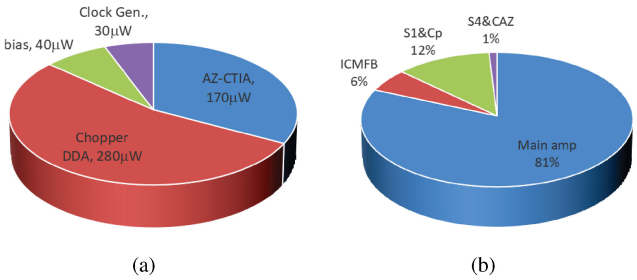

Fig. 4. (a) Power breakdown of the sensing interface prototype and (b) noise breakdown of the AZ-CTIA.

voltage is applied on a 0.55pF MLCC capacitor to generate the input current. This ensures that the input current is free of low frequency noise. The modulated output is further amplified using a commercial amplifier and sampled using a 10bit commercial ADC at 1MHz sampling frequency. The sampled output is then demodulated with the chopping frequency, and the demodulated output is then averaged every 5m seconds to remove the 200Hz component. This averaged output is actually the baseline signal of this measurement setup. The Allan deviation of the averaged output is shown in Fig. 6. It reached a minimum value of 73fA at roughly 1s average time. This brief is compared with the prior arts in Table II.

VI. Conclusion

This brief presents a structural design methodology for a CMOS current sensing interface with ultra-low dc measurement uncertainty. The relationship among averaging, calibration, noise power spectrum, Allan variance, and dc measurement uncertainty is analyzed in this methodology. A dedicated auto-zeroing capacitive transimpedance amplifier

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	[22]	[13]	[23]	[24]	This work
Topology	CTIA +ΔΣ	CC	Passive +ΔΣ	CTIA +ΔΣ	AZ +CTIA
Tech. (nm)	500	130	350	180	180
Supply (V)	3.3	1.2	1.5	1.8	3.3
Area (mm^2)	0.085	0.05	0.5	0.11	0.1
Power (μW)	11	3	16.8	50.3	520
C_f (pF)	NA	10	10	NA	0.2
C_{in} (pF)	NA	NA	10	NA	5
f_{ck} (kHz)	250	20	500	5	15
DR (dB)	62	92.2	77.5	78.2	80
IRN ($fA/\sqrt{Hz}$)	130	70	6960	30.3	36
Allan Dev.	NA	NA	NA	NA	73 fA @ 1 s

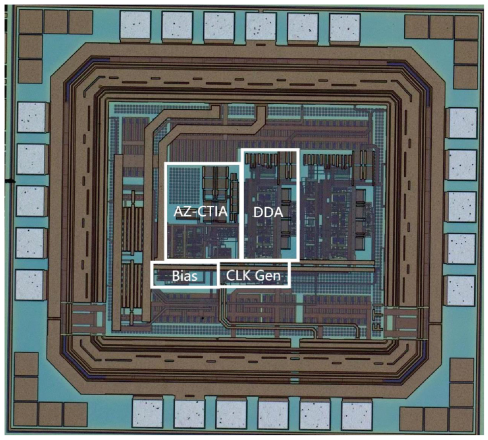

Fig. 5. Chip microphotograph.

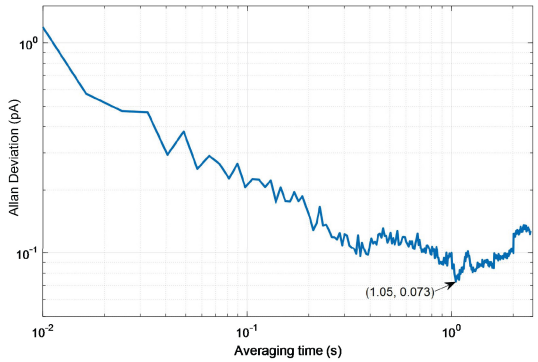

Fig. 6. Allan deviation plot derived from the demodulated output.

(AZ-CTIA) topology is proposed for near-zero signal loss and near-perfect noise cancelation. A prototype design in a 180nm CMOS technology is implemented and the measurement result achieves a 73fA minimum dc uncertainty at 1s averaging time.

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