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A Systematic Design Approach for Phased-array Receivers

Wei Deng, Reza Mahmoudi, Arthur van Roermund

Department of Electrical Engineering, Mixed-signal Microelectronics group, Eindhoven University of Technology, 5600 MB, Eindhoven, The Netherlands

Abstract — Phased-array receivers are popular electronic systems due to the advantages of signal to noise ratio (SNR) improvement and interference cancellation. However, they are mostly discussed on circuit level, and it is hardly seen any systematic design approach for phased-array receivers in general. The scope of this paper is to analyze the difference between phased-array and single-chain receivers from noise and linearity perspectives, and provide a systematic design approach to minimize the overall power consumption.

Index Terms — System analysis and design, phased-array, receivers, noise, linearity.

I. INTRODUCTION

Phased-array receivers are important electronic systems that have a wide range of applications. Compared with a single-chain receiver, two of the main benefits that array-system can provide are signal to noise ratio (SNR) enhancement and interference cancellation. Topics about phased-array circuits have been widely discussed [1]. To improve the system performance further, not only the circuit design but also the system design needs to be optimized. The scope of this paper is to optimize the phased-array receivers from noise and linearity perspectives, and provide a systematic design approach to minimize the overall power consumption.

With a single-chain receiver, important system parameters are front-end gain (G_{FE}), noise figure (NF_{FE}), and third order input intercept point ($IIP3_{FE}$), ADC noise figure (NF_{ADC}) and third order input intercept point ($IIP3_{ADC}$) [2]. With a phased-array receiver, three more system parameters are added as shown in Fig. 1, antenna number n , desired incidence angle θ_d , and interferer incidence angle θ_i . The general principles of phased-array system are as follow:

- 1) Desired signals are adding in-phase.
- 2) Noises are adding in power.
- 3) Interferers are adding out-of-phase.

The impact of adding additional parameters to the system noise and linearity performance will be separately discussed in section II. Section III uses IEEE 802.11a standard as an example to demonstrate the systematic design approach of the phased-array receiver to meet the standard requirements with minimum overall power consumption.

Fig. 1. Phased-array receiver.

II. ARRAY SYSTEM NOISE AND LINEARITY ANALYSIS

Depending on the location where the required phase shifter performed, phased-array can be classified as RF, LO, IF or digital beam-forming. In this paper, we take the RF beam-forming architecture as an example.

A. Phased-array noise analysis

Fig. 2(a) shows a phased-array receiver in which signal and noise power level at the antenna inputs are S_{in} and N_{FL} , respectively. Front-end (FE) equivalent noise power (N_{FE}) is referred to the input. Front-end gain (G_{FE}) enlarges signal as well as noise. Analog to digital converter (ADC) converts analog signal into digital domain, but also adds quantization noise (N_{ADC}). Assuming a unity gain ADC and a lossless & noise-free phase shifter which combines signal and noise from each path, at point A, the correlated signals from all antenna inputs are added in voltage, nevertheless, the uncorrelated noise from each path are added in power, yielding:

$$S_A = S_{in} \cdot (n^2 \cdot G_{FE}) \quad (1)$$

$$N_A = (N_{FL} + N_{FE}) \cdot n \cdot G_{FE} = \left(\frac{1}{n} \cdot N_{FL} + \frac{1}{n} \cdot N_{FE}\right) \cdot (n^2 \cdot G_{FE}) \quad (2)$$

From (1) and (2), we are able to project phased-array receiver in Fig. 2(a) into an equivalent single-path structure in Fig 2(b). The equivalent values for N_{FL} , N_{FE} and G_{FE} are $(1/n) \cdot N_{FL}$, $(1/n) \cdot N_{FE}$ and $n^2 \cdot G_{FE}$, respectively. All the blocks after point A are maintained. Note that

Fig. 2. (a) Phased-array receiver on block level. (b) Equivalent single-path structure for (a).

$n^2 \cdot G_{FE}$ consists by two parts, antenna array gain n^2 , and front end gain G_{FE} . From Fig. 2(b), we can derive the input referred total noise power as:

$$N_{tot,in} = \frac{1}{n} \cdot N_{FL} + \frac{1}{n} \cdot N_{FE} + \frac{1}{n^2 \cdot G_{FE}} \cdot N_{ADC} \quad (3)$$

Hence, the total noise factor (F_{tot}) of the phased-array receiver is:

$$F_{tot} = \frac{N_{tot,in}}{N_{FL}} = \frac{1}{n} \cdot \left(1 + \frac{N_{FE}}{N_{FL}} \right) + \frac{1}{n^2 \cdot G_{FE}} \cdot \frac{N_{ADC}}{N_{FL}} \quad (4)$$

The equivalent Friis noise equation for phased-array is:

$$F_{tot} = \frac{1}{n} \cdot F_{FE} + \frac{1}{n^2} \cdot \frac{F_{ADC} - 1}{G_{FE}} \quad (5)$$

where F_{FE} and F_{ADC} represent noise factor of the front-end and ADC, respectively. It is obviously to see that due to the antenna array gain, both front-end and ADC input referred noises are reduced.

A design flow for a single-path receiver which indicates four variables that can be used for the trade-off between RF and ADC blocks was reported in [2]. To optimize the phased-array receiver performance, we can generate the phased-array noise power (mW) flow diagram in Fig. 3, where N_{tot} is the equivalent total noise referring to ADC input, and N_{FE} is the different between N_{tot} and ADC noise N_{ADC} . N_{FE} can be expressed as:

Fig. 3. Phased-array noise power (mW) flow diagram.

$$\Delta N_{FE} = \frac{F_{tot} \cdot n^2 \cdot G_{FE}}{F_{ADC}} \quad (6)$$

Combining (5) and (6), the noise figure of front-end and ADC can be derived in (7) and (8), respectively.

$$NF_{FE}[dB] = 10 \log \left[n \cdot 10^{\frac{NF_{tot}}{10}} \cdot \left(1 - 10^{\frac{\Delta N_{FE}}{10}} \right) + \frac{1}{n} \cdot 10^{\frac{G_{FE}}{10}} \right] \quad (7)$$

$$NF_{ADC}[dB] = NF_{tot} + G_{FE}[dB] - \Delta N_{FE}[dB] + 20 \log n \quad (8)$$

We can see that NF_{FE} has a direct relation with N_{FE} , and NF_{ADC} has a reverse relation with N_{FE} . Keeping NF_{tot} , G_{FE} , and n constant, adjusting N_{FE} can result in the trade-off between front-end and ADC noise.

B. Phased-array linearity analysis

In a single-chain receiver, the linearity performance reflects on the third order input intercept point (IIP3). It is in many cases dominant by the interferer instead of the desired signal. Phased-array receiver has the advantage of enhance the desired signal by adding them in-phase, and reject the unwanted interferer (from another angle) by adding them out-of-phase. This property can be expressed in (9) as:

$$S_{SUM} = \sum_{k=0}^{n-1} A(t) \cdot e^{j2\pi f_c t} \cdot e^{j(k-1)\Delta\phi} \cdot e^{-j(k-1)\Delta\phi} \quad (9)$$

where $A(t)$ is the amplitude of the coming signal and f_c is the carrier frequency. $\Delta\phi$ is the input signal phase difference (can be either desired or unwanted signal), and $\Delta\phi$ is the phase compensation (for desired signal) on each path. Further more, assuming antenna spacing $d = \lambda/2$ (λ is the signal wavelength), the space angle (deg) can be transferred to phase difference by:

Fig. 4. Phased-array antenna gain patterns, when $n=1, 2, 4, 8$, assuming desired signal coming from 0° .

$$\Delta\phi = \frac{2\pi}{\lambda} \cdot d \cdot \sin\theta = \pi \cdot \sin\theta \quad (10)$$

Assuming normalized signal amplitude, $A(t)=IV$, combining (9) and (10), and taking only the absolute amplitude of S_{SUM} , normalized array gain, A_{SUM} , can be expressed as,

$$A_{SUM} = \left| \sum_{k=0}^{n-1} e^{j(k-1)\pi\sin\theta} \cdot e^{-j(k-1)\Delta\phi} \right| \quad (11)$$

When $n=1$, it is a single antenna receiver without any directivity. Hence, the array gain is unity for all incidence angles. When $n \neq 1$, multiple antennas produce antenna patterns which are function of n , θ_i , and θ_d . Assuming $\theta_d = 0^\circ$, adjusting $\Delta\Phi$ to the desired signal results $\Delta\Phi=0$. A_{SUM} can be expressed in (12), and plotted in Fig. 4 with $n=1, 2, 4, 8$ as examples.

$$A_{SUM}[dB] = 20 \log \left| \sum_{k=0}^{n-1} e^{j(k-1)\pi\sin\theta} \right| \quad (12)$$

Defining a function $L(n, \theta_i, \theta_d)$ that describes any points on Fig. 4. For example, the value of point M is $L(n=4, \theta_i=35^\circ, \theta_d=0^\circ)=-5dB$. The suppression of point M from the peak ($n=4$) is $12dB - (-5dB) = 17dB$. Introducing $L(n, \theta_i, \theta_d)$ to Fig. 2(a), one can find the equivalent gain for the interferer signal at point A : $G_{FE} + L(n, \theta_i, \theta_d)$. Assuming interferers dominant the receiver linearity performance, equivalent Friis linearity equation for phased-array is:

$$\frac{1}{IIP3_{tot}} = \frac{1}{IIP3_{FE}} + \frac{L \cdot G_{FE}}{IIP3_{ADC}} \quad (13)$$

Fig. 5. Phased-array distortion power (mW) flow diagram.

According to [2], we can generate the phased-array distortion power (mW) flow diagram in Fig. 5, where D_{tot} is the equivalent total distortion power referring to ADC output, and D_{FE} is the different between D_{tot} and ADC distortion power D_{ADC} . D_{FE} can be expressed as,

$$\Delta D_{FE}[dB] = 2 \cdot (IIP3_{ADC} - IIP3_{tot} - G_{FE} - L) \quad (14)$$

Combining (13) and (14), the $IIP3_{FE}$ and $IIP3_{ADC}$ can be derived in (15) and (16), respectively.

$$IIP3_{FE}[dB] = -10 \log \left(10^{\frac{IIP3_{tot}}{10}} - 10^{\frac{0.5 \cdot \Delta D_{FE} + IIP3_{tot}}{10}} \right) \quad (15)$$

$$IIP3_{ADC}[dB] = \frac{1}{2} \cdot \Delta D_{FE} + IIP3_{tot} + G_{FE} + L(n, \theta_i, \theta_d) \quad (16)$$

It shows that $IIP3_{FE}$ has a reverse relation with D_{FE} , and $IIP3_{ADC}$ has a direct relation with D_{FE} . Keeping $IIP3_{tot}$, G_{FE} , and L constant, adjusting D_{FE} can result in the trade-off between front-end and ADC linearity.

III. SYSTEMATIC DESIGN FOR PHASED-ARRAY RECEIVER

The predefined specifications of wireless standards are determining today's design strategy. Standards usually include: bandwidth of the signal (BW), minimum signal to noise and distortion ratio ($SNDR_{min}$) (derived from BER and modulation scheme), minimum detectable signal power ($P_{S,min}$), desired signal power ($P_{S,want}$) and interferer power (P_{Int}) for inter-modulation characterization. This allows us to determine the receiver total noise figure and total input intercept point, as:

$$NF_{tot}[dB] = P_{S,min} - SNDR_{min} - 10 \log(kT \cdot BW) \quad (17)$$

$$IIP3_{tot}[dB] = \frac{P_{Int} - P_{S,want} + SNDR_{min}}{2} + P_{Int} \quad (18)$$

Taking IEEE 802.11a standard [3] as an example, utilizing (17) and (18), we can calculate that $NF_{tot}=15dB$ and $IIP3_{tot}=-26dBm$. Assuming the desired signal coming from 0° ($\theta_d=0^\circ$), interferer coming from 35° ($\theta_i=35^\circ$), when $n=4$, we can get $L=-5dB$. Substitute NF_{tot} , $IIP3_{tot}$, and L into (7), (8), (15), and (16). We can plot NF_{FE} vs N_{FE} , NF_{ADC} vs N_{FE} , $IIP3_{FE}$ vs D_{FE} , and $IIP3_{ADC}$ vs D_{FE} with various G_{FE} and n combinations in Fig. 6(a), (b), (c), and (d), respectively. By choosing various sets of (N_{FE} , D_{FE}), we can get various sets of (NF_{FE} , NF_{ADC} , $IIP3_{FE}$, $IIP3_{ADC}$, G_{FE} , n) to meet system requirements. Targeting for minimum system power consumption, we can derive the overall system power relation in (19),

$$P_{sys} = n \cdot P_{C,FE} \cdot 10^{\frac{G_{FE} + IIP3_{FE} - NF_{FE}}{10}} + P_{C,ADC} \cdot 10^{\frac{IIP3_{ADC} - NF_{ADC}}{10}} \quad (19)$$

where $P_{C,FE}$ and $P_{C,ADC}$ denote the power coefficient of the front-end and ADC, respectively. With fixed $P_{C,FE}$ and $P_{C,ADC}$, we can find one set of (N_{FE} , D_{FE}) results in the minimum system power consumption.

IV. CONCLUSION

This paper has presented a systematic design approach for phased-array receivers. It started with analyzing the difference between phased-array and single-chain receivers from noise and linearity perspectives, and then provided a systematic design approach to minimize the overall power consumption.

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Fig. 6. (a) NF_{FE} vs N_{FE} , (b) NF_{ADC} vs N_{FE} , (c) $IIP3_{FE}$ vs D_{FE} , (d) $IIP3_{ADC}$ vs D_{FE} .