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Receiver Front-End Circuits for Future Generations of Wireless Communications

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Abstract—In this paper, new receiver concepts and CMOS circuits for future wireless communications applications are introduced. The concepts derived are applied to a few classes of wireless communications standards that are broad-band at radio frequencies and/or require a broad-band baseband circuitry. Multimode multiband operation and adaptivity as key requirements for future generation receivers are highlighted throughout the paper. The tradeoffs between power consumption, noise figure and linearity performance of low-noise amplifiers, mixers, and intermediate frequency filters are considered too.

Index Terms—Broad-band radio frequency (RF), multiband circuits, multimode circuits, RFCMOS.

I. INTRODUCTION

THE number of systems that use radio links and the number of standards for such systems are both increasing very quickly. Many applications require multiple radio links, either for different purposes (e.g., a Bluetooth link in a cellular phone) or for compatibility with different systems at various locations (e.g., different types of cellular phone networks in different countries). In order to increase flexibility and functionality of the RF transceivers, cost-effective and multistandard RF design solutions are needed [1]–[4]. The challenge is to design a multimode, multiband receiver that fulfills the requirements of different standards simultaneously [5], [6].

From the application perspective, the standards for cellular (personal) communications (GSM-850/GSM-900/DCS/PCS), the standards for wireless local area network (WLAN) access (802.11a and 802.11b-g) and the standards for short-range communications (Bluetooth) could be supported with one receiver and distributed selectivity. The assumption here is some form of off-chip RF filtering. A high level of integration and reduced number of external discrete components will further reduce the costs, but this will make the design even more difficult. If the low-noise amplifier (LNA) is designed to support more operating frequencies, the control of the design parameters becomes more

complex in order to keep the correct input matching at different frequencies without degrading the gain, noise figure (NF) and linearity. In this paper, the key enablers of a multistandard single-chip solution are a broad-band LNA (e.g., with resistive feedback) and an active BALUN that fulfill all the noise and linearity specifications required by different standards. The extensive use of negative feedback and the lack of integrated inductors result in broad-band operation (850 MHz–6 GHz) and process invariance with small footprint. Another key enabler is a high-linearity *IQ* down-conversion mixer and low-pass filter (LPF) with harmonic rejection. The receiver can operate in zero intermediate frequency (IF) or low-IF mode depending of the desired standard. A flexible LPF provides IF selectivity before analog-to-digital (A/D) conversion. The RX front-end can also work at the lower part of the UWB spectrum and is closely related to the IF part of a multi-Gb/s WPAN (IEEE802.15.3.c) receiver.

The bandwidth congestion and a spectral-efficiency minded design philosophy have pushed the spectral efficiency of the existing radio solutions beyond the robustness limit of 5 bits/s/Hz. The assignment of free bandwidth in the millimeter-wave (mm-wave) frequency range has sparked interest in using silicon RF integrated circuits for operation in those bands. The direct relationship between the channel capacity and bandwidth points toward less spectrally efficient radio solutions in the millimeter wave bands; additionally, it opens a new era in the radio design where robustness is at stake. These radios are broad-band in nature at IF and the techniques applied in the multimode, multiband radio solutions can be applied as well to the IF part of a mm-wave receiver front-end (e.g., 60 GHz). A tunable IF filter (e.g., 1.7–6 GHz) is considered as another key enabler of future wireless communications (multi Gb/s WPAN) in this paper. The filter employs the broad-band LNA and the high linearity mixers of the first solution for amplification/bandwidth control and passive poly-phase filters (PPFs) for selectivity. The organization of the paper is as follows: in Section II, the basic operation of the resistive-feedback LNA, active BALUN and *IQ* mixer is described. Their gain, NF and linearity performance is further analyzed in this section. A tunable IF filter for a mm-wave receiver front-end is presented in Section III. Section IV is reserved for conclusions.

II. MULTIBAND RECEIVER FRONT-END

The broad-band receiver front-end is shown in Fig. 1. A broad-band, inductor-less LNA is the first building block in the RF chain. The active BALUN, with some power gain, converts the single-ended signal into a differential signal. A harmonic reject (HR) mixer converts the RF signal to low/zero-IF and the output of the mixer is applied to a transimpedance amplifier configured as a LPF. An eight-phase generator provides the required local oscillator (LO) phases to the HR mixer. The sampled-data

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Fig. 1. Broad-band receiver front-end.

Fig. 2. Simplified circuit diagram of the broad-band LNA.

filter ensures IF selectivity and has a tunable bandwidth. As less selectivity is applied in the RF channel selectivity is achieved at IF. A LNA with resistive feedback and a frequency range of 0.5–6 GHz is introduced in [7]. It operates at a higher supply voltage and has higher power dissipation (42 mW @ 2.7 V).

In this section, a CMOS090LP broad-band resistive feedback LNA with a low NF is proposed [2]. Total dissipation of the IC is 16.8 mW at a supply voltage of 1.2 V. The broad-band inductor-less LNA with resistive feedback is depicted in Fig. 2. The first stage in the feedforward path of the LNA is a common-source amplifier. A cascode transistor *Mn2* increases the output impedance and the reverse isolation of the common-source amplifier *Mn1*. In the cascode amplifier, the load resistor *Rd1* is stacked on top and some dc current flows through this configuration. As at low supply voltages the voltage drop across the load resistor and transistors becomes critical, a pMOS transistor *Mp1* is used. Then, a part of the dc current flows through the pMOS transistor and the total ac current ideally flows through the transistor *Mn2* and the load resistor. The second stage in the feedforward path of the LNA is a voltage-to-current converter. The source follower *Mn3/Mn4* is an active voltage follower. Hence, the voltage at node C will track the output voltage of the first stage (V_B). The current of transistor *Mn3* is ideally constant and equal to I_{bias} . The voltage signal VC is converted in a current on the R_m , C_m series combination and the transistor *Mn4*. A level-shifter provides the dc bias of *Mn4*. The current of the transistor *Mn4* is transferred, with some gain, to the transistor (*Mn5*) of the output stage of the LNA. The output current is converted into voltage on the load resistor *Rd2*. The feedback resistor *Rf* is dc blocked by *Cf1*, while *Cf* is used to control peaking at higher

Fig. 3. Active BALUN.

Fig. 4. HR mixer and LPF.

frequencies and plays a role in input matching. At moderate frequencies and for sufficiently high C_m , the voltage gain can be approximated by

$$G \cong \frac{A_{V0}}{\left(1 - \frac{R_s}{R_f} A_{V0}\right)} \quad (1)$$

where A_{V0} is the voltage gain of the feedforward path of the LNA. The voltage gain of the feedforward path of the LNA can be increased by increasing the current gain between the second and third stage of the LNA, and by increasing the ratio of the load resistors in the corresponding stages. At lower frequencies, the bandwidth of the LNA will extend by increasing the $R_m * C_m$ product. At high frequencies, the parasitic capacitances of the transistors, especially from the first stage, will determine the 3-dB bandwidth of the broad-band LNA. The input matching, at moderate frequencies, is set by

$$R_{in} = \frac{R_f}{1 - A_{V0}} \cong -\frac{R_f}{A_{V0}}. \quad (2)$$

The *NF* of the LNA is determined by the noise contribution of the first stage and the feedback resistor *Rf*. For a large value of *Rm* and a high $R_m/Rd1$ ratio, the noise of the second and third stages contributes to the total *NF*. The linearity performance of the LNA depends on many parameters. In the first stage, it is determined by the overdrive voltage of the transistor *Mn1*, and the voltage swing at nodes A and B. Therefore, the linearity of the first stage can be improved by increasing the overdrive voltage

Fig. 5. Clock generation for HR mixer.

of $Mn1$ and keeping the transistors $Mn1$, $Mn2$, and $Mp1$ far from the linear region. In the second stage, the nonlinearity will be determined by the voltage swing at node C , the bias current I_{bias} and the resistor R_m . Hence, the linearity of the second stage can be improved by reducing the voltage swing at the node C , increasing R_m and/or increasing I_{bias} . The overdrive voltage of the transistor $Mn5$ and the voltage swing at the node D will determine the nonlinearity of the third stage. From this analysis we conclude that the NF of the circuit under consideration can be traded off for linearity. The measured power gain of the LNA is around 22 dB, and the 3-dB bandwidth is 6 GHz. The best NF is 2.5 dB at 2.7 GHz and increases gradually, at the end of the band, up to 3.1 dB. The input matching ($S_{11} < -10$ dB) is achieved in the frequency range of $0.9 \div 7$ GHz. For an input signal up to -30 dBm the measured third-order input intercept point (IIP3) (two-tone test) is -3 dBm. The active BALUN (see Fig. 3) converts the single ended signal from the LNA into a balanced signal required at the mixer input. The RF input is ac coupled to the drain of the current source transistor $Mn1$. The operational transconductance amplifier (OTA) ensures a self-biasing mechanism of the BALUN, offset correction at the two differential outputs, and second-order input intercept point (IIP2) improvement of the circuit. For a better matching between $Mn4$ and $Mn2$, the resistors R_x are added. The drain currents of the two transistors have a class AB operation and opposite signs. In order to improve phase matching between outputs, feedforward capacitors have been added in the layout. The OTA has a bandwidth of 40 MHz to control fast varying second-order intermodulation (IM2) components. The BALUN provides gain, isolating the HR mixer from the LNA and improving the overall NF.

Fig. 4 shows one half of the I/Q HR mixer and LPF realized with a trans-impedance amplifier. The individual mixers are ac coupled to the BALUN and driven with six LO phases. The I/Q mixers are driven with quadrature clock phases. By properly scaling the resistor values ($R_B = R_A/\sqrt{2}$) and the dimensions ($W_B = \sqrt{2} * W_A$) of the transistors of the three switching sections [9], the down-conversion products from the third and fifth LO harmonics are rejected. For the chosen bandwidth, the seventh harmonic falls out of the band. The OTA keeps the drains of the switches at virtual ground and filters the high frequency switching components. It fulfills the role of the anti-aliasing filter before sampled-data filter. For the generation of the required eight phases for the I/Q mixers, a sixth-order PPF with resistive interpolation is used (see Fig. 5). Unity gain buffers separate the two third-order sections and reduce the losses. The design is equiripple for the stopband and flat transfer in the pass-band for an LO frequency in the $850 \text{ MHz} \div 6 \text{ GHz}$ band. At the outputs ($O_1 \dots O_8$) of the interpolation network we get eight

Fig. 6. Receiver front-end photomicrograph.

Fig. 7. Measured IIP3 of the receiver front-end.

phases with $\pi/4$ discrete steps and equal amplitudes. For this, the choice of the resistor values in the interpolation network is not arbitrary. For equal amplitudes, R_2 and R_3 are related as $R_3 = 2(1 + \sqrt{2})R_2$ and the choice of R_1 is fairly independent of R_3 and R_2 . The outputs of the interpolation network are applied to low-swing differential CML buffers, for clock generation.

This clocking concept offsets the need of high frequency dividers and rail-to-rail buffers reducing the possible LO contamination through the supply and substrate. The RF front-end is designed and implemented in a baseline CMOS 90-nm LP process. Fig. 6 shows the chip photomicrograph. The active chip area of the receiver front-end including the RF signal path and the LO generation is $1600 \mu\text{m} \times 1088 \mu\text{m}$. The active chip area of the RF signal path is $980 \mu\text{m} \times 1070 \mu\text{m}$.

The measured HRion of the third and the fifth harmonic is -52 and -87 dB, respectively. This is a consequence of the chosen HR mixer and the accuracy of the eight LO phases. Fig. 7 illustrates the measured IIP3 of the implemented front-end. The two test tones are at 1 and 1.001 GHz. The frequency of the LO signal is 997 MHz. The output fundamental signals are at 3 and 4 MHz,

Fig. 8. Measured IIP2 of the receiver front-end.

Fig. 9. Tunable BPF.

Fig. 10. Bandpass filter: Principle of operation.

while the third-order intermodulation (IM3) products are located at 2 and 5 MHz. The measured IIP3 is about -13 dBm.

Fig. 8 shows the measured IIP2 of the front-end. The frequencies of the two test tones are 1.01 and 1.0103 GHz. The frequency of the LO signal is 1 GHz. The output fundamental signals are at 10 and 10.3 MHz, while the IM2 products are located at 999.7 MHz. The measured IIP 2 is $+30$ dBm.

III. IF SELECTIVITY

Fig. 9 shows the new concept of a tunable bandpass IF filter (1.7–6 GHz) for a near zero-IF, multiGb/s WPAN (IEEE802.15.3.c) receiver. In this particular case, the filter provides channel selectivity. This concept can be applied to multimode, multiband receivers for IF selectivity. The filter comprises two broad-band differential LNAs, a sixth-order positive PPF, a high-linearity mixer section preceded by a LPF, and a negative PPF (NPF). The principle of operation for the bandpass PPF (BPF) is depicted in Fig. 10. Firstly, the RF signal at f_{RF} is down-converted to near zero-IF at a frequency f_{IF} . Then, the PPF rejects the negative frequencies

Fig. 11. Positive PPF transfer.

Fig. 12. Harmonic-reject mixer section.

with more than 45–50 dB (Fig. 11). A fixed LPF attenuates higher frequency bands before the first mixing part. Thereafter, the signal is mixed to negative frequencies at $-f_{IF}$ and the NPF rejects the positive frequencies. The mixers are of HR types (see Fig. 4) with high linearity. The result is the desired channel. The sixth-order PPF has an equiripple response in the stopband facilitated by the design procedure and the position of the zeros. The filter has an extra zero at 0 Hz due to the use of a decoupling capacitor in the filter path, before the unity buffers. This extra zero ensures a sharp roll-off for signals out of the passband. The passband transfer has 3-dB voltage gain and below 0.2-dB passband ripple in the whole band of interest. By using a sixth-order PPF, the stopband has a frequency ratio of more than 6 and the stopband attenuation of more than 40 dB. A real advantage of the equiripple transfer is the relative insensitivity to process variations. When the absolute accuracy of the time constants is impaired, due to the mismatch between the sections, the positions of the zeroes are shifted in the same direction, keeping the equiripple behavior. A loss of about 5 dB can be expected from the stopband transfer and attenuation as the capacitors are of MIM type (2% spread) and the resistors of polysilicon type have a spread of 10%. Fig. 12 shows a block diagram of the HR complex mixer. As depicted here, the I/Q complex mixer requires 8-phase LO signals for harmonic rejection and correct operation. As explained in Fig. 10, the complex mixer transforms the central frequency $+f_{IF}$ to a negative frequency $-f_{IF}$. The I signal is multiplied with the first clock sequence and the Q signal is multiplied with the same clock sequence shifted with $\pi/2$ and then added to the first multiplication result. The summation point is the low impedance input of the transimpedance amplifier (TIA). The

Fig. 13. BPF transfer and bandwidth control.

Fig. 14. Bilinear SC resistor and capacitor.

bandwidth of the filter can be adjusted with the crystal precision of the local oscillator. As the higher cutoff frequency of the BPF is fixed by the PPF and an extra series capacitor, the bandwidth control is very accurate, producing truly IF selectivity at gigahertz frequencies without an A/D converter and digital selectivity. In Fig. 13 the simulated bandpass filter transfer and bandwidth control for different LO frequencies is shown. The transition band is extremely narrow (~ 600 dB/decade) due to sharp roll-off in the RC poly-phase and the extra zero @ 0 Hz. The PPF part of the filter can be used for the clock generation of the HR mixer.

For the sampled data filter from Fig. 1, the concept of the tunable bandpass filter from Fig. 9 can be applied again with minor modifications. The bilinear, switched-capacitors network from Fig. 14 has an equivalent resistor and a time constant of

$$R_{eq} = \frac{1}{4 \cdot f_s \cdot C_1}; \quad \tau_{eq} = \frac{C_2}{4 \cdot f_s \cdot C_1}. \quad (3)$$

By replacing the passive RC PPF with the bilinear SC poly-phase sections as in Fig. 15, the result is a sampled data bandpass tunable filter with controllable bandwidth (e.g., from 30 kHz up to 20 MHz to cope with different IF bandwidths present in a multimode, multiband receiver). The sampling frequency is chosen from different constraints: high resistor values of the poly-phase section, low power consumption of the sampling part and a minimum required sample rate related to the filter bandwidth.

Fig. 15. Bilinear SC poly-phase section.

IV. CONCLUSION

We have presented receiver concepts and circuits for future wireless communications standards in a baseline CMOS process. A multimode, multiband receiver architecture was presented and new concepts and circuit topologies were highlighted throughout the paper. In particular, power consumption, NF, and linearity tradeoffs in LNAs and mixers were discussed. In the last part of the paper we described a continuous time tunable bandpass filter for a near zero-IF, Gb/s WPAN receiver. The filter can be tuned with crystal precision in a continuous way from 1.7 to 6 GHz and serves for channel selectivity. The same filter concept can be applied for IF selectivity in a multi-mode, multiband receiver as a replacement for the sampled-data bandpass filters.

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