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A Four-Quadrant S²I Switched-Current Multiplier

Gabriele Manganaro and Jose Pineda de Gyvez

Abstract—The analysis, design, and implementation of a two-step current-sampling switched-current (S²I) multiplier is presented. The S²I technique has been employed to compensate analog errors due to charge injection as well as those arising from the finite output impedance. A thorough circuit analysis investigating the offset sources of the S²I cell and of the multiplier's nonlinearities sets up the platform to effectively design the multiplier and to avoid the use of feedback, or cascode techniques, to deal with channel modulation effects. The multiplier has been implemented using a 2- μ m n-well MOSIS CMOS technology. Experimental results are in agreement with the theoretical findings. The following are brief highlights of the measurement results: 1) 0.425 millions of multiplications per second; 2) 1.7% total harmonic distortion for a sinusoidal of 35- μ A (50 Hz); 3) 206 kHz of bandwidth; 4) 50 dB of SNR; and 5) 0.3-mW zero input power consumption for a ± 3 -V power supply. A complete set of detailed experimental results is provided in the paper.

Index Terms—Analog multipliers, nonlinear circuits, sampled data circuits.

I. INTRODUCTION

ANALOG multipliers are fundamental functional blocks in many circuits and systems [1]–[3]. Sampled-data multipliers were first implemented some time ago using switched capacitor (SC)-based circuits [4]–[9]. Many different approaches have been investigated in this context ranging from time-division charging of a capacitor [4] to multiplication of binary numbers by interfacing an analog multiplier with DAC's and ADC's [5]. Other approaches have been based on depletion-mode MOS transistors (DMOST's) operated in the triode region and embedded in SC-based circuits [6]–[7]; multivalued logic [8] and pulse-based arithmetic [9] SC multipliers have been presented as well.

Switched-current (SI) circuits [10] represent a feasible alternative to SC circuits especially due to their compatibility with digital technology. However, although some nonfiltering applications of SI circuits have been developed [10], [11], to the best knowledge of the authors, only one SI multiplier has ever been presented until now [1]. The complexity of this circuit required one extra clock phase besides the normal clock phases used in common second generation SI cells [10], two explicit capacitors to cope with clock feedthrough problems, and a regulated-cascode architecture to deal with channel modulation effects [1]. In this circuit, the multiplication of any

two given currents x and y is accomplished by evaluating their quadratic terms: $(x+y)^2 - x^2 - y^2 = 2xy$. One smart aspect of Leenaert's [1] multiplier is that any quadratic term is evaluated by using the same squarer circuit in different clock phases. This avoids the need for precisely matched squarer circuits as is the case in some continuous time current multipliers [2].

This paper presents an alternative implementation by using the S²I switched-current technique that has already been proven effective in filtering and converting applications [12]–[14]. One of the most important features of S²I is that it allows to compensate for analog errors due to charge injection [10], [14], [15] as well as for those arising from the finite output impedance. The signal-dependent clock feedthrough is sampled and stored in the initial sampling phase of the current copier operation and then algebraically added to the corrupted current to minimize the corresponding error. Likewise, more sophisticated circuit techniques have been applied to this elementary circuit architecture [13], [14]. We have considered only the basic cell in the design of the multiplier.

II. ANALYSIS OF THE S²I MEMORY CELL

The circuit of an S²I cell and its phases is shown in Fig. 1. M_C is referred to as the *coarse memory* while M_F is called the *fine memory*. Fig. 2 shortly reports a small-signal analysis of the cell: i_{1a} and i_{1b} are the currents stored on ϕ_{1a} and ϕ_{1b} , respectively, while Δi is the clock feedthrough. Current δI is mainly the offset due to the signal-independent clock feedthrough in M_F , and g_{0F} is the total output impedance of M_F augmented by the feedback effect due to its drain-gate capacitance. Notice that $i_i(n-1) \cong i_{1a}$, therefore only the coarse memory error is stored into the fine memory [Fig. 2(b)] on ϕ_{1b} . Moreover, most of the input current $i_i(n-1)$ is nulled by i_{1a} making the actual input resistance smaller than its equivalent on ϕ_{1a} . The dimensionless constant Ψ is the voltage gain of a CMOS inverter in which M_F works as the current source and M_C works as the driver. The final output current $i_0(n-1/2)$ is

$$\begin{aligned} i_0(n-1/2) &= -i_i(n-1) \frac{g_{mF}}{g_{mF} + g_{0C} + g_{dsF}} \frac{g_L}{g_{0C} + g_{0F} + g_L} \\ &\quad - \Delta i \alpha - i_{1a} \alpha - \delta I \frac{g_L}{g_{0C} + g_{0F} + g_L} \end{aligned} \quad (1a)$$

$$\alpha \equiv \left(1 - \frac{g_{mF}}{g_{mF} + g_{dsF} + g_{0C}} \right) \frac{g_L}{g_{0C} + g_{0F} + g_L}. \quad (1b)$$

Observe from (1b) that the first term in brackets is close to 0 while the other one is less than 1. Therefore, the second and

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Fig. 1. S²I memory cell and clock waveforms.

third terms can be neglected in (1a). Let us now assume that all the MOST have the same small-signal transconductance g_m . Two cases are distinguished: if the load consists of a diode-connected transistor (e.g., another current mode stage) then $g_L = g_m$. If, instead, the load is another S²I memory cell then ϕ_2 is partitioned into ϕ_{2a} (during which $g_L = g_m$) and ϕ_{2b} (during which $g_L \cong (g_{mC}g_{mF})/(g_{dsF} + g_{dsC}) = \Psi g_m$). In the former case, the information retrieved from the memory is underestimated when $g_{dsF} = g_{0F}$ in (1):

$$i_0(n-1/2) \cong -i_i(n-1) \left(\frac{g_m}{g_{0C} + g_{0F} + g_m} \right)^2 - \delta I \frac{g_m}{g_{0C} + g_{0F} + g_m}. \quad (2)$$

Taking $g_0 = g_{0F} = g_{0C}$, (2) can be approximated to

$$\begin{aligned} i_0(n-1/2) &\cong -i_i(n-1) \frac{1}{1 + 4 \frac{g_0}{g_m}} - \delta I \frac{1}{1 + 2 \frac{g_0}{g_m}} \\ &= -i_i(n-1) \frac{1}{1 + 4 \frac{g_0}{g_m}} + i_{\text{offset}} \end{aligned} \quad (3)$$

where i_{offset} represents the output current offset. Given that the ideal signal function of an S²I cell is $H_i(z) = I_0(z)/I_i(z) = -z^{-1/2}$, we can take the z -transform

$$I_0(z) \cong I_i(z) \frac{H_i(z)}{1 + 4 \frac{g_0}{g_m}} + I_{\text{offset}}(z). \quad (4)$$

A perfect signal-dependent clock feedthrough cancellation is obtained considering only the effect of the channel length modulation of M_F and M_C on ϕ_2 . The corresponding final expression is

$$I_0(z) = I_i(z) \frac{H_i(z)}{1 + \frac{g_{0T}}{g_m}} + I_{\text{offset}}(z) \quad (5)$$

where $g_{0T} = g_{0F} + g_{0C}$ is the total output conductance of the memory cell.

When, instead, the load of the memory cell is constituted by another S²I cell, then the load changes to $g_L \cong \Psi g_m$ during

ϕ_{2b} . Therefore, g_L dominates over the output impedance of the cell allowing to completely transfer the output current $i_0(n-1/2)$ to the next stage. This implies that (2) is substituted by

$$i_0(n-1/2) \cong -i_i(n-1) \frac{g_m}{g_{0C} + g_{0F} + g_m} - \delta I \frac{\Psi g_m}{g_{0C} + g_{0F} + \Psi g_m}. \quad (6)$$

The fractional term multiplying δI in (6) is very close to one. Moreover, taking $g_0 = g_{0F} = g_{0C}$:

$$i_0(n-1/2) \cong -i_i(n-1) \frac{1}{1 + 2 \frac{g_0}{g_m}} - \delta I. \quad (7)$$

Equation (7) is formally equal to (5) considering that the total output conductance is $2g_0$. If, however, as it is commonly assumed [10], the channel modulation is neglected on ϕ_{1a} and ϕ_{1b} but considered on ϕ_2 , then we have: 1) there is no current attenuation on ϕ_{1a} and ϕ_{1b} and 2) the Norton equivalent of the S²I cell (with an output conductance equal to $2g_0$) transfers the retrieved current to a load with conductance equal to Ψg_m on ϕ_{2b} . Hence

$$I_0(z) = I_i(z) \frac{H_i(z)}{1 + \frac{2g_0}{\Psi g_m}} + I_{\text{off}}(z). \quad (8)$$

This analytically proves that the S²I cell achieves not only the feedthrough cancellation but it also reduces the error due to the finite g_m/g_0 ratio as compared with common second-generation cells [12]–[13]. Moreover, this analytical result is in complete agreement with the simulation [12] and experimental results [13], [14] obtained by Hughes *et al.*

The sampling frequency in common second-generation cells is limited by the settling time of the cell sampler [10]. In the case of S²I, the cell treats the coarse phase ϕ_{1a} settling error as the other errors and so attempts to cancel it during the fine phase ϕ_{1b} . This means that the bandwidth is the same as that of a standard second-generation cell.

Fig. 2. Small-signal analysis for the S²I memory cell. Phase: (a) ϕ_{1a} , (b) ϕ_{1b} , and (c) ϕ_2 .

III. THE S²I MULTIPLIER ARCHITECTURE

Starting from the algorithm introduced by Leenaerts *et al.* [1], an alternative circuit implementation is now presented. The product of two currents x and y fed at the inputs of the multiplier is accomplished by evaluating the left-hand side of (9):

$$(x + y)^2 - x^2 - y^2 = 2xy. \quad (9)$$

The squarer circuit shown in Fig. 3 has been considered [16] in order to obtain the square of a current. For this circuit, a relationship including the input/output offset errors gives

$$i_0 = I_b + e_1 + \frac{(i_i + e_2)^2}{4I_b} \quad (10)$$

Fig. 3. The current squarer.

Fig. 4. Block diagram of the S^2I multiplier.

where i_0 and i_i are the output and input currents, respectively, I_b is a constant current related to the bias voltage V_{bias} , e_1 is the output offset error, and e_2 is the input offset error. The approach introduced in [1] consists of using the same squarer circuit many times while storing intermediate results in the SI memory cells.

The block diagram of the whole system realizing the above algorithm is depicted in Fig. 4. The algorithm consists of four main steps described by means of four main clock phases: ϕ_1 , ϕ_2 , ϕ_3 , ϕ_4 . The circuitry consists of three building blocks: the current squarer, an adjustable current mirror, and two S^2I memory cells. From this figure it is seen that, analogously to [1], a complementary version of the squarer circuit shown in Fig. 3 is used. In this way, due to the fact that the adopted technology is a CMOS n-well, it is possible to avoid the bulk effects on M_2 by connecting its source to the n-well.

As recalled in Section II, the S^2I cell minimizes the channel length modulation effect and implicitly the problem of the finite g_m/g_0 ratio in comparison to other SI cells not utilizing cascode or feedback-based approaches. However, the retrieved contents of the memory cells are expected to have an attenuation. Among the four steps, the biggest unbalance occurs during ϕ_4 because the squared input signal is directly added up to the rest of the previously calculated results without an equally corresponding attenuation. Therefore, during this last phase, the ratio of the mirror is changed so that the unbalance is compensated. The mirror has unity gain during all the phases but ϕ_4 . Strictly speaking, similar problems are expected also in phases ϕ_2 and ϕ_3 . Therefore, for better accuracy, a similar ratio-tuning can also be accomplished in those phases with only a small increase in the complexity of the system. However, simulation results have clearly shown that for a satisfying accuracy [nonlinearity of around $\pm 1\%$ full scale (FS)] this is not necessary. The analysis of this behavior is reported in the next section.

The circuit schematic of the complete multiplier is shown in Fig. 5(a). In this figure, it is clearly seen how the current gain of the mirror is slightly changed during ϕ_4 by adding a small-area diode-connected MOST parallel to the existing one. This, however, will cause an extra bias current coming out from the right branch of the mirror due to the unbalance in I_b . This will add up to the constant offset error present in the output of the S^2I cells and will cause a constant current offset on I_{out} . This

undesired offset can be canceled in two ways. If the multiplier is going to be used alone, an extra current can be added during ϕ_4 by using an additional current source and a current steering switch. This is realized by M_{10} , as shown in Fig. 5(a). This is, for example, what has been done in the fabricated chip whose experimental results are discussed in Section V. If, instead, many multipliers are going to be used in the same chip (as in the case of a neural network or in the case of adaptive filters and so on), then a more suitable technique consists of realizing another multiplier (namely a replica multiplier) without inputs. The output current offset of this multiplier is added up to the outputs of all the other multipliers by using current mirrors. In this way, the output offset of the other multipliers can be drastically reduced in spite of process variations.

Seven of the nine control signals used to drive the switches are depicted in Fig. 5(b). The other two signals are $\phi_2 + \phi_3 = \phi_1 + \phi_4$ and $\phi_3 + \phi_4 = \phi_1 + \phi_2$. The nine control signals are obtained as combinations of the various “master” phases. It can be noticed that while the sub-phases used to control the internal switches of the memory cells are not overlapping (namely, $\phi_{1a} + \phi_{3a}$, $\phi_{1b} + \phi_{3b}$, ϕ_{2a} , ϕ_{2b}), the current steering switches are controlled by signals with overlapping rising and falling edges ($\phi_1 + \phi_4$, $\phi_1 + \phi_2$, ϕ_4). This minimizes the generation of current spikes without interfering with the operation of the circuit.

IV. ANALYSIS AND DESIGN OF THE S^2I MULTIPLIER

In this section, the behavioral analysis of the S^2I multiplier is carried out. The approach presented takes into account the nonidealities of the circuits and devices. Eventually, an algorithm for the circuit design of the multiplier is discussed.

A. Circuit Analysis of the Multiplier

In [12] and [13], the behavior and some of the applications of the S^2I cell have been discussed. However, to analyze the proposed multiplier, the effect of the finite conductance ratio in the memory cells, as well as in the other building blocks, has to be taken into account. These topics are discussed below.

For the sake of clarity, it will be assumed that all the g_m 's are equal and that all the g_{ds} 's are equal as well. Strictly speaking, a complete analysis requires the behavioral analysis of the multiplier in seven phases (ϕ_{1a} , ϕ_{1b} , ϕ_{2a} , ϕ_{2b} , ϕ_{3a} ,

Fig. 5. (a) Circuit schematic of the S^2I multiplier and (b) control signals for the switches.

ϕ_{3b} and ϕ_4). However, taking advantage of the analysis of the S^2I memory cell carried out in Section II, we can consider its small-signal equivalent circuit as follows. During ϕ_1, ϕ_2 , and ϕ_3 , the memory cell working in the sampling phase (composed by the two subphases “a” and “b”) has a small signal equivalent circuit consisting of a conductance equal to Ψg_m . The current stored in the cell is the one flowing into this conductance. During the retrieval phase the small-signal circuit is composed of an ideal current source supplying the current stored in the previous phase in parallel with a conductance equal to $2g_{ds}$. Notice that, although the cells supply a fixed output offset when the stored current is retrieved, we can nevertheless implicitly consider this offset as part of the squarer offset e_1 . During ϕ_4 , instead, the circuit load is assumed to be the generic conductance g_L . Therefore, the analysis is carried out in the four main phases ϕ_1, ϕ_2, ϕ_3 , and ϕ_4 .

Let us now refer to the complete circuit schematic shown in Fig. 5(a) and to the small-signal equivalents shown in Fig. 6. The current source I_1 depicted in Fig. 5(a) is implemented by using a single PMOS supplying a constant current equal to I_b . According to the discussion of Section III, the mirror $M_{4a}-M_5$ supplies the following current (11) in phase ϕ_1 :

$$i_1 = -\left(e_1 + \frac{(x + y + e_2)^2}{4I_b}\right). \quad (11)$$

The corresponding small-signal equivalent is shown in Fig. 6(a). Here, g_{0M} represents the output conductance of the right-hand-side branch of the current mirror. Therefore, following the previous discussion, we have that $g_{0M} = 2g_{ds}$. Notice that only cell 1 is connected to node A and that the input conductance of the memory cell is Ψg_m . Hence, the

Fig. 6. Small-signal equivalent circuits for the S^2I multiplier. (top left) Phase ϕ_1 . (top right) Phase ϕ_2 . (bottom left) Phase ϕ_3 . (bottom right) Phase ϕ_4 .

current stored in the cell is

$$i_{s1} = \frac{\Psi g_m}{\Psi g_m + 2g_{ds}} i_1. \quad (12)$$

In phase ϕ_2 , the mirror supplies i_2 which is added to i_{s1} (retrieved from cell 1) and the result is stored in cell 2. Again, the actual current stored in cell 2 is the one flowing into Ψg_m . Hence, from the small-signal equivalent circuit shown in Fig. 6(b):

$$i_2 = -\left(c_1 + \frac{(x + e_2)^2}{4I_b}\right); \quad i_{s2} = \frac{\Psi g_m}{\Psi g_m + 4g_{ds}} [i_2 - i_{s1}]. \quad (13)$$

In phase ϕ_3 , the mirror supplies i_3 which is added to i_{s2} supplied by cell 2 and the result i_{s2} is stored into cell 1. Thus, considering the small-signal equivalent circuit depicted in Fig. 6(c)

$$i_3 = -\left(c_1 + \frac{(e_2)^2}{4I_b}\right); \quad i_{s3} = \frac{\Psi g_m}{\Psi g_m + 4g_{ds}} [i_3 - i_{s2}]. \quad (14)$$

Finally, in phase ϕ_4 , the mirror changes its ratio. This is accomplished by shunting M_{4b} and M_{4a} . The ratio changes from 1:1 to 1: β with $\beta < 1$. However, because the bias current on the left branch of the mirror is not changed, an extra current $(1-\beta)I_b$ is supplied by its right-hand-side branch. This represents an output offset that can be canceled as discussed in the previous section. In terms of the small-signal analysis, the mirror supplies i_4 which is added to i_{s3} supplied by cell 1. The result is that i_o flows into the output load g_L . So, from the small-signal equivalent circuit of Fig. 6(d)

$$i_4 = -\left(c_1 + \frac{(y + e_2)^2}{4I_b}\right)\beta; \quad i_o = \frac{g_L}{g_L + 4g_{ds}} [i_4 - i_{s3}]. \quad (15)$$

Substituting (12)–(14) into (15), the following expression is obtained:

$$i_o = \left\{ i_4 - \left[i_3 - \left(i_2 - \frac{\Psi g_m}{\Psi g_m + 2g_{ds}} i_1 \right) \frac{\Psi g_m}{\Psi g_m + 4g_{ds}} \right] \times \frac{\Psi g_m}{\Psi g_m + 4g_{ds}} \right\} \frac{g_L}{g_L + 4g_{ds}}. \quad (16)$$

Defining

$$\eta \equiv \frac{\Psi g_m}{\Psi g_m + 4g_{ds}} \\ \rho \equiv \frac{g_L}{g_L + 4g_{ds}}. \quad (17)$$

Equation (16) can be approximated to

$$i_o \cong \{i_4 - [i_3 - (i_2 - \eta i_1)\eta]\rho\} \\ = \{i_4 - i_3\eta + i_2\eta^2 - i_1\eta^3\}\rho = i\rho \quad (18)$$

where i is just a current proportional to the actual output current i_o . Let us then analyze i by substituting i_1 , i_2 , i_3 , and i_4 from (11)–(15) into (18). After some algebra, the following relationship is obtained:

$$i = c_1(\eta^3 - \eta^2 + \eta - \beta) + c_2^2 \frac{1}{4I_b}(\eta^3 - \eta^2 + \eta - \beta) \\ + \frac{x^2}{4I_b}\eta^2(\eta - 1) + \frac{y^2}{4I_b}(\eta^3 - \beta) \\ + \frac{xe_2}{2I_b}\eta^2(\eta - 1) + \frac{ye_2}{2I_b}(\eta^3 - \beta) + \frac{\eta^3}{2I_b}xy. \quad (19)$$

The first two terms of the right-hand side represent an offset, the last term is the desired result, while the remaining terms constitute the nonlinear distortion. Note that η is very close but less than 1. Therefore, the third and fifth terms, being multiplied by a factor $\eta^2(\eta - 1)$, can be neglected. Thus, relationship (19) can be rewritten as

$$i = i_{\text{off}} + \frac{y^2}{4I_b}(\eta^3 - \beta) + \frac{ye_2}{2I_b}(\eta^3 - \beta) + \frac{\eta^3}{2I_b}xy \\ i_{\text{off}} = c_1(\eta^3 - \eta^2 + \eta - \beta) + c_2^2 \frac{1}{4I_b}(\eta^3 - \eta^2 + \eta - \beta) \quad (20)$$

where i_{off} is the offset current. The nonlinear error is canceled by setting the current mirror ratio as

$$\beta = \beta_0 \equiv \eta^3 = \left(\frac{1}{1 + \frac{4g_{ds}}{\Psi g_m}} \right)^3. \quad (21)$$

The final expression is therefore

$$i = c_1(-\eta^2 + \eta) + c_2^2 \frac{1}{4I_b}(-\eta^2 + \eta) + \frac{\eta^3}{2I_b}xy. \quad (22)$$

It is worth noting that because $\eta \cong 1$ the offset is almost canceled as well. It follows then that

$$i_o \cong \frac{\eta^3 \rho}{2I_b} xy. \quad (23)$$

The analysis carried out in this section demonstrates the big advantage that the proposed architecture has on the effect of the nonlinearity cancellation by selecting the appropriate mirror gain.

B. Circuit Design

Let us consider the circuit diagram shown in Fig. 5 and, for the sake of clarity, assume a symmetric power supply ($V_{dd} = -V_{ss}$). Let us consider the two memory cells composed by M_6 – M_9 and the corresponding switches. The quiescent drain voltages of the MOST's are chosen to stay at ground. To avoid the drain voltage of these transistors jumping when the switches turn on or off, M_6 and M_9 are designed for

$$|V_{GS}| = |V_{DS}| = |V_{dd}|. \quad (24)$$

Therefore $V_{ref} = 0$ V. The bias current I_D can be chosen to be a safe value for the adopted technology. Alternatively, it can be chosen to satisfy other possible requirements on g_m and/or g_{ds} or for a desired S/N ratio. From these considerations the aspect ratios are determined as

$$\begin{aligned} \left(\frac{W}{L}\right)_{NMOST} &= \frac{2I_D}{K'_N(V_{dd} - V_{TN})^2(1 + \lambda_N V_{dd})} \\ \left(\frac{W}{L}\right)_{PMOST} &= \frac{2I_D}{K'_P(V_{dd} - |V_{TP}|)^2(1 + \lambda_P V_{dd})}. \end{aligned} \quad (25)$$

There is still a degree of freedom that allows us to choose either W or L . Two alternatives are possible. If the output impedance of the cell is of major concern then L is fixed and W is determined accordingly. The second alternative regards the area WL . Larger areas minimize the clock feedthrough. On the other hand, smaller areas are necessary for high speed.

Both transistors M_4 and M_5 constitute a current mirror. Hence, to minimize the current error due to the channel modulation effect, the quiescent drain voltage of M_{4a} is chosen to stay at ground. M_1 , M_2 , and M_3 constitute the squarer circuit and it is assumed that all of them are equal [16]. Hence, from the above considerations, it follows that the quiescent drain voltage of M_1 stays at $V_{dd}/2$. The square law holds for $|i_i| < 2I_b$ [16], [1]. Therefore, a minimum value for I_b is fixed because the maximum value of $|i_i|$ is essentially given by $|x_{max}| + |y_{max}|$. Taking into consideration the above assumptions for the node voltages and the fact that M_1 , M_2 , and M_3 are biased for a drain current equal to $I_b/2$, while M_{4a} and M_5 are biased for a drain current equal to I_b , the design of these transistors is then straightforward.

In (21), the mirror ratio (current gain) has been obtained. Assuming that $(W/L)_5 = (W/L)_{4a}$, the aspect ratio of M_{4b} is obtained as follows:

$$\left(\frac{W}{L}\right)_{4b} = \left(\frac{W}{L}\right)_{4a} \left(\frac{1-\beta}{\beta}\right). \quad (26)$$

However, the final design of M_{4b} also depends on the actual voltage drop of the switch in series with M_{4b} . A common measure of the accuracy is given by the difference between the multiplier's actual and ideal output, at full scale, as a percentage of the full scale itself. This is known as *internal trim error* ε [3]. This includes the effect of offset, feedthrough, nonlinearity, and scale-factor errors. A plot of ε versus β , obtained by HSPICE simulation for a 100-kHz clock frequency and large signals, is shown in Fig. 7(a).

Let us now consider the switches. The control voltages for the switches go from rail to rail while their terminals

(a)

(b)

Fig. 7. (a) Percentage trim error (ε) versus mirror correction factor (β). The total error correction is obtained for the optimal value $\beta_0 = 0.5161$ in the considered example. (b) Measured transfer characteristic. Output current I_o versus input current I_x . The original scales are in volts (see text). The corresponding currents are reported.

stay at a voltage close to ground during the whole operation of the circuit. Therefore, minimum size switches can easily be designed by using either NMOS transistors or CMOS transmission gates. However, for the adopted technology, no appreciable difference has been noticed by substituting the NMOST's with the CMOS switches, thus, single NMOST's have been used in the considered implementation. There is one exception only: because the voltage at the drain of M_1 is $V_{dd}/2$ the two switches steering the currents x and y at the input of the squarer are implemented using CMOS switches instead of simple NMOST's.

V. EXPERIMENTAL PERFORMANCE EVALUATION

A prototype of the proposed multiplier has been fabricated in MOSIS Orbit n-well 2- μ m technology. In this section, the experimental results obtained by testing the chip are discussed. A summary of the measured parameters is reported in Table I.

The control signals for the switches have been generated on-chip by means of digital circuitry [17], [18] driven by an external master clock of frequency f_c . The multiplier performs $f_c/4$ multiplications per second since the frequency of the four phases ϕ_1 to ϕ_4 is $f_c/4$. The nominal clock frequency is $f_c = 400$ kHz. Indeed, it has been experimentally verified

TABLE I
PERFORMANCE OF THE TESTED CHIP

Output function (ideal)	$I_{out} = 5000 A^{-1} I_x I_y$
Input range	$\pm 35 \mu A$
Max output current	$\pm 6 \mu A$
Internal Trim error ε (Full Scale)	1.0% at $f_c = 400 KHz$ 1.5% at $f_c = 1.7 MHz$
THD ($I_x = 35 \mu A$, $I_y = 35 \mu A \sin(2\pi 50)$)	1.73%
Accuracy vs. Supply	0.2% / %
SNR	50 dB
Output offset	200 nA
x-feedthrough	< 200 nA
y-feedthrough	200 nA
-3dB Small-signal bandwidth	200 KHz at $f_c = 1.7 MHz$
Full power response	150 KHz at $f_c = 1.7 MHz$
Max clock frequency f_c	1.7 MHz
Max throughput	0.420 MOPS at $f_c = 1.7 MHz$
Die area	$225 \times 250 \mu m^2$
Power consumption	0.3 mW
Power supply	$\pm 3V$

that the maximum frequency at which the circuit works without appreciable performance degradation (1.5% FS) is $f_c = 1.7$ MHz, corresponding to 0.425 million multiplications per second. The input currents have been provided by means of off-chip $V-I$ converters. In particular, two Howland circuits have been used [19]. The output current of the multiplier is measured by feeding a 2.2-k Ω grounded resistor. The power supply is ± 3 V and the power consumption with zero inputs is 0.3 mW (essentially constant until $f_c = 1.7$ MHz).

The multiplier's ideal transfer characteristic is $I_{out} = 5000 A^{-1} I_x I_y$. The measured input current ranges from -35 to $35 \mu A$ with a maximum output current of $\pm 6 \mu A$. It has also been verified that the multiplier is still working for an input range of around $\pm 40 \mu A$ but with reduced linearity as shown in Fig. 8(a). The experimental transfer characteristic of the multiplier is shown in Fig. 7(b). Due to the inherently discrete-time nature of the circuit, the output current is a pulse train and its envelope corresponds to the result of the multiplication. Thus, in order to trace the curves of Fig. 7(b), the voltage swing at the output resistor has been amplified and filtered by using a lowpass filter that separates the carrier from the envelope. The curve has been traced using an HP 4145B curve tracer and the corresponding currents are reported close to the original instrument scales.

As previously pointed out, in this realization the constant offset current is internally compensated by inserting during phase ϕ_4 a current source in node A (realized by the NMOST). However, due to unavoidable process variations, an offset current of 200 nA has been measured at the output. This can be easily zeroed by a suitable shift of the voltage level of the second terminal of the output resistor (less than 1 mV in our case).

An internal trim error of 1.0% FS has been measured at a clock frequency of $f_c = 400$ kHz. This degrades to 1.5% FS at $f_c = 1.7$ MHz. More complete information on the nonlinearity is given by the total harmonic distortion (THD) for a sinusoid at 50 Hz. The trim error, in fact, is referred only to the accuracy at full scale, while the THD involves the entire range of operation of the circuit. In order to measure THD, a 50-Hz sinusoid is fed at one input while the other

(a)

(b)

Fig. 8. (a) Total harmonic distortion versus input currents. It is worth remembering that the full scale value is $35 \mu A$. (b) x -feedthrough (dashed line) and y -feedthrough (solid line) versus clock frequency.

input is held constant. From the analysis carried out in the previous section, it turns out that the input current that mainly affects the linearity is I_y . Therefore, a worst-case result is obtained if the sinusoidal signal is fed on the input y . This is the case herewith considered. The THD has been measured by acquiring the spectrum of the output current using an HP 3588A spectrum analyzer. A plot of the THD for different values of the sinusoid amplitude and of I_x is shown in Fig. 8(a). The plot includes values outside the normal range of operation as well. Measurements obtained with negative I_y are analogous to the one shown in Fig. 8(a).

Another important performance parameter is the *input feedthrough* [3]. In particular, the *x-feedthrough* refers to the case in which the y input is zero. Conversely, the *y-feedthrough* refers to the case in which the x input is zero. The maximum values of feedthrough obtained by keeping one of the inputs at zero and varying the other input through the full allowed range are depicted in Fig. 8(b) as a function of the clock frequency. The -3 -dB small-signal bandwidth, measured at a clock frequency of $f_c = 1.7$ MHz, is close to 200 kHz. It is worth mentioning that, in practice, higher clock frequencies are hardly applicable and the performance of the circuit rapidly starts to degrade. The full power bandwidth, at $f_c = 1.7$ MHz, is 150 kHz. Finally, the percentage of THD variation at full scale for a variation of the power supply is

Fig. 9. Die microphotography of the multiplier.

0.213%/ (i.e. -13 dB %/%) while the SNR is 50 dB (again, as well as for the measurement of the THD, this is the worst case: the signal is fed to y while x fixes the gain).

A die photograph of the multiplier is shown in Fig. 9. The whole area, including the references for biasing the circuit is $225 \times 250 \mu\text{m}^2$.

VI. CONCLUSION

The design, analysis, and experimental results of an S^2I switched-current multiplier have been presented. A comprehensive analysis to understand the sources of offsets and nonlinearities of our circuit has been performed. It has been found that, by appropriately setting a current-mirror gain, the nonlinearity can effectively be canceled. An actual IC prototype was fabricated using MOSIS n-well $2\text{-}\mu\text{m}$ technology. Experimental results are consistent with theoretical findings. The use of improved S^2I cells described in [13] can enhance the performance even more.

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